QAP
Quad Analog POTS
PEB 3465 Version 1.2

Wired
Communications

Infineon
technologies

N e v e r   s t o p   t h i n k i n g .

Attention please!

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide (see address list).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

QAP
Quad Analog POTS
PEB 3465 Version 1.2

PRELIMINARY

Wired
Communications

Infineon
technologies

Never stop thinking.

Previous Version:

Page	Subjects (major changes since last revision)

For questions on technology, delivery and prices please contact the Infineon Technologies Offices in Germany or the Infineon Technologies Companies and Representatives worldwide: see our webpage at http://www.infineon.com

Table of Contents   **Page**

List of Figures   Page

List of Tables   Page

PRELIMINARY

1   General Description

The highly integrated MuSLIC chip set supports to realize an extremely compact Analog Subscriber Line Interface Module. Only a few external components are required and there is no trimming or adjustment necessary to meet worldwide recommendations.

The chip set consists of three out of seven available ICs:

Table 1   MuSLIC Chip Set ICs

PEB 31664	MuPP µC-S	
PEB 31665	MuPP IOM®-2	Multichannel Processor for POTS
PEB 31666	MuPP µC-E	
PEB 3465	QAP	Quad Analog POTS
PEB 4164	AHV-SLIC-S	
PEB 4165	AHV-SLIC	Advanced High Voltage Subscriber Line Circuit
PEB 4166	AHV-SLIC-E	

The Quad Analog POTS IC (QAP) PEB 3465 provides all analog frontend functions for four completely independent channels. Each channel is equipped with all necessary A/D- and D/A converters and filter functions for the AC and DC- path as well with a control and supervision interface to the AHV-SLIC, including digital I/O pins for channel specific control functions. Additionally the QAP provides analog input pins for measurement purposes.

Only four signals are needed for the highspeed serial interface to the MuPP IOM-2/MuPP µC ("MuPP"), which provides all signal processing and system interfacing for 16 channels.
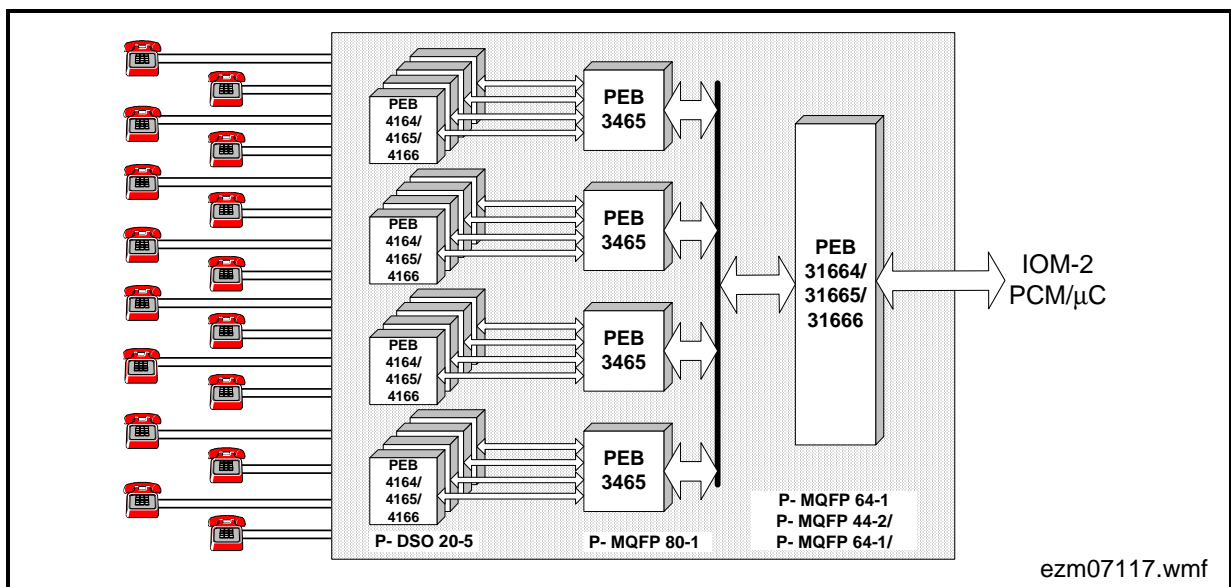
Figure 1   Application of an Analog Linecard for 16 Subscribers using MuSLIC

PRELIMINARY

Quad Analog POTS   PEB 3465
QAP

Version 1.2

1.1   Features

- Four channel analog frontend for POTS
- Only a few external components are required
- No trimming or adjustments are required
- Advanced low power BiCMOS[1] technology
- High performance AD and DA conversion
- Four pin serial interface
- Three operating modes:
  Power Down, Active and Ringing
- Standard SMD P-MQFP-80-1 package

P-MQFP-80-1

---
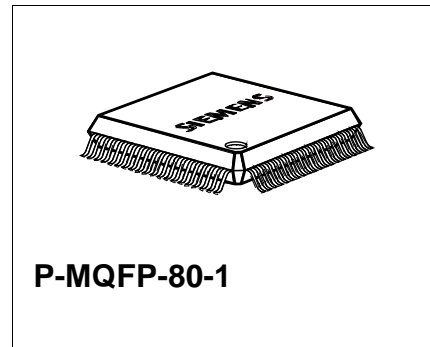
[1]   Abbreviations see **Page 41**

Type	Package
PEB 3465	P-MQFP-80-1

PRELIMINARY

1.2 Pin Configuration (Top View)

Figure 2 Pin Configuration (Top View)

PRELIMINARY

1.2.1 Pin Definition and Functions

The following tables group the pins according to their functions. They include pin number, pin name, type, a brief description of the function, and cross-references referring to the sections in which the pin functions are discussed.

Table 2   Pin Definition and Functions

Pin No.	Name	Type	Function

Power Supply Pins

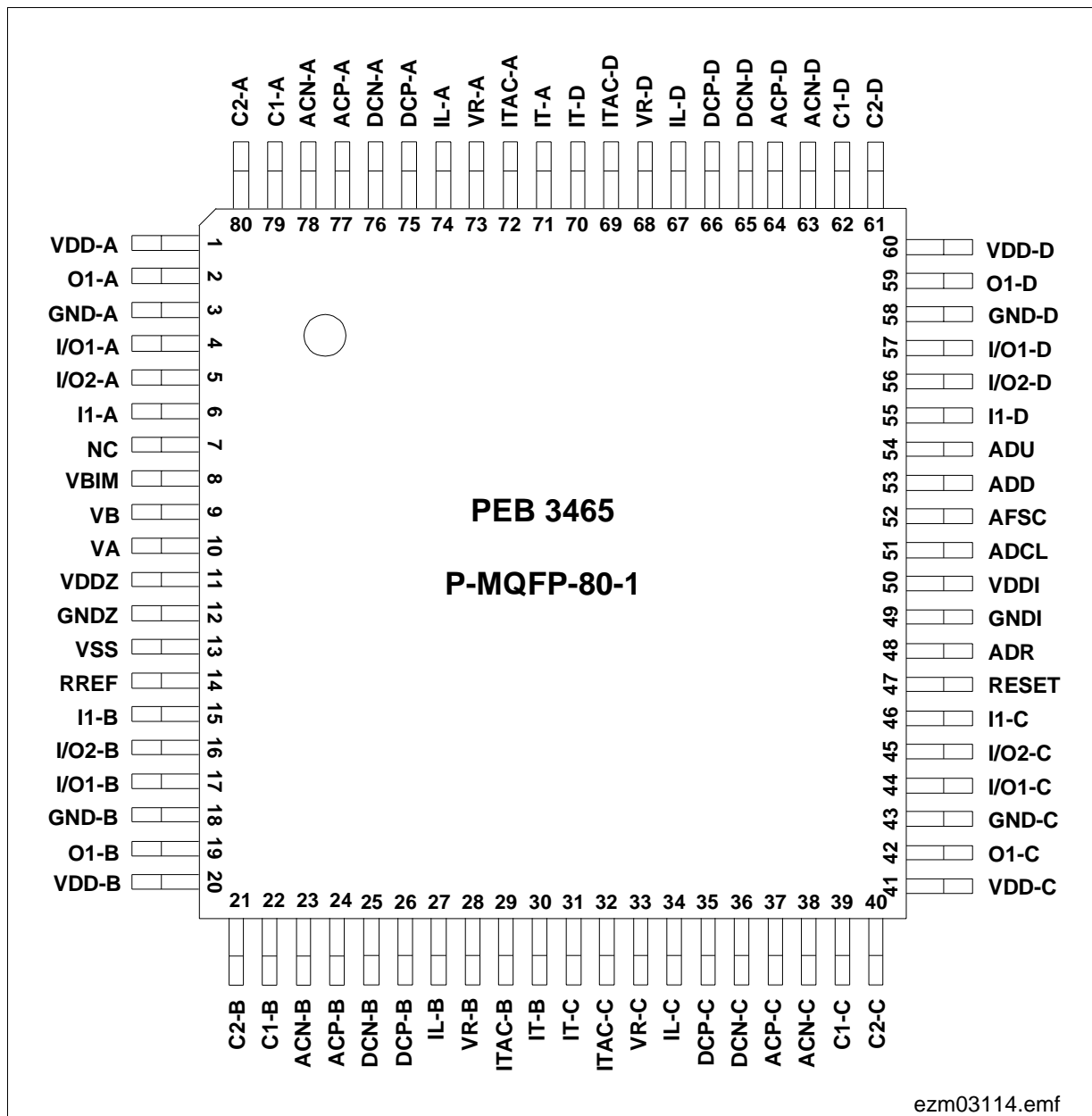| Pin No.	Name	Type	Function
1	VDD-A	–	+ 5 V analog supply voltage (channel A)
20	VDD-B	–	+ 5 V analog supply voltage (channel B)
41	VDD-C	–	+ 5 V analog supply voltage (channel C)
60	VDD-D	–	+ 5 V analog supply voltage (channel D)
3	GND-A	–	Analog ground (channel A)
18	GND-B	–	Analog ground (channel B)
43	GND-C	–	Analog ground (channel C)
58	GND-D	–	Analog ground (channel D)
11	VDDZ	–	+ 5 V analog supply voltage (bias)
12	GNDZ	–	Analog ground (bias)
13	VSS	–	– 5 V analog supply voltage
50	VDDI	–	+ 3.3 V or + 5 V digital supply voltage
49	GNDI	–	Digital ground

Interface Pins to MuPP

Pin No.	Name	Type	Function
54	ADU	O	Analog data upstream
53	ADD	I	Analog data downstream
51	ADCL	I	Analog data-clock
52	AFSC	I	Analog frame-sync.
48	ADR	I	Select odd or even port nr.
47	RESET	I	Interface-reset (active high)

PRELIMINARY

Table 2   Pin Definition and Functions (Continued)

Pin No.	Name	Type	Function

Interface to AHV-SLIC

Pin No.	Name	Type	Function
71	IT-A	I	Transversal current input (AC+DC), channel A
72	ITAC-A	I	Transversal current input (AC), channel A
73	VR-A	I	Reference input, channel A
74	IL-A	I	Longitudinal current input, channel A
77	ACP-A	O	Two wire output voltage (ACP), channel A
78	ACN-A	O	Two wire output voltage (ACN), channel A
75	DCP-A	O	Two wire output voltage (DCP), channel A
76	DCN-A	O	Two wire output voltage (DCN), channel A
79	C1-A	I/O	Digital interface to AHV-SLIC, channel A
80	C2-A	O	Digital interface to AHV-SLIC, channel A
30	IT-B	I	Transversal current input (AC+DC), channel B
29	ITAC-B	I	Transversal current input (AC), channel B
28	VR-B	I	Reference input, channel B
27	IL-B	I	Longitudinal current input, channel B
24	ACP-B	O	Two wire output voltage (ACP), channel B
23	ACN-B	O	Two wire output voltage (ACN), channel B
26	DCP-B	O	Two wire output voltage (DCP), channel B
25	DCN-B	O	Two wire output voltage (DCN), channel B
22	C1-B	I/O	Digital interface to AHV-SLIC, channel B
21	C2-B	O	Digital interface to AHV-SLIC, channel B
31	IT-C	I	Transversal current input (AC+DC), channel C
32	ITAC-C	I	Transversal current input (AC), channel C
33	VR-C	I	Reference input, channel C
34	IL-C	I	Longitudinal current input, channel C
37	ACP-C	O	Two wire output voltage (ACP), channel C
38	ACN-C	O	Two wire output voltage (ACN), channel C
35	DCP-C	O	Two wire output voltage (DCP), channel C
36	DCN-C	O	Two wire output voltage (DCN), channel C

PRELIMINARY

Table 2   Pin Definition and Functions (Continued)

Pin No.	Name	Type	Function
39	C1-C	I/O	Digital interface to AHV-SLIC, channel C
40	C2-C	O	Digital interface to AHV-SLIC, channel C
70	IT-D	I	Transversal current input (AC+DC), channel D
69	ITAC-D	I	Transversal current input (AC), channel D
68	VR-D	I	Reference input, channel D
67	IL-D	I	Longitudinal current input, channel D
64	ACP-D	O	Two wire output voltage (ACP), channel D
63	ACN-D	O	Two wire output voltage (ACN), channel D
66	DCP-D	O	Two wire output voltage (DCP), channel D
65	DCN-D	O	Two wire output voltage (DCN), channel D
62	C1-D	I/O	Digital interface to AHV-SLIC, channel D
61	C2-D	O	Digital interface to AHV-SLIC, channel D

PRELIMINARY

Table 2   Pin Definition and Functions (Continued)

Pin No.	Name	Type	Function

IO Pins[1]

Pin No.	Name	Type	Function
4	IO1-A	I/O	User-programmable I/O pin, channel A
5	IO2-A[2]	I/O	User-programmable I/O pin, channel A
6	I1-A	I	Fixed input pin, channel A
2	O1-A	O	Fixed output pin, channel A
17	IO1-B	I/O	User-programmable I/O pin, channel B
16	IO2-B[2]	I/O	User-programmable I/O pin, channel B
15	I1-B	I	Fixed input pin, channel B
19	O1-B	O	Fixed output pin, channel B
44	IO1-C	I/O	User-programmable I/O pin, channel C
45	IO2-C[2]	I/O	User-programmable I/O pin, channel C
46	I1-C	I	Fixed input pin, channel C
42	O1-C	O	Fixed output pin, channel C
57	IO1-D	I/O	User-programmable I/O pin, channel D
56	IO2-D[2]	I/O	User-programmable I/O pin, channel D
55	I1-D	I	Fixed input pin, channel D
59	O1-D	O	Fixed output pin, channel D

Miscellaneous Function Pins

Pin No.	Name	Type	Function
14	RREF	O	Test pin, do not connect
10	VA	I	Voltage sense A
9	VB	I	Voltage sense B
8	VBIM	I	Battery image sense input

Pins not Used

Pin No.	Name	Type	Function
7	N.C.	–	Not connected (not used)

[1] Unused fixed input pin should be terminatedd with pull up or pull down.
Unused programmable pins should be programmed to output.

[2] If the PEB3465 is used together with the AHV-SLICs PEB4164 or PEB4166 it is recommended to use the IO2-Pin to drive the C3-Pin of the SLIC.
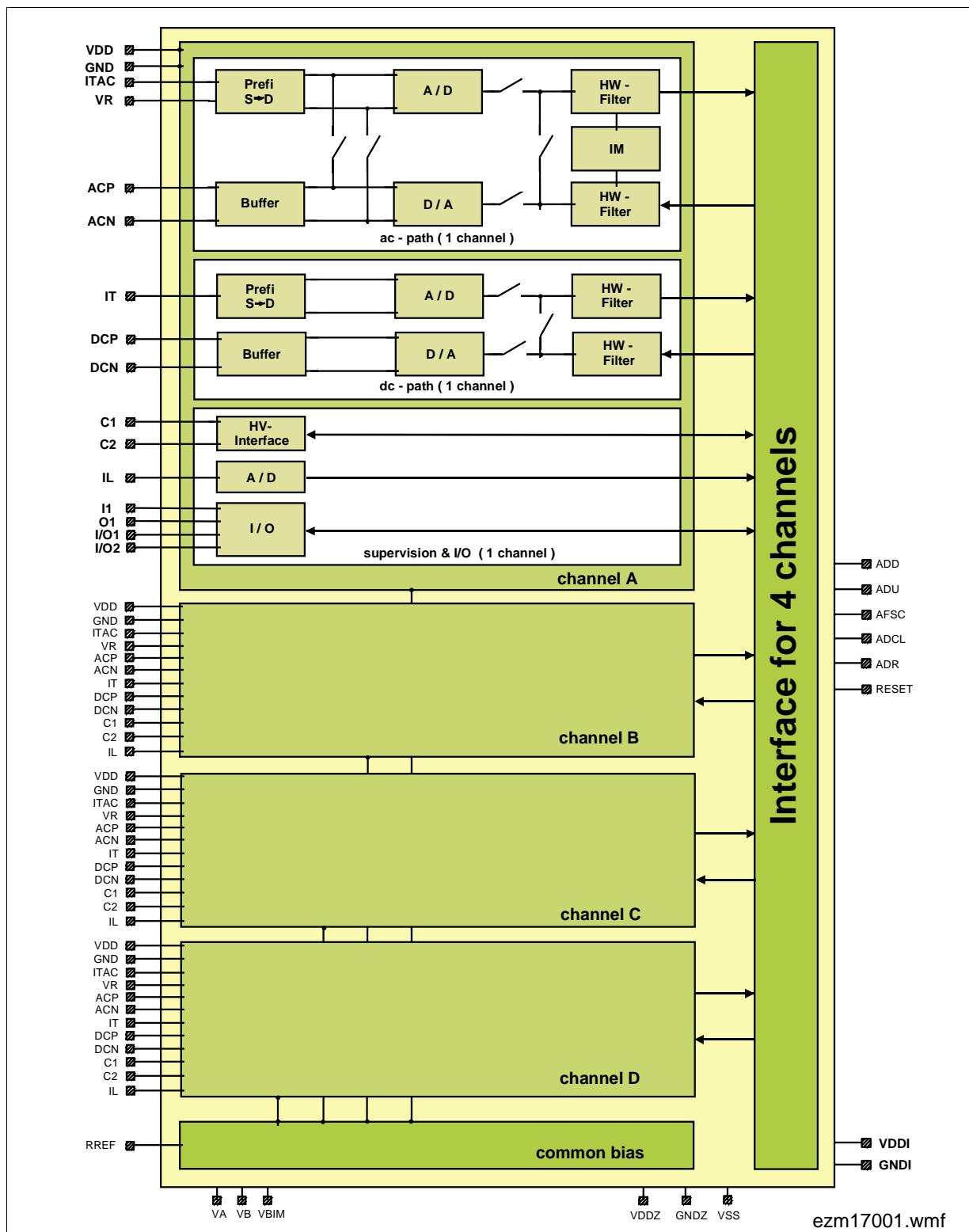
PRELIMINARY

1.2.2   Functional Block Diagram

Figure 3   Functional Block Diagram

PRELIMINARY

1.2.3 Application Diagrams

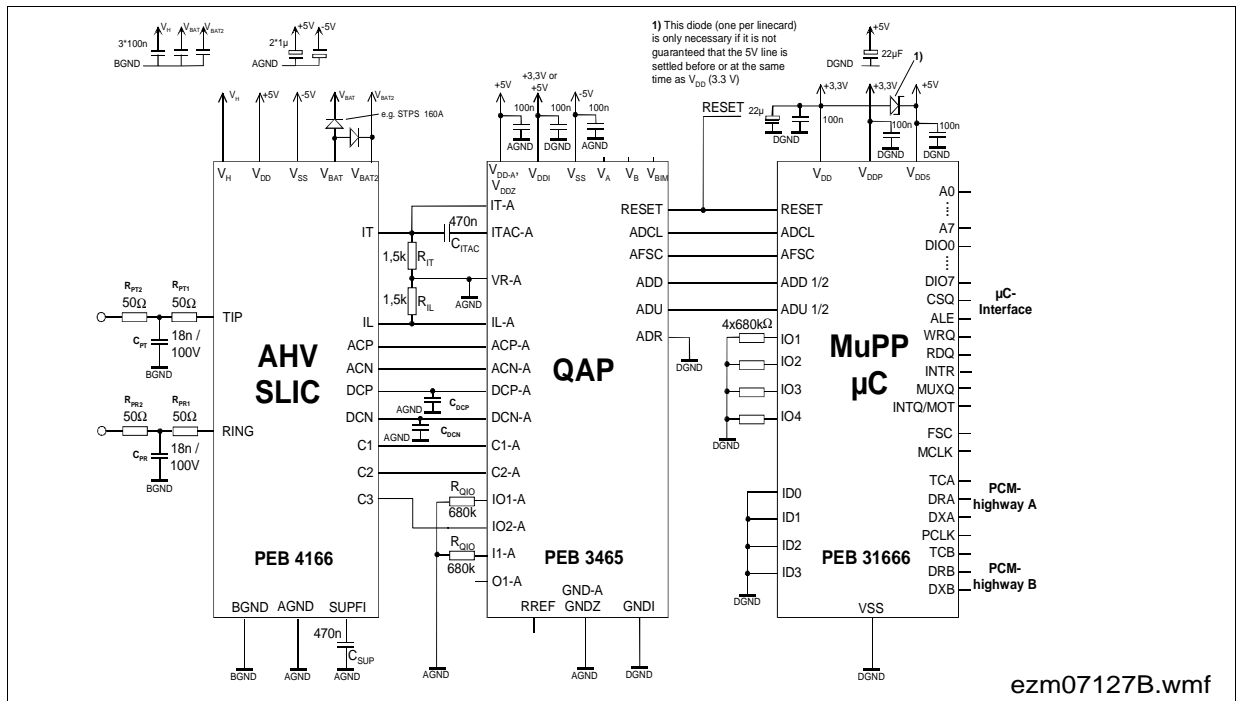**Figure 4   QAP with AHV-SLIC and MuPP µC (for one Subscriber)**

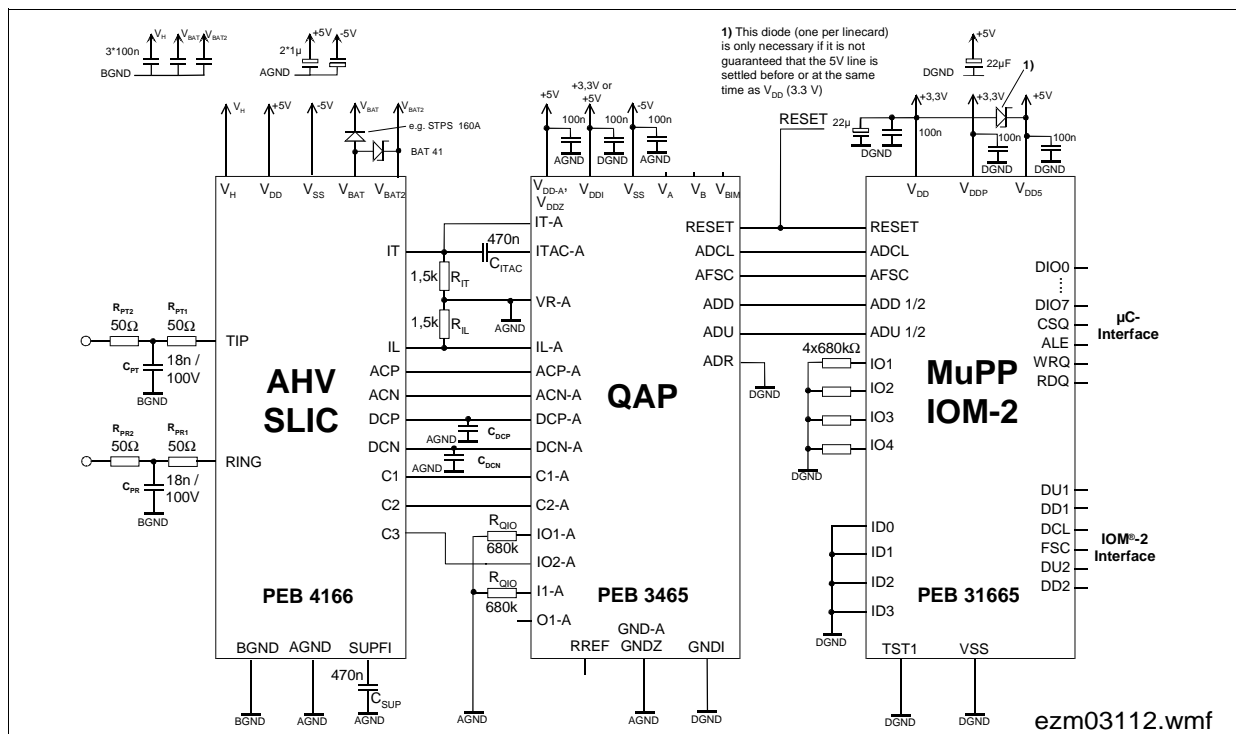**Figure 5   QAP with AHV-SLIC and MuPP IOM-2 (for one Subscriber)**

Table 3   List of Components in Application Circuits (Figure 4 & Figure 5)

Symbol	Value			Unit	Tolerance
	min.	typ.	max.		
R_{PT1} [1]	30	50		Ω	0,1 %
R_{PT2} [2]	0	50		Ω	0,1 %
R_{PR1}	30	50		Ω	0,1 %
R_{PR2}	0	50		Ω	0,1 %
R_{IT}		1,5		kΩ	1 %
R_{IL}		1,5		kΩ	1 %
R_{QIO}		680		kΩ	5 %
R_{MIO}		680		kΩ	5 %
C_{PT}	0,2	18	20	nF	10 %
C_{PR}	0,2	18	20	nF	10 %
C_{ITAC}		470		nF	10 %
$C_{DCP/N}$		100		nF	10 %
C_{SUP}		470		nF	10 %

[1] Absolut value not critical, but matching with RPR1 is important

[2] Absolut value not critical, but matching with RPR2 is important.

2 Functional Description

The Multichannel Signal Processing Subscriber Line Interface Codec Filter chip set, MuSLIC, is a logic continuation of the well established family of the Infineon Technologies PCM-Codec-Filter-ICs with the integration of all DC-feeding, supervision and meterpulse injection features on chip as well. Fabricated in advanced CMOS, BiCMOS and High Voltage technology SPT 170 the MuSLIC is tailored for very flexible solutions in analog/digital communication systems.

The chip set consists of the digital signal processor for 16 channels (MuPP, multichannel processor for POTS), the analog/digital and digital/analog converter for 4 channels (QAP, quad analog POTS) and the high voltage interface chip for 1 channel (AHV-SLIC, advanced high voltage subscriber line interface circuit).

The MuPP uses the benefits of a DSP not only for the voice channel but even for line feeding and supervision which leads to a very high flexibility without the need of external components. Based on an advanced digital filter concept, the PEB 31665/PEB 31666/PEB 31664 (MuPP) and the PEB 3465 (QAP) provide excellent transmission performance. The new filter concept leads to a maximum of independence between the different filter blocks. Each filter block can be seen as a one to one representative of the corresponding network element. Together with the software package MuSLICOS, filter optimizing to different applications can be done in a clear and straight forward procedure. The AC frequency behavior is mainly determined by the digital filters. Using the oversampling 1 bit $\Sigma\Delta$-AD/DA converters, linearity is only limited by second order parasitic effects.

The digital solution of line feeding offers free programmability of feeding current and voltage as well as very fast settling of the DC-operating point after transitions. A 0.3 Hz lowpass filter in the DC-loop is mainly responsible for the system stability.

Additionally Teletax generation and filtering is implemented as well as free programmable balanced ring generation with zero-crossing injection. Off hook detection with programmable thresholds is possible in all operating modes. To reduce overall power consumption of the linecard, the MuPP, the QAP and the AHV-SLICs provide a Power Down mode with off-hook detection (PDNR).

To program the MuSLIC or to get status information about the chip set or the system, two user interfaces are available: the IOM®-2 interface and a 8-bit-parallel simple microcontroller interface.

The AHV-SLICs PEB4165 and PEB4166 provide battery feeding between - 15 V and - 80 V and ringing injection with a differential ring voltage up to 85 Vrms. In order to achieve these high amplitudes, an auxiliary positive battery voltage is used during ringing. This voltage can also be applied to drive very long telephone lines.

The AHV-SLICs are designed for a voltage feeding - current sensing line interface concept and provide sensing of transversal and longitudinal currents on both wires. In

PRELIMINARY

Power Down mode the AHV-SLIC is switched off turning the line outputs to a high impedance state. Off-hook supervision is provided by activating a line current sensor.

2.1 Principles

2.1.1 Signal Flow Graph: AC

peb3465_0001_ac-work graph.emf
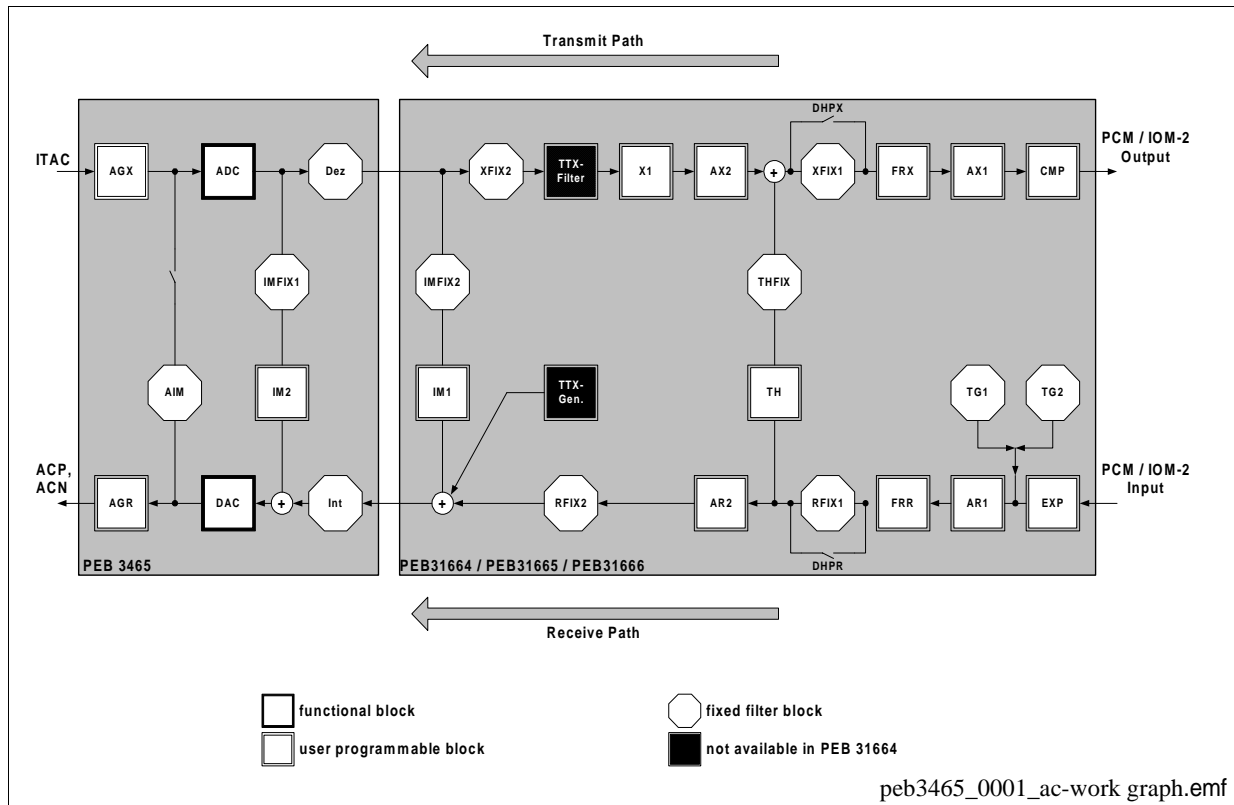
Figure 6 Signal Flow Graph: AC

Transmit Path

The analog input signal has to be connected to pin ITAC of the QAP by an external capacitor (470 nF) for AC/DC separation. After passing a programmable gain stage (AGX = 0, 3.5 or 9.5 dB) and a simple antialiasing prefilter the voice signal is converted to a 1-bit digital data stream in the $\Sigma\Delta$-converter. The first down sampling steps are done in fast running digital hardware filters on the QAP. This down sampled AC-signal (64 kHz sampling rate) is sent to the MuPP via the MuPP/QAP-Interface in the ADU-channel. The following signal processing is done in the DSP-machine of the MuPP. The benefits are the programmability of frequency and the gain behavior. At the end the fully processed signal is transferred to the PCM / IOM-2 Interface (A-law / µ-law / 16 bit linear) signal representation.

PRELIMINARY

### Receive Path

The digital input signal is received via the PCM / IOM-2 Interface of the MuPP. Expansion, PCM-lowpass-filtering, gain correction and frequency response correction are the next steps which are done by the DSP-machine. This 64 kHz AC signal is sent from the MuPP to the QAP via the MuPP/QAP-Interface in the ADD-channel. The up sampling interpolation steps are processed by fast hardware structures in the QAP to reduce the DSP-workload. The 1-bit data stream is then converted to an analog equivalent. A subsequent programmable gain stage (AGR = 0 or $-3,5$ dB) and smoothing filter provides the AC output signal at the Pins ACP and ACN of the QAP for direct connection to the AHV-SLIC.

Loops

There are two different loops implemented: The Impedance Matching (IM) loop which is divided into 3 separate loops to guarantee very high flexibility to various impedances, and the Transhybrid Balancing (TH) loop.

2.1.2   Signal Flow Graph: DC
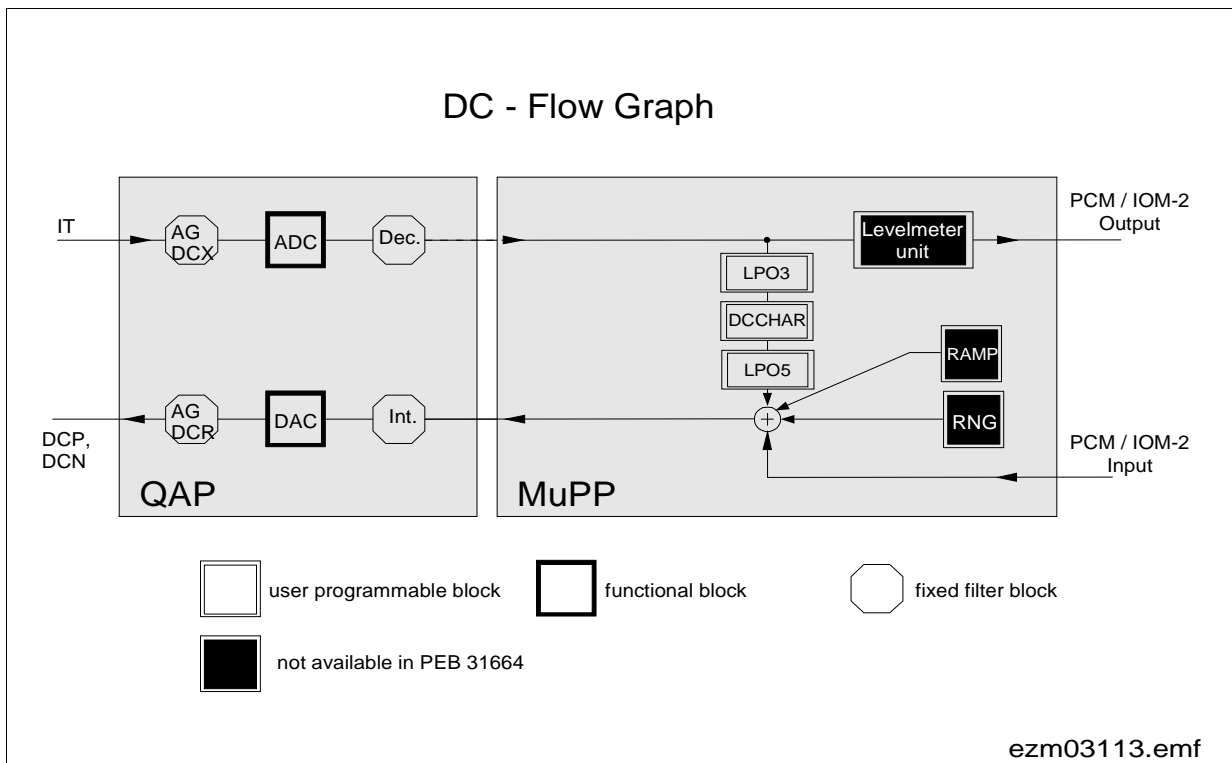
Figure 7   Signal Flow Graph: DC

PRELIMINARY

DC Characteristic

The incoming information (transmit direction) at pin IT (scaled transversal AC + DC-current, transferred to a voltage via an external 1.5 kΩ resistor at IT) passes first an antialiasing filter and is then converted to a 1-bit digital data stream in the $\Sigma\Delta$-converter. Down sampling is done in hardware filters of the QAP. This DC-information (2 kHz sampling rate) is then fed to the MuPP where it is first lowpass filtered (0.3 Hz corner frequency) for stability and noise reasons. The following DC-characteristic consists of three branches which represents different kinds of feeding behavior. In typical applications it acts as a programmable constant current source (R_{in} > 30 kΩ). If the desired value cannot be held feeding switches automatically and smoothly to the resistive branch (R_{in} programmable between 0 … 1.6 kΩ). The third branch is used for feeding long lines - the DC-characteristic switches to a constant voltage behavior. For superimposing voice as well as Teletax pulses the necessary drop at the line can be calculated and taken into account as well. The outgoing bit stream (2 kHz sampling rate), representing the DC-feeding value is then sent back to the QAP where a 1-bit $\Sigma\Delta$-converter and a following smoothing filter (using 2*100 nF external capacitor) establish the desired values at the Pins DCP and DCN, respectively. Depending on the operating mode (Active, Ringing, Active with Boosted Battery) a gain of 0 or 4 dB is inserted.

For test purposes it is possible to close a loop to test either the analog part or the digital part of the DC path.

Additional Features

The QAP provides three general purpose input Pins (VA, VB, VBIM) for measuring. Via the MuPP/QAP-Interface it is possible to select one of these inputs for the measurement. The DC-signal at the selected input is converted to digital using the same $\Sigma\Delta$-converter as for Ground Key information (IL, accuracy of $\pm$8%) and sent to the MuPP. The input range is between – 2.4 V … + 2.4 V. As a further selection it is also possible to measure the internal VDDZ-voltage of the QAP.This voltage is internal divided by 4 and can be measured by setting VDDIM.

3 Interfaces

3.1 MuPP/QAP Interface

The MuPP/QAP-Interface, the link between MuPP and QAP is a serial interface based on the 6 signals AFSC (analog frame sync), ADCL (analog data clock), ADU1/ADU2 (analog data upstream) and ADD1/ADD2 (analog data downstream). ADU1 and ADD1 are common to the first group of 8 time slots (channels) and ADU2 and ADD2 to the second 8 time slots (channels). AFSC and ADCL are common to both groups of time slots.
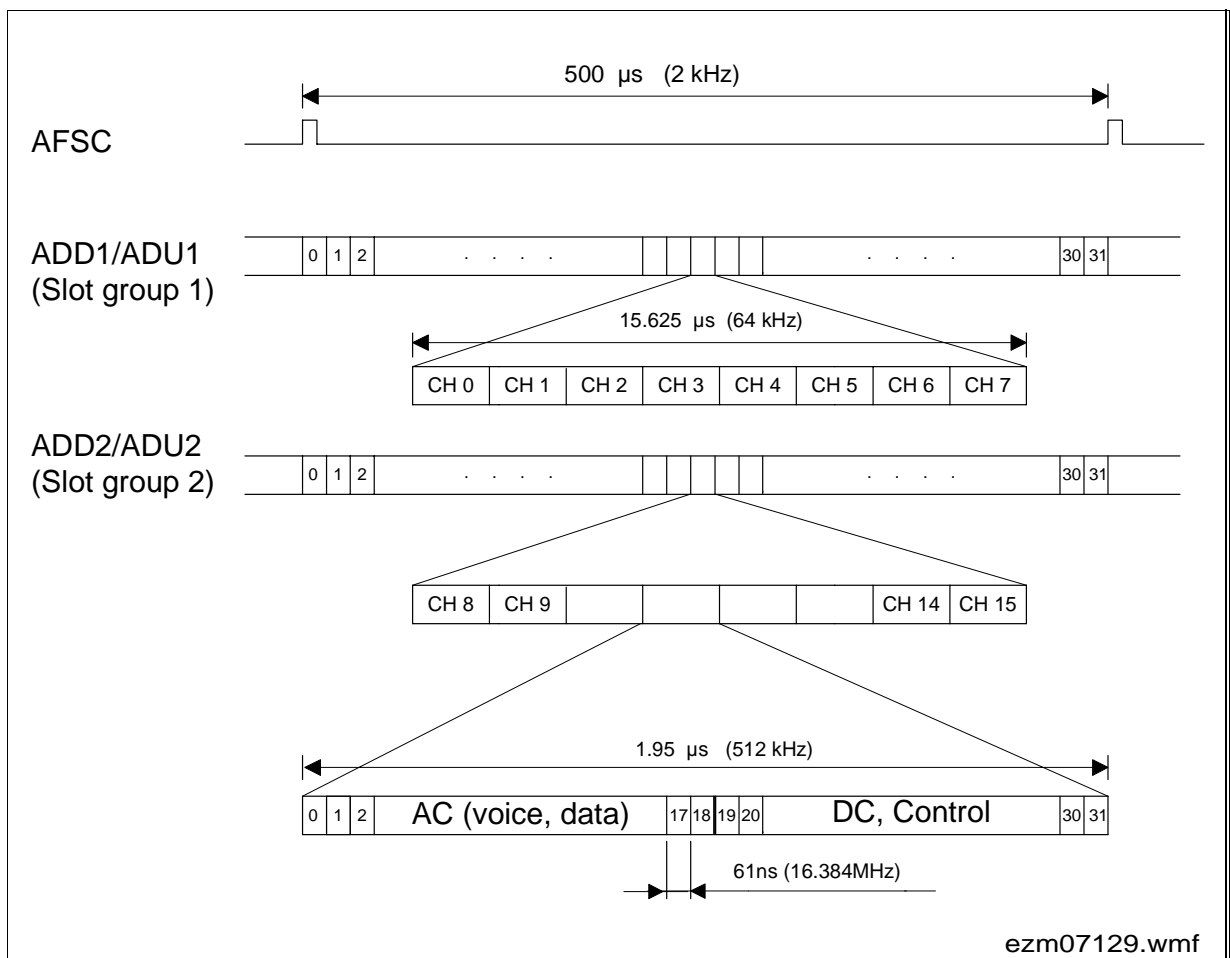

Figure 8   MuPP/QAP Interface: Frame, Bit Structure

3.2 QAP/AHV-SLIC Interface

Output Voltage AC (ACP, ACN)

The output voltage at the pins ACP and ACN represents the AC-information together with Teletax information at the receive path. The AC-information is received via the MuPP/QAP-Interface in the ADD channel. The 64 kHz bitstream is converted to analog, passes a programmable gain stage of 0 / – 3.5 dB (TTX is also affected) and is buffered to drive a load of R_L > 15 kΩ and C_L < 20 pF, which is the input impedance of the AHV-SLIC.

Output Voltage DC (DCP, DCN)

The output voltage at the pins DCP and DCN represents the DC-information together with the Ring Burst at the receive path. The DC-information is received via the MuPP/QAP-Interface in the ADD channel. The 2 kHz bitstream is converted to analog and buffered to drive external smoothing capacitors of 2*100 nF. The pins are directly connected to the AHV-SLIC.

Transversal Current Sense AC - Input (ITAC)

The pin ITAC is the input voltage pin for the AC transversal current information from the AHV-SLIC in the transmit path. AC/DC separation is done by an external highpass filter (ext. capacitor = 470 nF). The input resistance is larger than 20 kΩ. Current/voltage conversion is done via an external resistor of 1.5 kΩ (same for pin IT). The signal passes a programmable gain stage of 0, 3.5 or 9.5 dB, is converted to digital and sent to the MuPP via the MuPP/QAP-Interface in the ADU channel (64 kHz bitstream).

Transversal Current Sense DC - Input (IT)

The pin IT is the input voltage pin for the DC transversal current information from the AHV-SLIC in the transmit path. The input resistance is larger than 500 kΩ. Current/voltage conversion is done via an external resistor of 1.5 kΩ (same for pin ITAC). The voltage at pin IT is lowpass filtered and converted to digital. The bitstream (2 kHz) is sent to the MuPP via the MuPP/QAP-Interface for further signal processing.

Longitudinal Current Sense - Input (IL)

The scaled longitudinal current information transferred from the AHV-SLIC - the current/voltage conversion is done by an external resistor of 1.5 kΩ - is converted into digital and sent to the MuPP via the MuPP/QAP-Interface in the ADU channel.

Ternary Interface (C1, C2)

In order to set the AHV-SLICs to the different operating modes, the mode information of the board-contoller is passed through from the IOM-2-channel (PEB 31665) or μC-

PRELIMINARY

interface (PEB 31666, PEB 31664) via the MuPP/QAP-interface to the ternary AHV-SLIC interface pins C1 and C2.

PRELIMINARY

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
VDDA-VDDD referred to GNDA-GNDD		− 0.3	7	V	
VDDI referred to GNDI		− 0.3	7	V	
VSS referred to all GND pins		− 7	0.3	V	
GNDA-GNDD to GNDI		− 0.3	0.3	V	
VDDA-VDDD to VDDI		− 0.3	0.3	V	
Analog input and output voltages					
referred to VDD = 5 V; (VSS = − 5 V)		− 10.3	0.3	V	
referred to VSS = − 5 V; (VDD = 5 V)		− 0.3	10.3	V	
All digital input voltages					
referred to GNDI = 0 V; (VDDI = 5 V)		− 0.3	5.3	V	
referred to VDDI = 5 V; (GNDI = 0 V)		− 5.3	0.3	V	
DC input and output current at any input or output pin (free from latch-up)			100	mA	
Storage temperature	T_{STG}	− 65	125	°C	
Ambient temperature under bias	T_A	− 45	90	°C	
Power dissipation	P_D		1	W	

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.
Functional operation under these conditions is not implied.
Exposure to conditions beyond those indicated in the recommended operational conditions of this specification may effect device reliability.

PRELIMINARY

4.2 Operating Range

VDDA...VDDD, VDDZ = 5 V ± 5%; VDDI= 3.3 V ± 5%
VSS = - 5 V ± 10%; all GND's = 0 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
V_{DD} supply current						
Power down digital	$IDDD_{PD}$		7	10	mA	all channels PDown
Power down analog	$IDDA_{PD}$		10	13	mA	all channels PDown
Active digital	$IDDD_{Act.}$		23	30	mA	all channels active
Active analog	$IDDA_{Act.}$		60	70	mA	all channels active
V_{SS} supply current						
Power down	ISS_{PDown}		0.5	1	mA	all channels PDown
Active	ISS_{Act}		10	13	mA	all channels active
Power supply rejection-ratio	PSRR					ripple: 1 kHz, 80 mVrms
Receive VDD		45	60		dB	
Receive VSS		45	60		dB	
Transmit VDD		40	60		dB	
Transmit VSS		40	60		dB	
Power dissipation						
Power down	P_{PDown}		75	108	mW	all channels PDown
Active	P_{act1}		175		mW	1 channel active
Active	P_{act}		425	550	mW	all channels active

4.3 Electrical Parameters

Functionality and performance is guaranteed for $T_A = 0\,°C$ to 70 °C by production testing. Extended temperature range operation at $-40\,°C < T_A < 85\,°C$ is guaranteed by design, characterization and periodically sampling and testing production devices at the temperature extremes.

The target figures in this specification are based on the subscriber-line board requirements.

Unless otherwise noted, the transmission characteristics are guaranteed within the test conditions.

The 0 dBm0 definitions for receive and transmit are different.

A 0 dBm0 signal in transmit direction is equivalent to 604 mVrms.

A 0 dBm0 signal in receive direction is equivalent to 4365 mVrms.
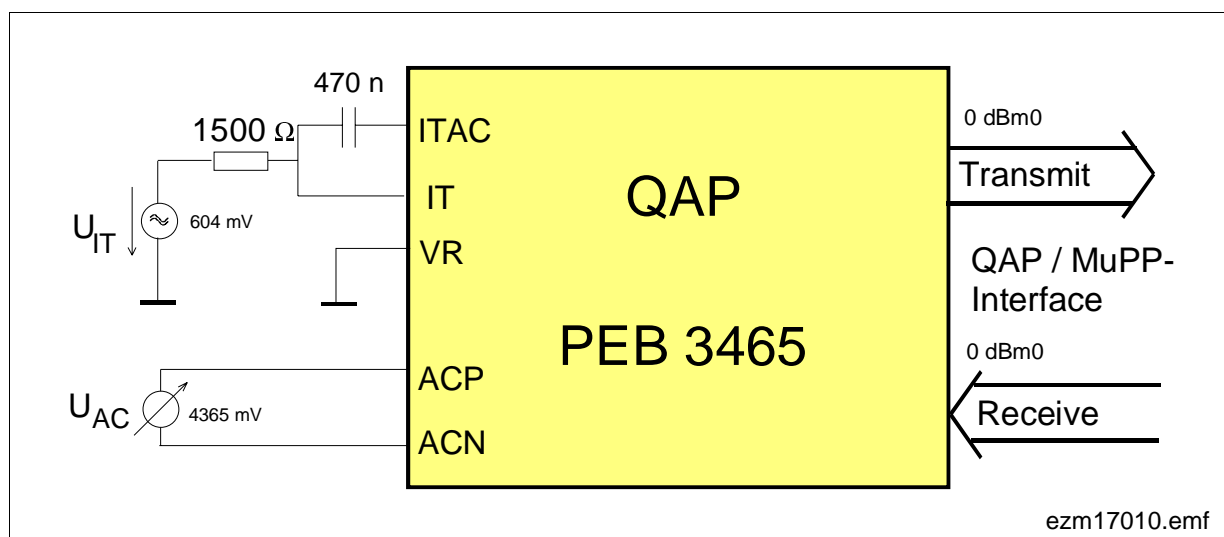
Figure 9   Transmission Characteristics

With $U_{IT} = 0\ dBm0|_{QAP} = -2.17\ dBm0|_{775mV} = 604\ mV$ for transmit

With $U_{AC} = 0\ dBm0|_{QAP} = 15.02\ dBm0|_{775mV} = 4365\ mV$ for receive
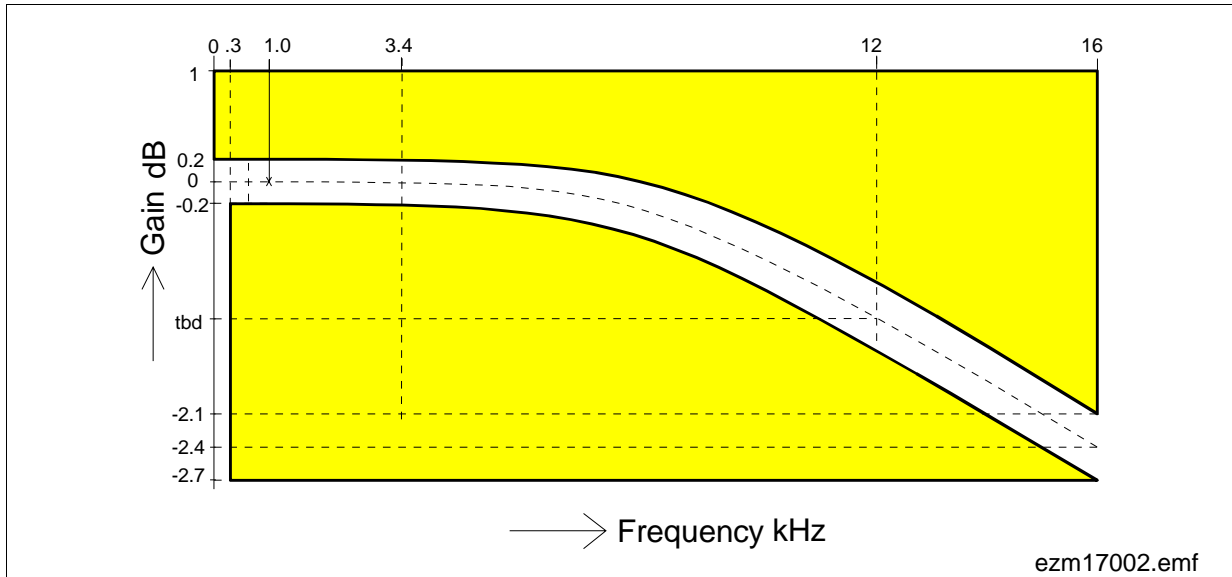
PRELIMINARY

4.3.1   Transmission Values

all VDD´s = 5V ± 5%; VSS = − 5V ± 10%; all GND´s = 0 V.

| Parameter	Symbol	Limit Values			Unit	Test Condition	Fig.
		min.	typ.	max.			
Absolute Gain (f = 300..3400 Hz) transmit (AG6dB = 0)	GX0	− 0.20	± 0.05	0.20	dB	f = 1 kHz	
receive (AG6dB = 0)	GR0	− 0.20	± 0.05	0.20	dB	f = 1 kHz	
transmit (AG6dB = 1)	GXG	− 0.25	± 0.05	0.25	dB	f = 1 kHz	
receive (AG6dB = 1)	GRG	− 0.25	± 0.05	0.25	dB	f = 1 kHz	
transmit (AG6dB = 1, USGAIN = 1)	GRG	− 0.3	± 0.05	0.3	dB	f = 1 kHz	
transmit (TTX-signals)	GTTX-X	− 2.1	− 2.4	− 2.7	dB	f = 16 kHz	**10**
receive (TTX-signals)	GTTX-R	− 4.0	− 3.7	− 3.4	dB	f = 16 kHz	**11**
Absolute Gain Variation with temp. − 40° to 85°				± 0.1	dB		
Total Harmonic distortion							
transmit	THDT		− 56	− 48	dB	at − 17 dBm0; f = 1 kHz; 2nd, 3rd order	
receive	THDR		− 56	− 48	dB	at − 17 dBm0; f = kHz; 2nd, 3rd order	
Idle channel noise							
transmit	NTP		− 96	− 91	dBm0p	psophometric, VIN = 0 V	
	NTTXTP		− 99	− 88	dBm0p	psophometric, VIN = 16 kHz, − 1 dBm0	
receive	NRP		− 100	− 95	dBm0p	psophometric, code +0	
	NTTXRP		− 96	− 90	dBm0p	psophometric, VIN = 16 kHz, − 1 dBm0	
Crosstalk; any combination of direction and channel	CT		− 100		dB	at 0 dBm0, f = 1 kHz; guaranteed by design	

PRELIMINARY

Frequency Response

1. Transmit: reference frequency 1 kHz, signal level – 17 dBm0:

Figure 10   Frequency Response Transmit

2. Receive: reference frequency 1 kHz, signal level – 17 dBm0:
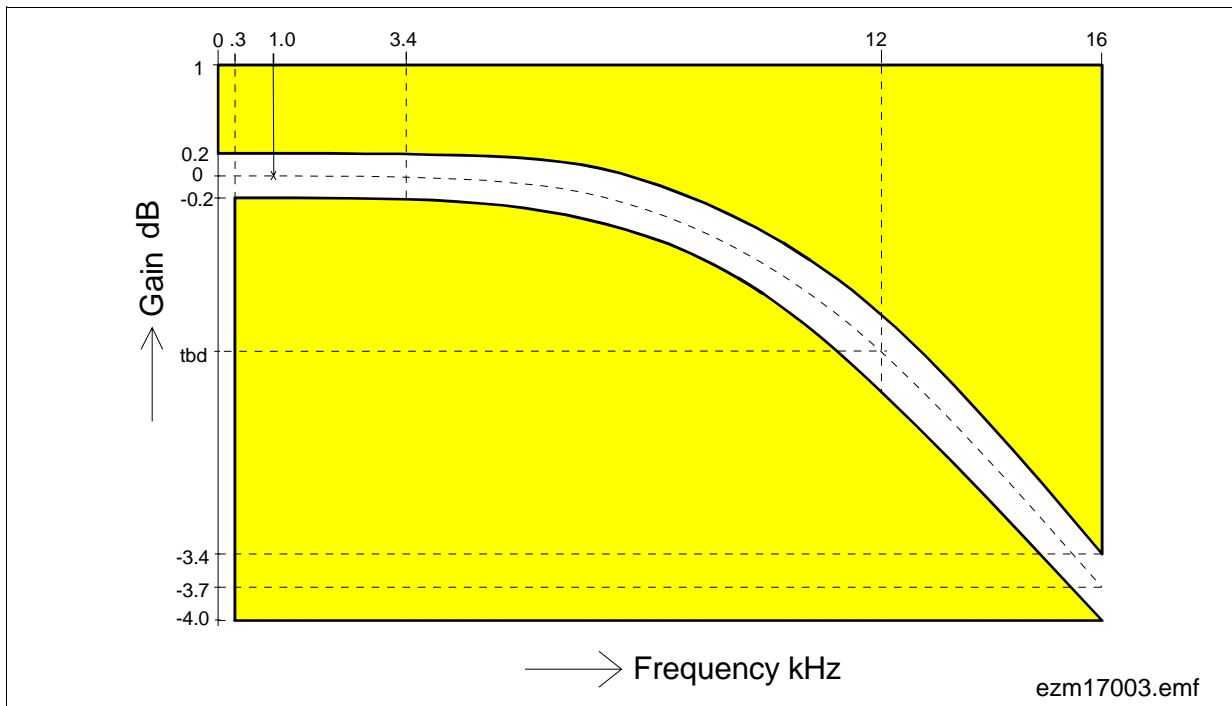
Figure 11   Frequency Response Receive

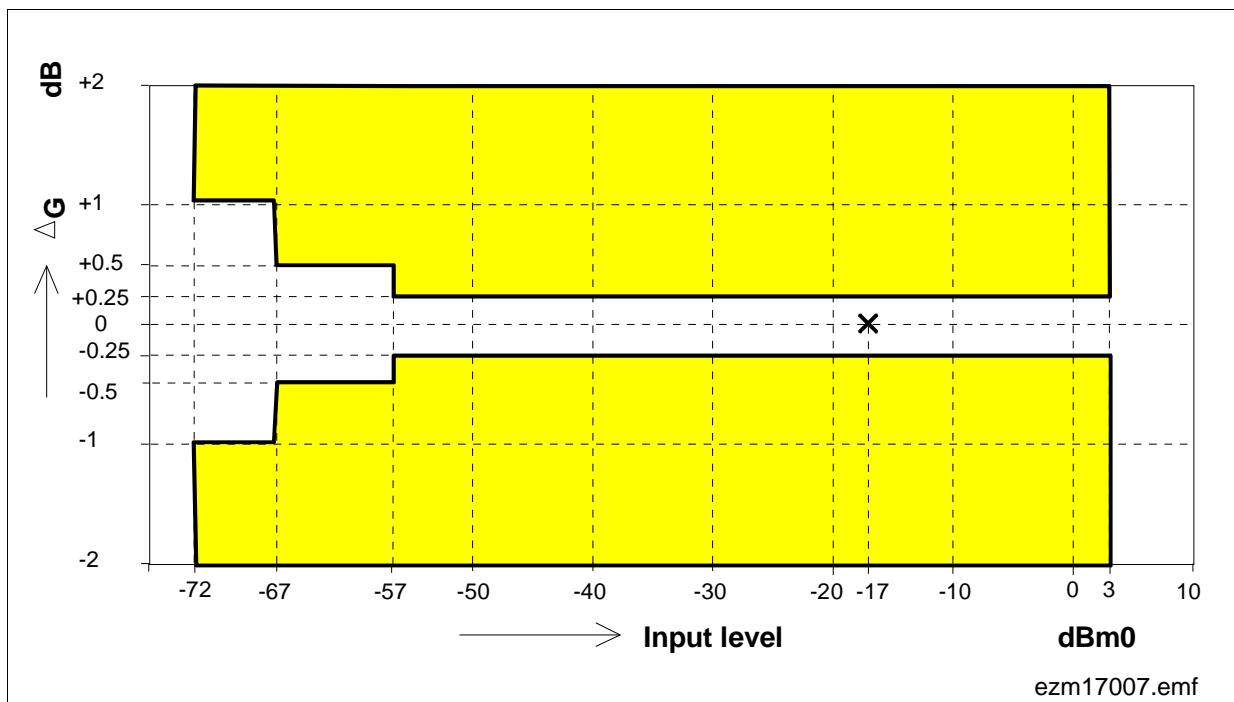**PRELIMINARY**

3. Out-of-Band Signals at Analog Output (Receive)

With a 0 dBm0 sine wave with frequency f (300 Hz to 3.4 kHz) applied to the digital input, the level of any resulting out-of-band signal at the analog output will stay at least 45 dB below a 0 dBm0, 1 kHz sine wave reference signal at the analog output.

Gain Tracking

The gain deviations stay within the limits in the figure below.

Transmit and Receive:
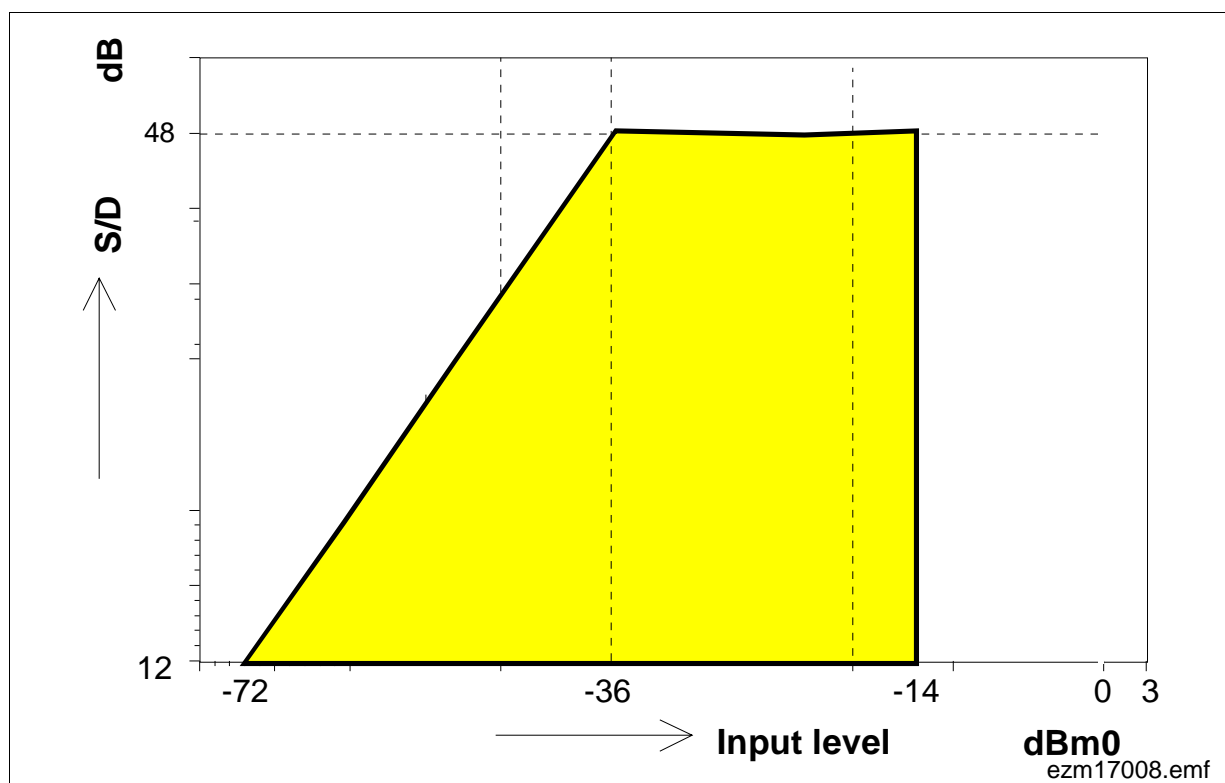measured with sine wave f = 1004 Hz; reference level = – 17 dBm0

Figure 12   Gain Tracking (Transmit and Receive)

PRELIMINARY

Total Distortion

The signal to distortion ratio exceeds the limits in the following figures:

1. Receive: measured with sine wave f = 1004 Hz.

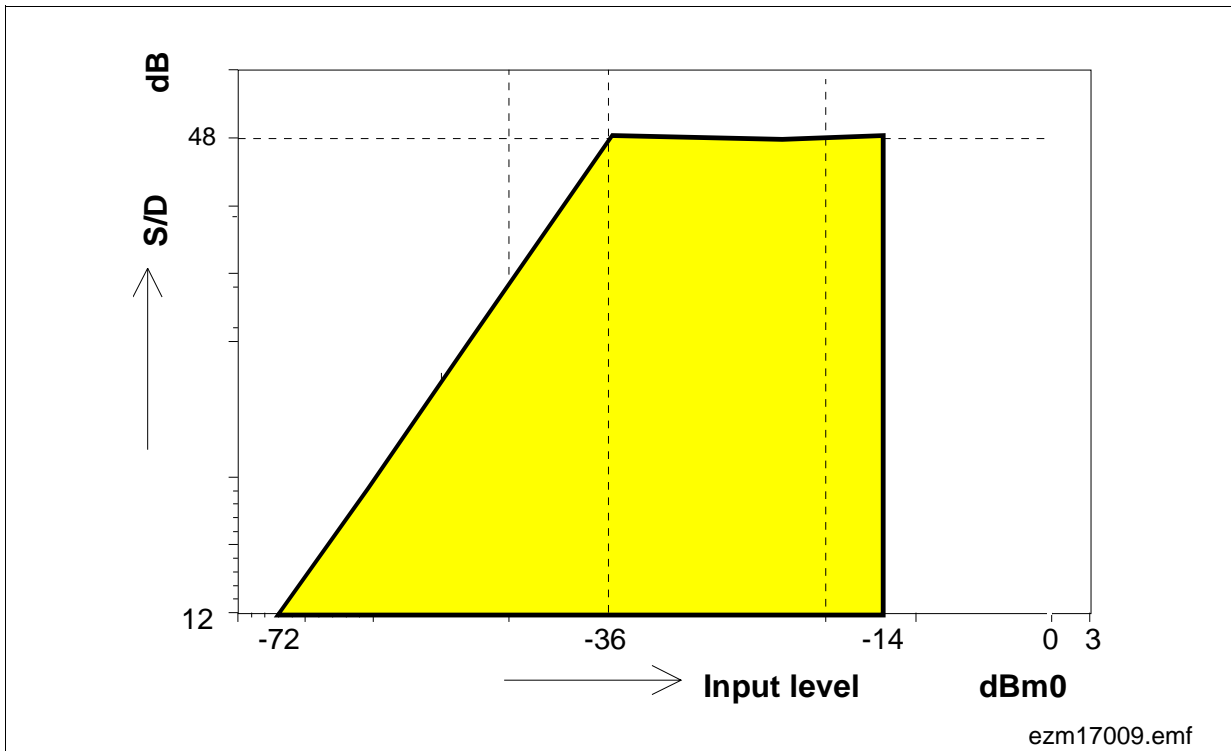
Figure 13   Total Distortion Receive

Table 4   Total Distortion Receive

Parameter	Symbol	Limit Values			Unit	Test Condition	Fig.
		min.	typ.	max.			
Signal to Distortion	SD_R	48	60		dB	Signal S = – 14 dBm0	13

PRELIMINARY

2. Transmit: measured with sine wave f = 1004 Hz

Figure 14   Total Distortion Transmit

Table 5   Total Distortion Receive

Parameter	Symbol	Limit Values			Unit	Test Condition	Fig.
		min.	typ.	max.			
Signal to distortion	SD_T	48	60		dB	Signal S = – 14 dBm0	**14**

PRELIMINARY

4.3.2　DC Characteristics

I/O-Pins

all V_{DD}'s = 5 V $\pm$ 5%; V_{SS} = $-$ 5 V $\pm$ 10%; all GND's = 0 V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min	max.		
Digital input pins ADCL, AFSC, ADD, ADR, RESET				V	
Low - input voltage	V_{IL}	$-$ 0.3	0.8	V	
High - input voltage	V_{IH}	2.0	VDD +0,3	V	
Input leakage current	I_{IL}	$-$ 1	1	µA	$-$ 0.3 <= V_{in} <= V_{DD}
Spike rejection for RESET	t_{rej}	50	200	ns	
digital output pin ADU					
Low-output voltage	V_{OL}		0.45	V	I_O = $-$ 2 mA
High-output voltage	V_{OH}	2.4		V	I_O = 2 mA
for I/O1 and O1:					
Low-output voltage	V_{OL}		0.6	V	I_O = $-$ 50 mA
High-output voltage	V_{OH}	3.5		V	I_O = 2 mA
for I/O2:					
Low-output voltage	V_{OL}		0.5	V	I_O = $-$ 2 mA
High-output voltage	V_{OH}	3.5		V	I_O = 2 mA

DC-Feeding

Figure 15   DC-Feeding Test Circuit

With U_{IT} = 0 dBm0DC$|_{QAP}$ = 1.1822 V for transmit

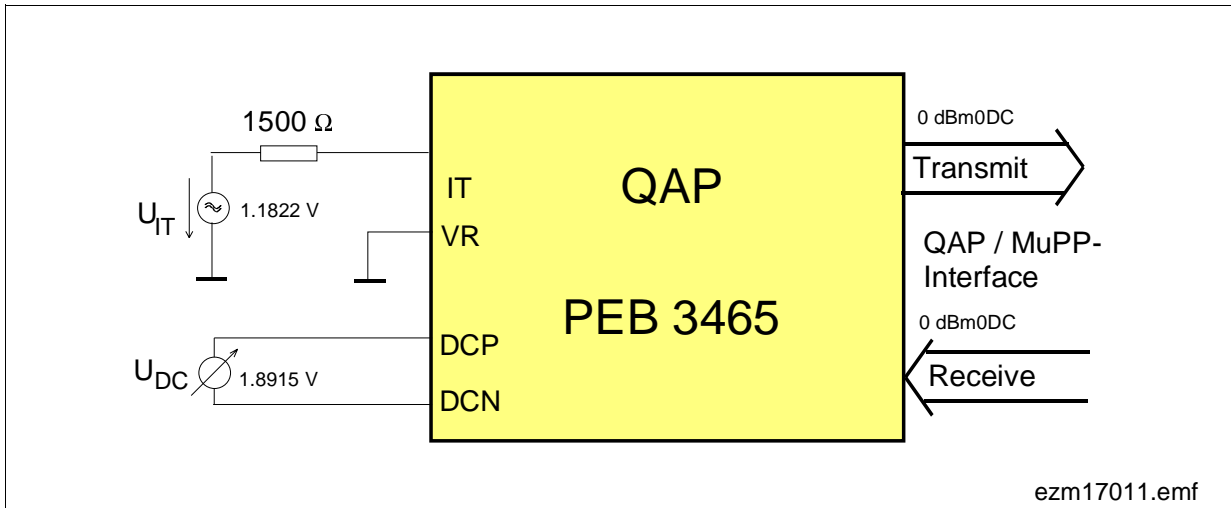With U_{DC} = 0 dBm0DC$|_{QAP}$ = 1.8915 V for receive

PRELIMINARY

all V_{DD}'s = 5 V $\pm$ 5%; V_{SS} = $-$ 5 V $\pm$ 10%; all GND's = 0 V

| Parameter	Symbol	Limit Values			Unit	Test Condition	Fig.
		min.	typ.	max.			
"Line Current" Measurement (IT):							
Transmit	$V_{IT\ offset}$[1]	$-$ 50		50	mV		**16**
	$V_{IT\ gain}$	$-$ 0.5	0	0.5	dB	f < 50 Hz	**16**
		$-$ 1.2	$-$ 0.65	$-$ 0.1	dB	f = 300 Hz	
	$V_{IT\ THD-}$	40	50		dB	f = 300 Hz	
Additional gain variation with temperature $-$ 40° to + 85°				$\pm$ 0.1	dB		
"Line Voltage" Feeding (DCP, DCN):							
Receive	$V_{DC\ offset}$	$-$ 25		25	mV		**17**
	$V_{DC\ gain}$	$-$ 0.5	0	0.5	dB	f < 50 Hz, dc_dispofi = 1	**17**
		$-$ 1.1	$-$ 0.55	0.0	dB	f = 300 Hz, dc_dispofi = 1	
	$V_{DC\ THD}$	40	50		dB	f=300 Hz, dc_dispofi = 1	
Receive Boosted	$V_{DC\ Boost}$	3.5	4.1	4.7	dB	dc_dacgain = 1	
Additional gain variation with temperature $-$ 40° to + 85°				$\pm$ 0.1	dB		

[1] This offset can be compensated in the system by performing an offset measurement as described in the Application note "Line and Board Testing with MuSLIC".

PRELIMINARY

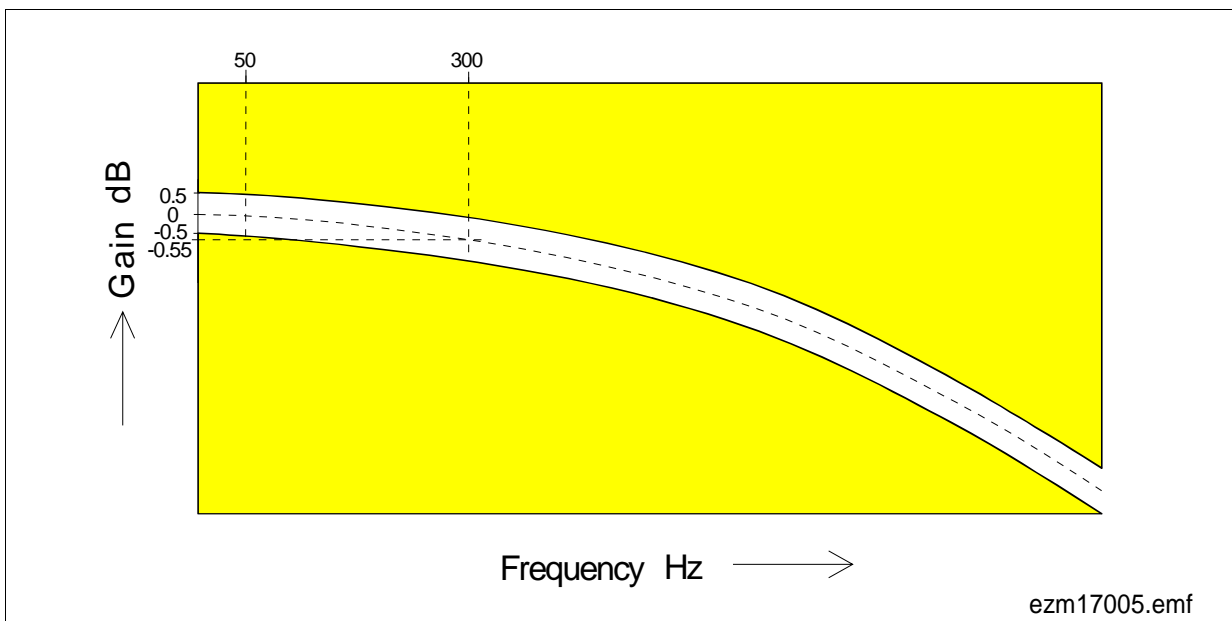## DC-Frequency Response

1. Transmit: reference frequency 50 Hz, signal level 0dBm0$_{DC}$
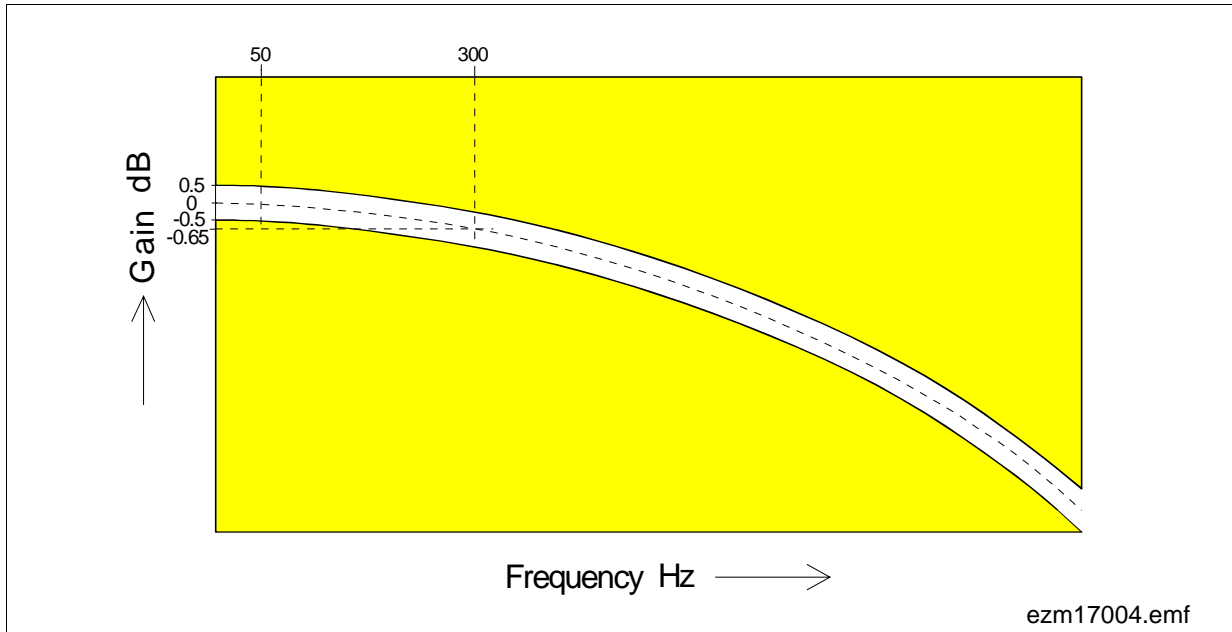
Figure 16   Frequency Response Transmit

2. Receive: reference frequency 50 Hz, signal level 0dBm0$_{DC}$

Figure 17   Frequency Response Receive

PRELIMINARY

## AHV-SLIC Interface & Supervision Functions

all V_{DD}'s = 5 V $\pm$ 5%; V_{SS} = $-$ 5 V $\pm$ 10%; all GND's = 0 V

Parameter	Symbol	Limit Values			Unit	Test Condition/Result	Fig.
		min.	typ.	max.			
Output voltage: AHV-SLIC-Interface C1, C2							
High level	V_{OHHV}	3.65			V	I_{out} < 10 µA	
Mid level	V_{OMHV}	2.2		2.8	V	I_{out} < 10 µA	
Low level	V_{OLHV}			1.35	V	I_{out} < 10 µA	
Current drained from pin C1 in all 3 states	I_{OTLo} I_{OTHi}	130		30	µA µA	tempa = 0 [1] tempa = 1	
Longitudinal Current Input (IL)	$V_{IL\ gain}$	$-$ 1.2	$-$ 0.5	0.2	dB	f < 50 Hz; V_{in} = 0dBm0$_{DC}$	**18**
		$-$ 1.8	$-$ 1.1	$-$ 0.4	dB	f = 300Hz	**18**
Auxiliary Inputs (V$_A$, V$_B$, V$_{BIM}$)	$V_{x\ gain}$	$-$ 1.2	$-$ 0.5	0.2	dB	f < 50Hz; V_{in} = 0dBm0$_{DC}$	**18**
		$-$ 1.8	$-$ 1.1	$-$ 0.4	dB	f = 300Hz	**18**
V_{DDIM}	V_{DDIM}	0.22* VDD	0.24* VDD	0.26* VDD	V	internal connected to VDDZ/4	**18**

[1] TEMPA is reported via the MuPP/QAP-Interface to the MuPP

PRELIMINARY
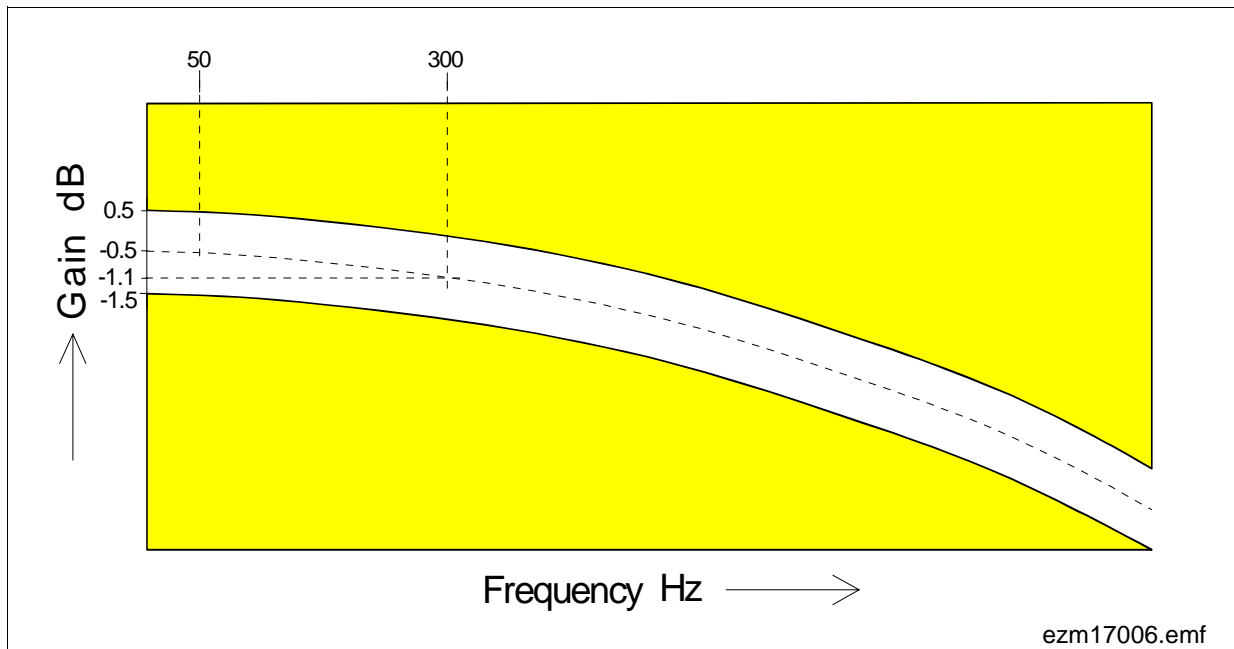
Figure 18   Frequency Response: Longitudinal Current Input & Auxiliary Inputs

4.3.3 MuPP-Interface Timing Characteristics
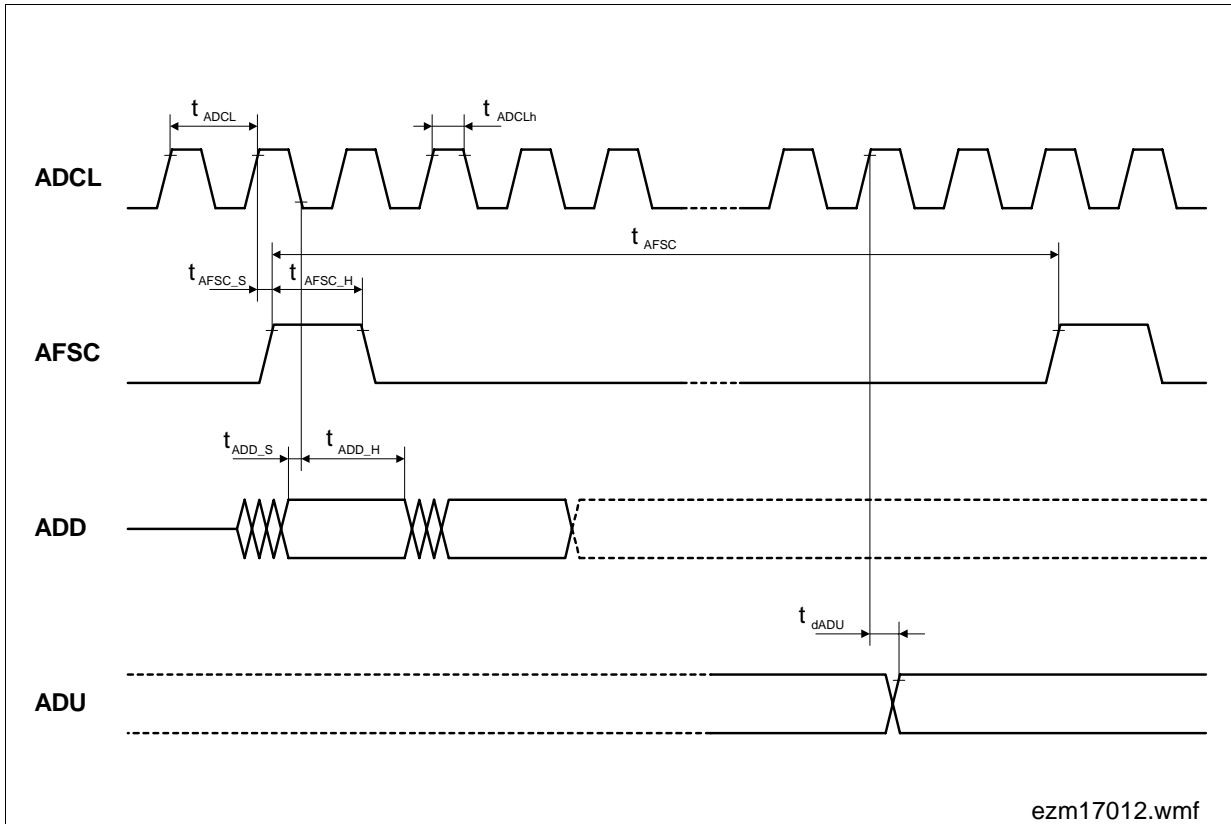
Figure 19   MuPP-Interface Timing Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period ADCL	t_{ADCL}		1/16384		ms
ADCL duty cycle	t_{ADCLh}	40	50	60	%
Period AFSC	t_{AFSC}		500		µs
AFSC setup	t_{AFSC_S}	10			ns
AFSC hold	t_{AFSC_H}	10			ns
ADD setup time	$t_{ADD\,S}$	10			ns
ADD hold time	$t_{ADD\,H}$	10			ns
ADU delay	t_{dADU}		15	30	ns

PRELIMINARY

5 Package Outlines

P-MQFP-80-1
(Plastic Metric Quad Flat Package)

0.25 min
2 +0.1 -0.05
2.45 max
H
0.15 +0.08 -0.02
7° max
0.65
0.3 ±0.08
0.88 ±0.15
C
☐ 0.1
12.35
⊕ 0.12 Ⓜ A-B D C 80x
17.2
☐ 0.2 A-B D 80x
14 1)
☐ 0.2 A-B D H 4x
D
A
B
14 1)
17.2
80
1
Index Marking
0.6x45°

1) Does not include plastic or metal protrusions of 0.25 max per side
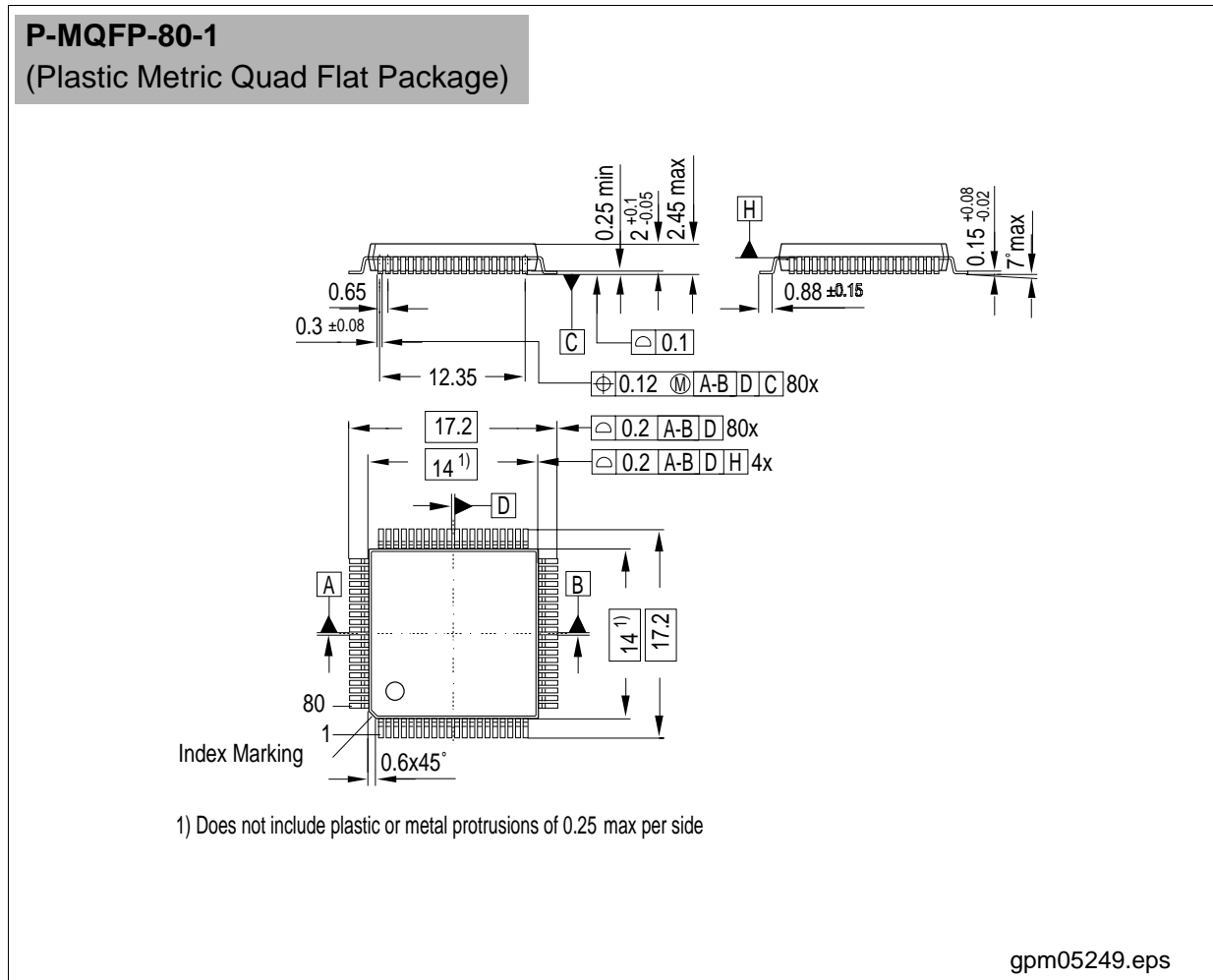
gpm05249.eps

Figure 20   Package Outline: PEB 3465 (QAP)

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our
data book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

PRELIMINARY

6 Glossary

ACT	Active Mode
ADC	Analog Digital Converter
AGR	Attenuation Receive
AGX	Attenuation Transmit
AHV-SLIC	Advanced High Voltage Subscriber Line Interface Circuit
BB	Boosted Battery
BiCMOS	Bipolar Complementary Metal Oxid Semiconductor
C1, 2	Digital Interface between QAP and AHV-SLIC
CMP	Compander
CODEC	Coder Decoder
DAC	Digital Analog Converter
DCCHAR	DC Characteristic block
DCL	Data Clock
DD	Data Downstream
DSP	Digital Signal Processor
EXP	Expander
FRR	Frequency Response Receive Filter
FRX	Frequency Response Transmit Filter
FSC	Frame Sync.
I1	Fixed Input Pin
IL	Longitudinal Current Input
IO	User Programmable I/O Pin
ISDN	Integrated Service Digital Network
IT	Transversal Current Input (for AC and DC)
ITAC	Transversal Current Input (for AC)
MuPP	Multi Channel Processor for POTS
MuSLIC	Multi Channel Subscriber Line Interface Circuit
MuSLICOS	MuSLIC Oriented Software
O1	Fixed Output Pin

PRELIMINARY

PCM	Pulse Code Modulation
POTS	Plain Old Telephone Service
PREFI	Antialiasing Pre Filter
QAP	Quad Analog POTS
RNG	Ring Generator
SLIC	Subscriber Line Interface Circuit
TST1	Test Pin
TH	Transhybrid Balancing
THFIX	Transhybrid Balancing Filter (fixed)
TTX	Teletax
TTXGEN	Teletax Generator
VBIM	Battery Image Input

Infineon goes for Business Excellence

"Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
Better operating results and business excellence mean less idleness and wastefulness for all of us, more professional success, more accurate information, a better overview and, thereby, less frustration and more satisfaction."

Dr. Ulrich Schumacher