IRHQ7110

PD-93785D

Radiation Hardened Power MOSFET
Surface Mount (LCC-28)
100V, 3.0A, Quad N-channel, Rad Hard HEXFET™ Technology

Features

- Single event effect (SEE) hardened
- Low total gate charge
- Simple drive requirements
- Hermetically sealed
- Surface mount
- Light weight
- ESD rating: Class 1A per MIL-STD-750, Method 1020

Product Summary

- **BV_{DSS}:** 100V
- **I_D :** 3.0A
- **$R_{DS(on),max}$:** 0.6Ω (100 krad(Si))
- **$Q_{G,max}$:** 11nC

LCC-28

Potential Applications

- DC-DC converter
- Motor drives

Product Validation

Qualified according to MIL-PRF-19500 for space applications

Description

IR HiRel rad hard HEXFET technology provides high performance power MOSFETs for space applications. This technology has over a decade of proven performance and reliability in satellite applications. These devices have been characterized for both Total Dose and Single Event Effects (SEE). The combination of low $R_{DS(on)}$ and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well-established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

Ordering Information

Table 1 Ordering options

Part number	Package	Screening Level	TID Level
IRHQ7110	LCC-28	COTS	100 krad(Si)
IRHQ7110SCS	LCC-28	S-Level	100 krad(Si)
IRHQ3110	LCC-28	COTS	300 krad(Si)
IRHQ3110SCS	LCC-28	S-Level	300 krad(Si)
IRHQ4110	LCC-28	COTS	500 krad(Si)
IRHQ4110SCS	LCC-28	S-Level	500 krad(Si)

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1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings (Pre-Irradiation)

Symbol	Parameter	Value	Unit
I_{D1} @ V_{GS} = 12V, T_C = 25°C	Continuous Drain Current	3.0	A
I_{D2} @ V_{GS} = 12V, T_C = 100°C	Continuous Drain Current	1.9	A
I_{DM} @ T_C = 25°C	Pulsed Drain Current [1]	12	A
P_D @ T_C = 25°C	Maximum Power Dissipation	12	W
	Linear Derating Factor	0.01	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy [2]	85	mJ
I_{AR}	Avalanche Current [1]	3.0	A
E_{AR}	Repetitive Avalanche Energy [1]	1.2	mJ
dv/dt	Peak Diode Reverse Recovery [3]	3.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Lead Temperature	300 (for 5s)	
	Weight	0.89 (Typical)	g

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.
[2] V_{DD} = 25V, starting T_J = 25°C, L = 18.7mH, Peak I_L = 3.0A, V_{GS} = 12V
[3] $I_{SD} \leq 3.0A$, di/dt ≤ 165A/µs, $V_{DD} \leq 100V$, $T_J \leq 150°C$

2 Device Characteristics

2.1 Electrical Characteristics (Pre-Irradiation)

Table 3 Static and Dynamic Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.6	Ω	V_{GS} = 12V, I_{D2} = 1.9A [1]
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 1mA
Gfs	Forward Transconductance	1.4	—	—	S	V_{DS} = 15V, I_{D2} = 1.9A [1]
I_{DSS}	Zero Gate Voltage Drain Current	—	—	25	µA	V_{DS} = 80V, V_{GS} = 0V
		—	—	250		V_{DS} = 80V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_G	Total Gate Charge	—	—	11	nC	I_{D1} = 3.0A V_{DS} = 50V V_{GS} = 12V
Q_{GS}	Gate-to-Source Charge	—	—	4.0		
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	5.5		
$t_{d(on)}$	Turn-On Delay Time	—	—	20	ns	I_{D1} = 3.0A ** V_{DD} = 50V R_G = 7.5Ω V_{GS} = 12V
t_r	Rise Time	—	—	25		
$t_{d(off)}$	Turn-Off Delay Time	—	—	40		
t_f	Fall Time	—	—	40		
$L_s + L_D$	Total Inductance	—	6.1	—	nH	Measured from the center of Drain pad to Source pad
C_{iss}	Input Capacitance	—	270	—	pF	V_{GS} = 0V V_{DS} = 25V f = 1.0MHz
C_{oss}	Output Capacitance	—	110	—		
C_{rss}	Reverse Transfer Capacitance	—	23	—		

** Switching speed maximum limits are based on manufacturing test equipment and capability.

[1] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

2.2 Source-Drain Diode Ratings and Characteristics (Pre-Irradiation)

Table 4 Source-Drain Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	3.0	A	
I_{SM}	Pulsed Source Current (Body Diode) [1]	—	—	12	A	
V_{SD}	Diode Forward Voltage	—	—	1.2	V	$T_J = 25°C$, $I_S = 3.0A$, $V_{GS} = 0V$ [2]
t_{rr}	Reverse Recovery Time	—	—	173	ns	$T_J = 25°C$, $I_F = 3.0A$, $V_{DD} \leq 25V$ di/dt = 100A/µs [2]
Q_{rr}	Reverse Recovery Charge	—	—	863	nC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

2.3 Thermal Characteristics

Table 5 Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-Case	—	—	10.4	°C/W

2.4 Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 3 and 4) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

2.4.1 Electrical Characteristics — Post Total Dose Irradiation

Table 6 Electrical Characteristics @ $T_J = 25°C$, Post Total Dose Irradiation [3, 4]

Symbol	Parameter	100 krad (Si) [5]		Up to 500 krad (Si) [6]		Unit	Test Conditions
		Min.	Max.	Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	100	—	V	$V_{GS} = 0V$, $I_D = 1.0mA$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.0	2.0	4.0	V	$V_{DS} = V_{GS}$, $I_D = 1.0mA$
I_{GSS}	Gate-to-Source Leakage Forward	—	100	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Leakage Reverse	—	-100	—	-100		$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	—	10	—	10	µA	$V_{DS} = 80V$, $V_{GS} = 0V$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (TO-3) [6]	—	0.556	—	0.706	Ω	$V_{GS} = 12V$, $I_{D2} = 1.9$ A
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance (LCC-28) [6]	—	0.6	—	0.75	Ω	$V_{GS} = 12V$, $I_{D2} = 1.9A$
V_{SD}	Diode Forward Voltage	—	1.2	—	1.2	V	$V_{GS} = 0V$, $I_F = 3.0A$

[1] Repetitive Rating; Pulse width limited by maximum junction temperature.
[2] Pulse width ≤ 300 µs; Duty Cycle ≤ 2%
[3] Total Dose Irradiation with V_{GS} Bias. $V_{GS} = 12V$ applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.
[4] Total Dose Irradiation with V_{DS} Bias. $V_{DS} = 80V$ applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, Method 1019, condition A.
[5] Part numbers IRHQ7110
[6] Part numbers IRHQ3110 and IRHQ4110

2.4.2 Single Event Effects — Safe Operating Area

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. 1 and Table 7.

Table 7 Typical Single Event Effects Safe Operating Area

Ion	LET (MeV·cm²/mg)	Energy (MeV)	Range (µm)	V_{DS} (V)				
				V_{GS} = 0V	V_{GS} = -5V	V_{GS} = -10V	V_{GS} = -15V	V_{GS} = -20V
Cu	28	285	43	100	100	100	80	60
Br	36.8	305	39	100	90	70	50	—
I	59.8	343	32.6	50	40	35	—	—

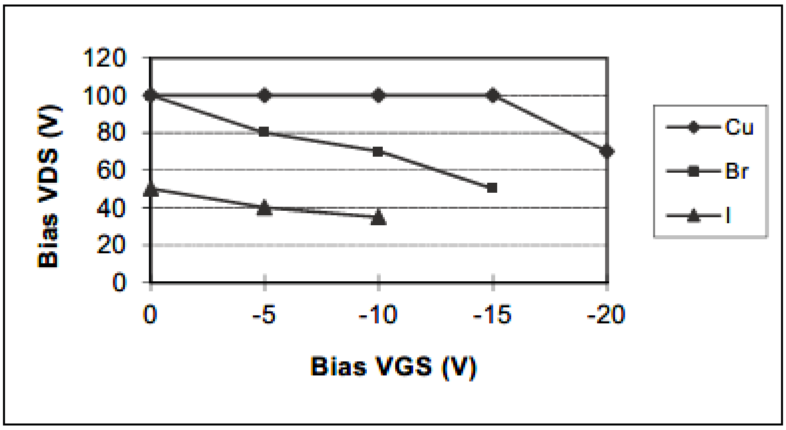


Figure 1 Typical Single Event Effect, Safe Operating Area

3 Electrical Characteristics Curves (Pre-irradiation)

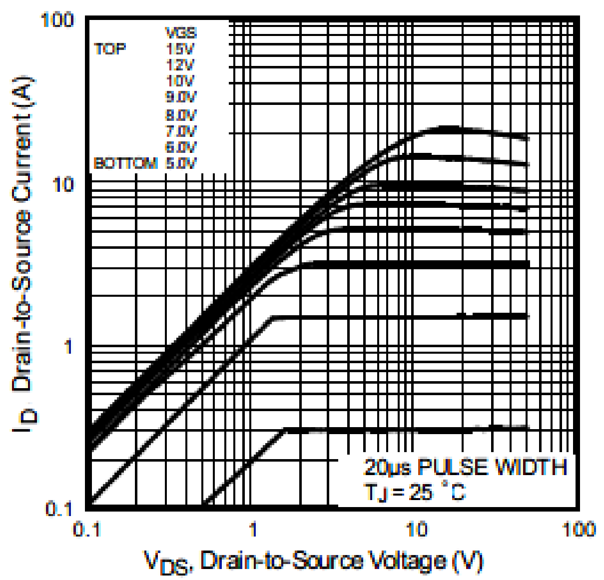


Figure 2 Typical Output Characteristics

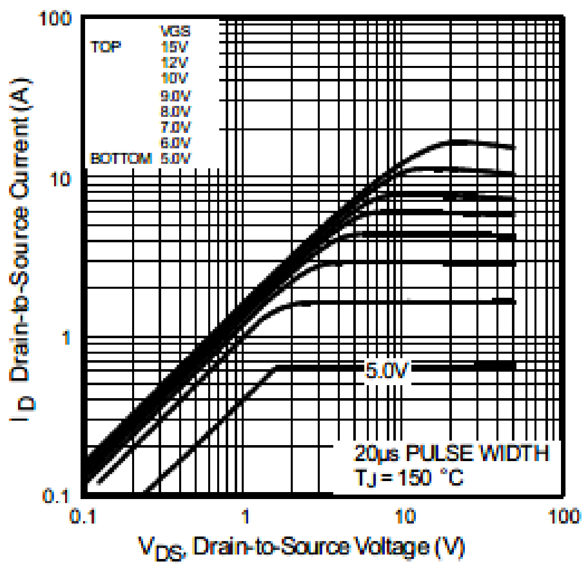


Figure 3 Typical Output Characteristics

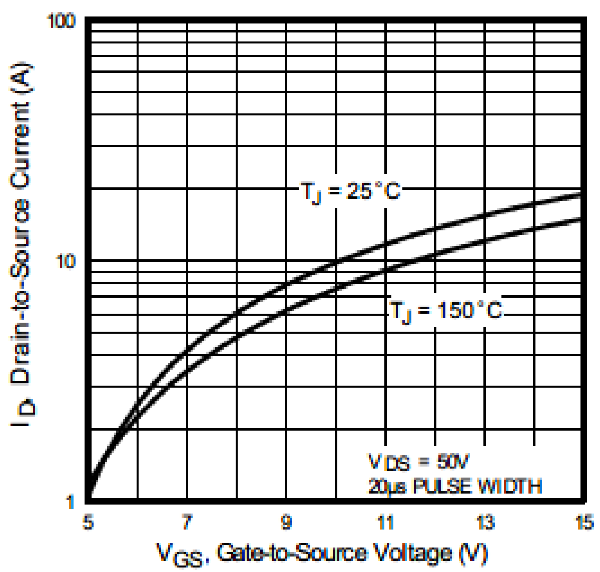


Figure 4 Typical Transfer Characteristics

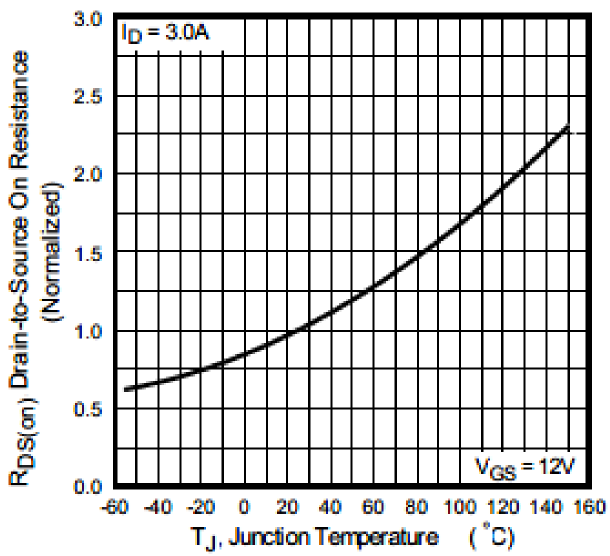


Figure 5 Normalized On-Resistance Vs. Temperature

Electrical Characteristics Curves (Pre-irradiation)

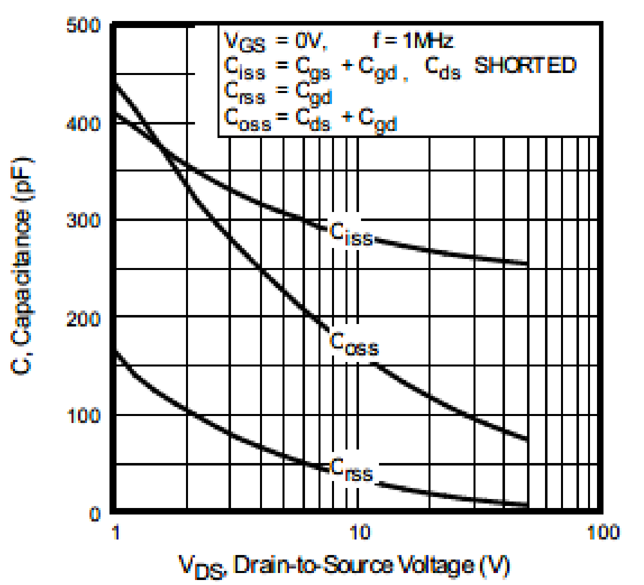


Figure 6 **Typical Capacitance Vs. Drain-to-Source Voltage**

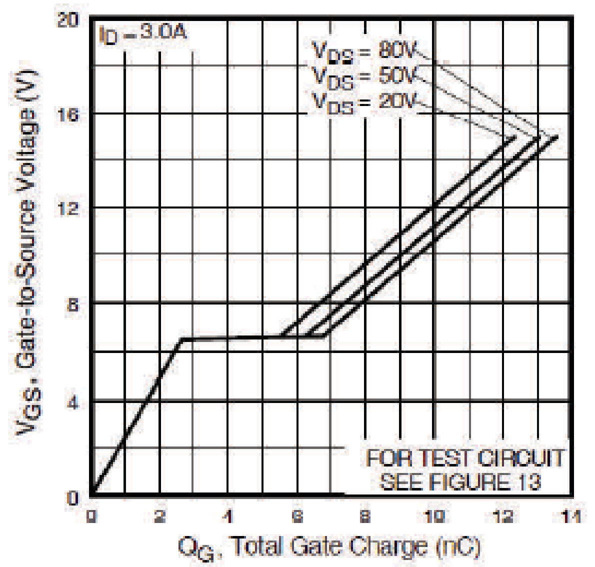


Figure 7 **Typical Gate-to-Source Voltage Vs. Typical Gate Charge**

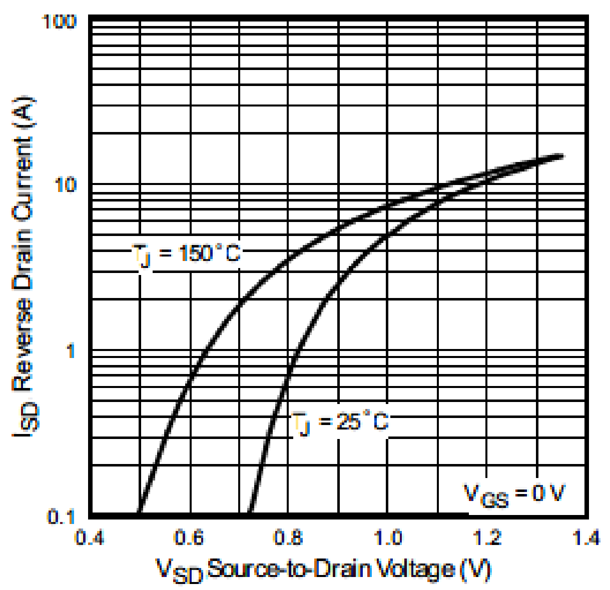


Figure 8 **Typical Source-Drain Current Vs. Diode Forward Voltage**

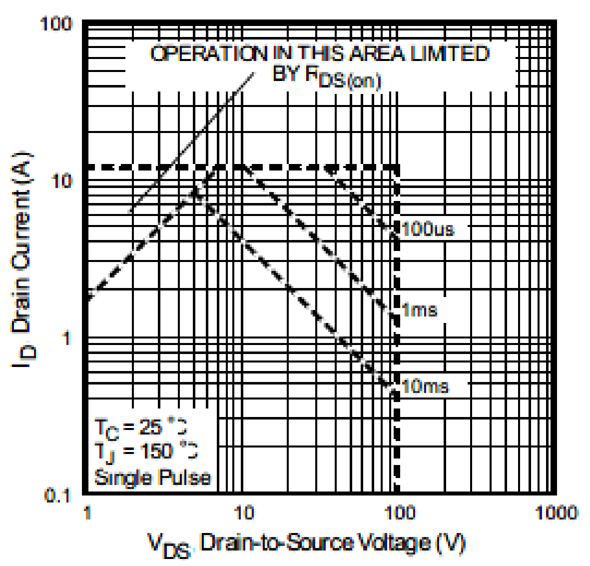


Figure 9 **Maximum Safe Operating Area**

Electrical Characteristics Curves (Pre-irradiation)

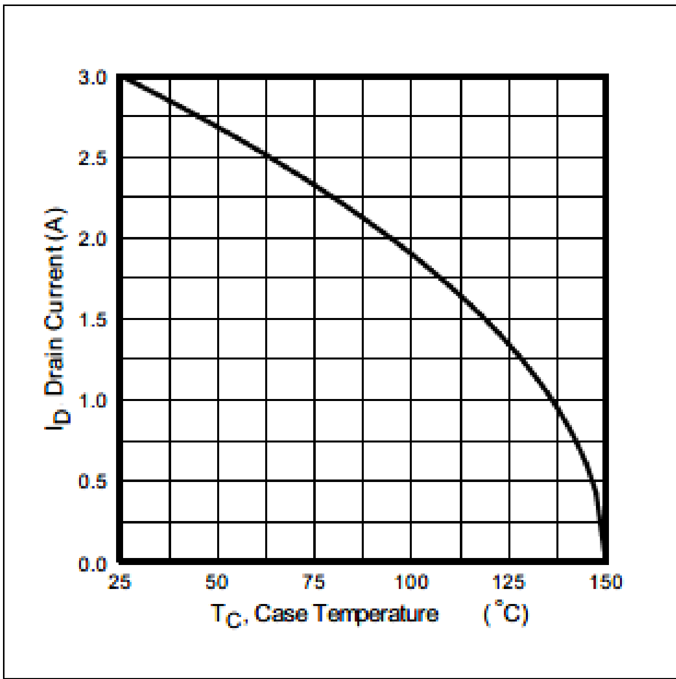


Figure 10 Maximum Drain Current Vs.Case Temperature

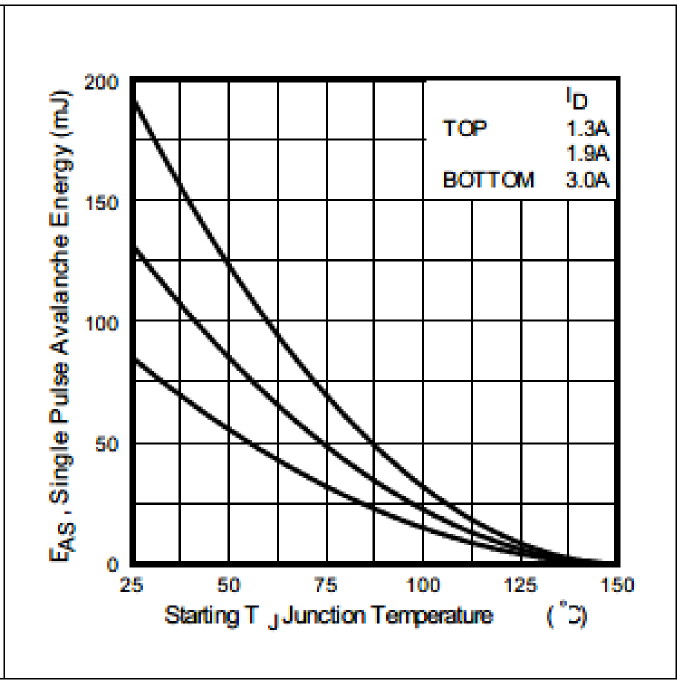


Figure 11 Maximum Avalanche Energy Vs. Junction Temperature

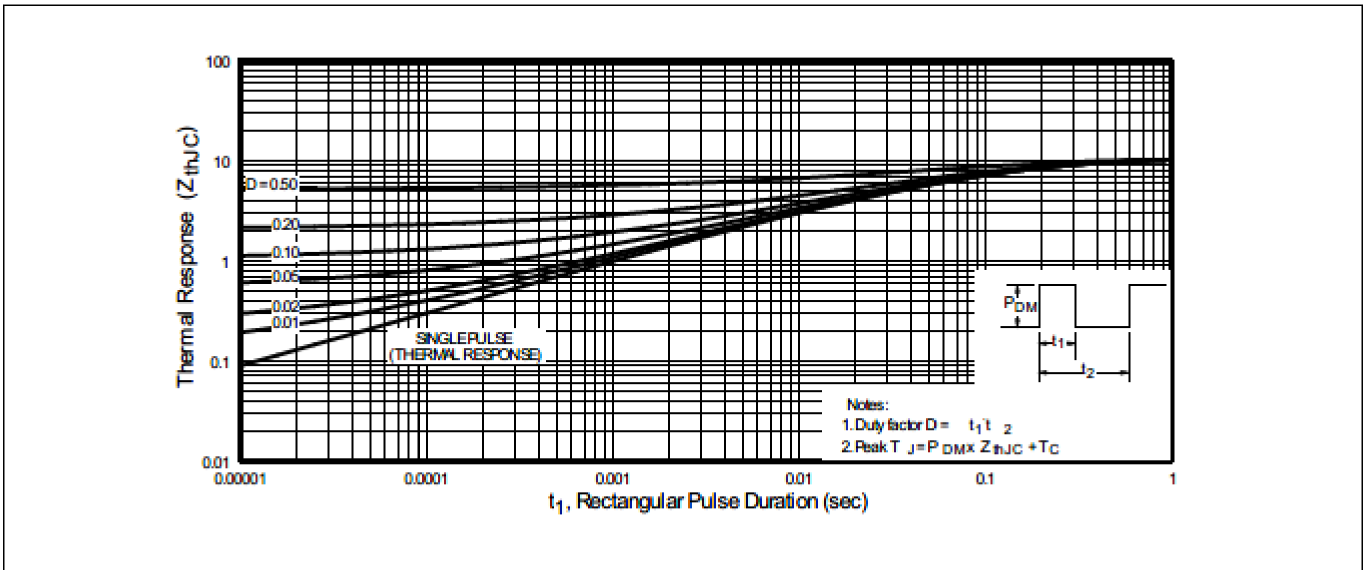


Figure 12 Maximum Effective Transient Thermal Impedance, Junction-to-Case

4 Test Circuits (Pre-irradiation)

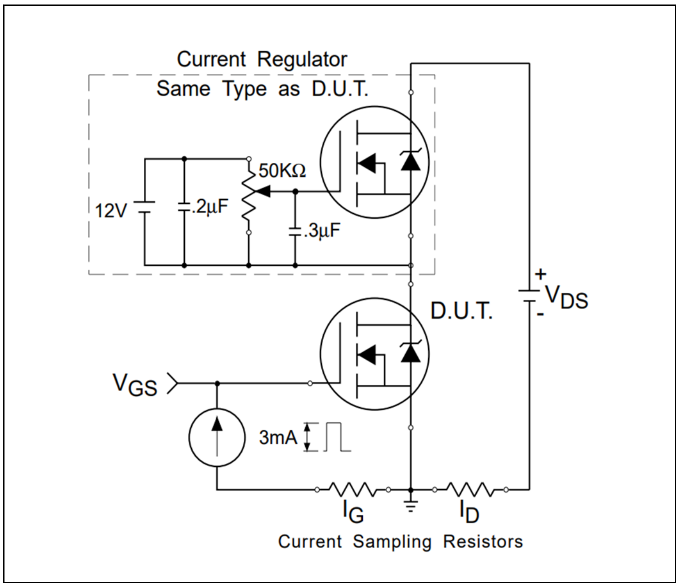


Figure 13 Gate Charge Test Circuit

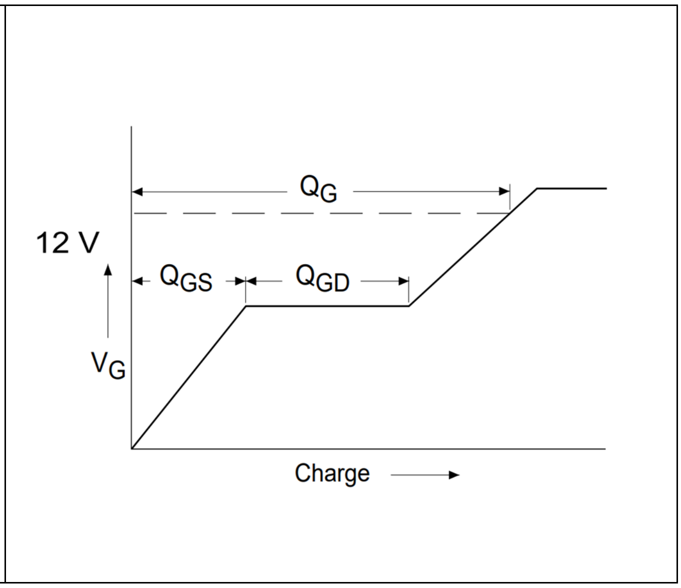


Figure 14 Gate Charge Waveform

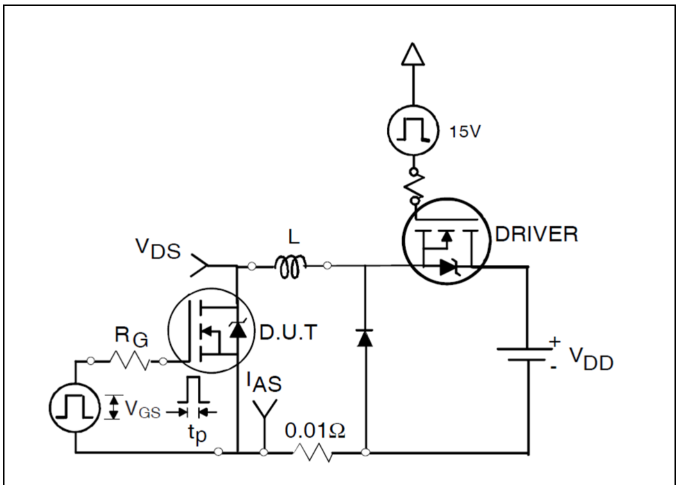


Figure 15 Unclamped Inductive Test Circuit

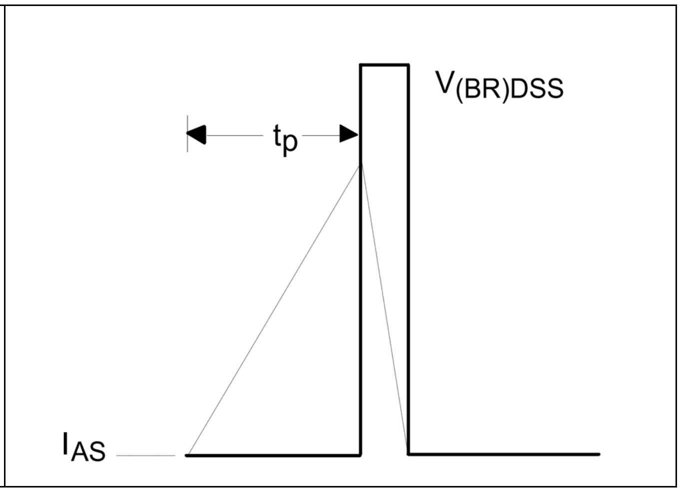


Figure 16 Unclamped Inductive Waveform

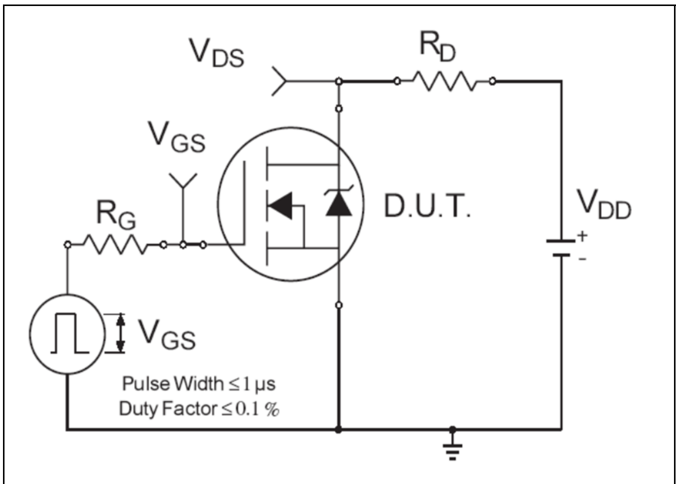


Figure 17 Switching Time Test Circuit

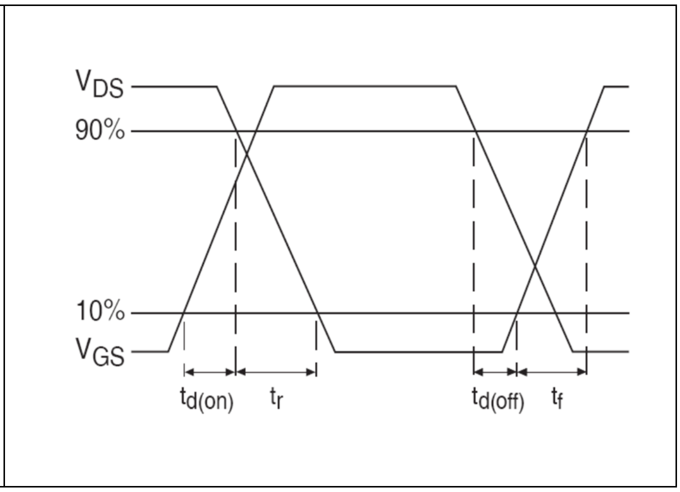
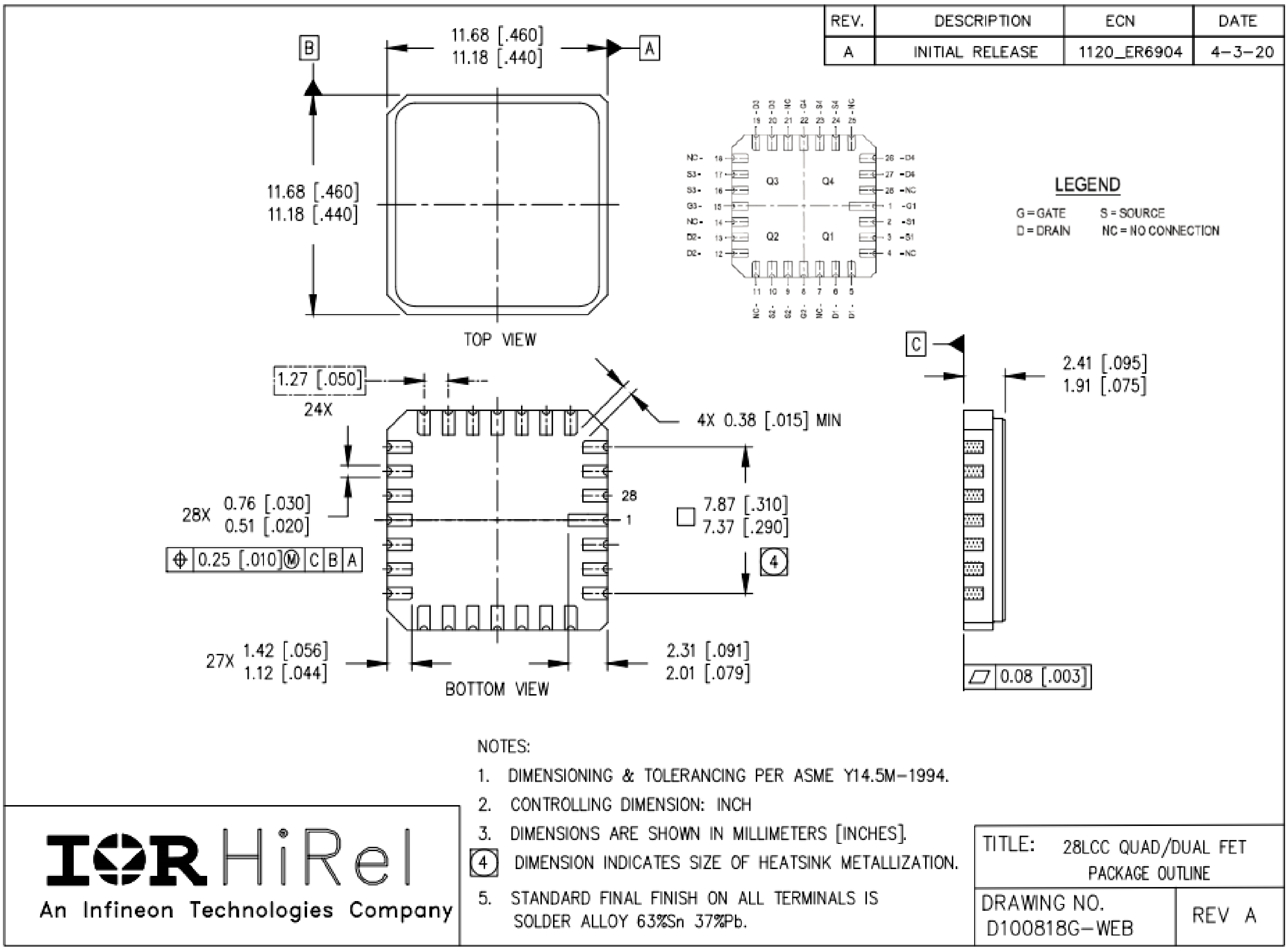


Figure 18 Switching Time Waveforms

5 Package Outline

Note: For the most updated package outline, please see the website: [LCC-28](LCC-28)



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Revision history

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	03/15/2000	Datasheet (PD-93785)
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Rev B	07/20/2011	Updated based on ECN-181.4
Rev C	12/12/2017	Updated based on ECN-1120_05393
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