ISL73847SEH

Radiation Hardened Single/Dual Phase Current Mode PWM Controller

The ISL73847SEH is a synchronous buck controller that can operate as a single or dual phase controller. It is intended to work with the ISL73041SEH (half bridge GaN FET driver) to generate Point-Of-Load voltage rails for commercial space applications.

It accepts an input voltage range of 4.5V to 19V with a programmable output switching frequency between 250kHz and 1.5MHz with a single resistor. The output can regulate a voltage upwards of 600mV and is limited on the top end by the minimum off time and selected switching frequency.

The wide input voltage range makes it a suitable power supply option for a high current FPGA core and other general purpose power solutions. The ISL73847SEH uses current mode modulation which simplifies loop compensation and provides excellent power supply rejection. Additionally, the output is remotely sensed to compensate for any voltage drop in the load conditions. All of this put together results in a robust power supply solution that requires minimal components while achieving high current density.

The ISL73847SEH also features a tri-level output that provides excellent protection against faults by driving a mid scale voltage to signal the power stage to enter a Hi-Z condition.

The ISL73847SEH operates across the military temperature range from -55°C to +125°C and are available in a 24 Ld hermetically sealed Ceramic Dual Flatpack (CDFP) package or in die form.

Features

- Wide operating voltage range:
  - Input: 4.5V to 19V
  - Output: 0.6V to $V_{PWR\_STAGE} \times ((T_{SW}-120ns)/T_{SW})$
- Programmable Output Switching Frequency
  - 250kHz to 1.5MHz
- Optional Droop regulation
- Current mode control provides
  - Excellent power supply rejection
  - Simplified control scheme
- Output differential remote sensing
- Programmable soft-start
- Enable control
- Power-good Indicator
- Radiation acceptance testing
  - LDR (0.01rad(Si)/s): 75krad(Si)
- SEE hardness (see SEE report for details)
  - No SEB/SEL LET_{TH}, VDD = 25V: 86MeV•cm^2/mg
  - SET/SEFI free at LET 86MeV•cm^2/mg
- Qualified to Renesas Rad Hard Hermetic Screening and QCI Flow (R34TB0001EU)
  - All screening and QCI is in accordance with MIL-PRF-38535L Class-V

Applications

- FPGA Core Power Supply
- General Purpose Power Supply

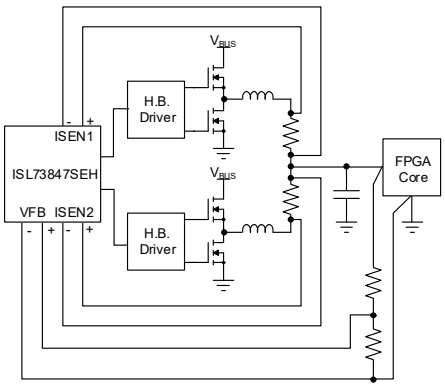


Figure 1. FPGA Core Power Supply Application

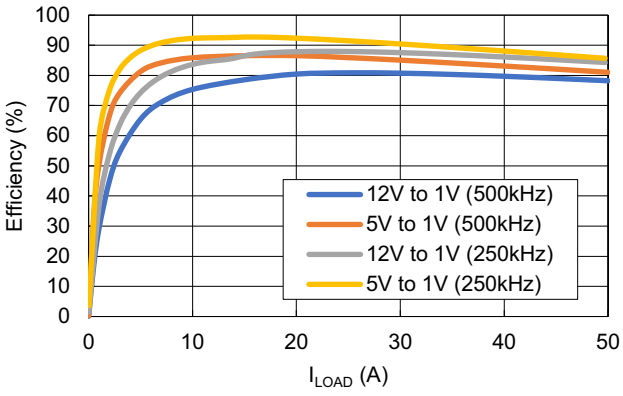


Figure 2. 12V to 1V and 5V to 1V Conversion Efficiency

Contents

1. Overview

1.1 Typical Application Diagrams

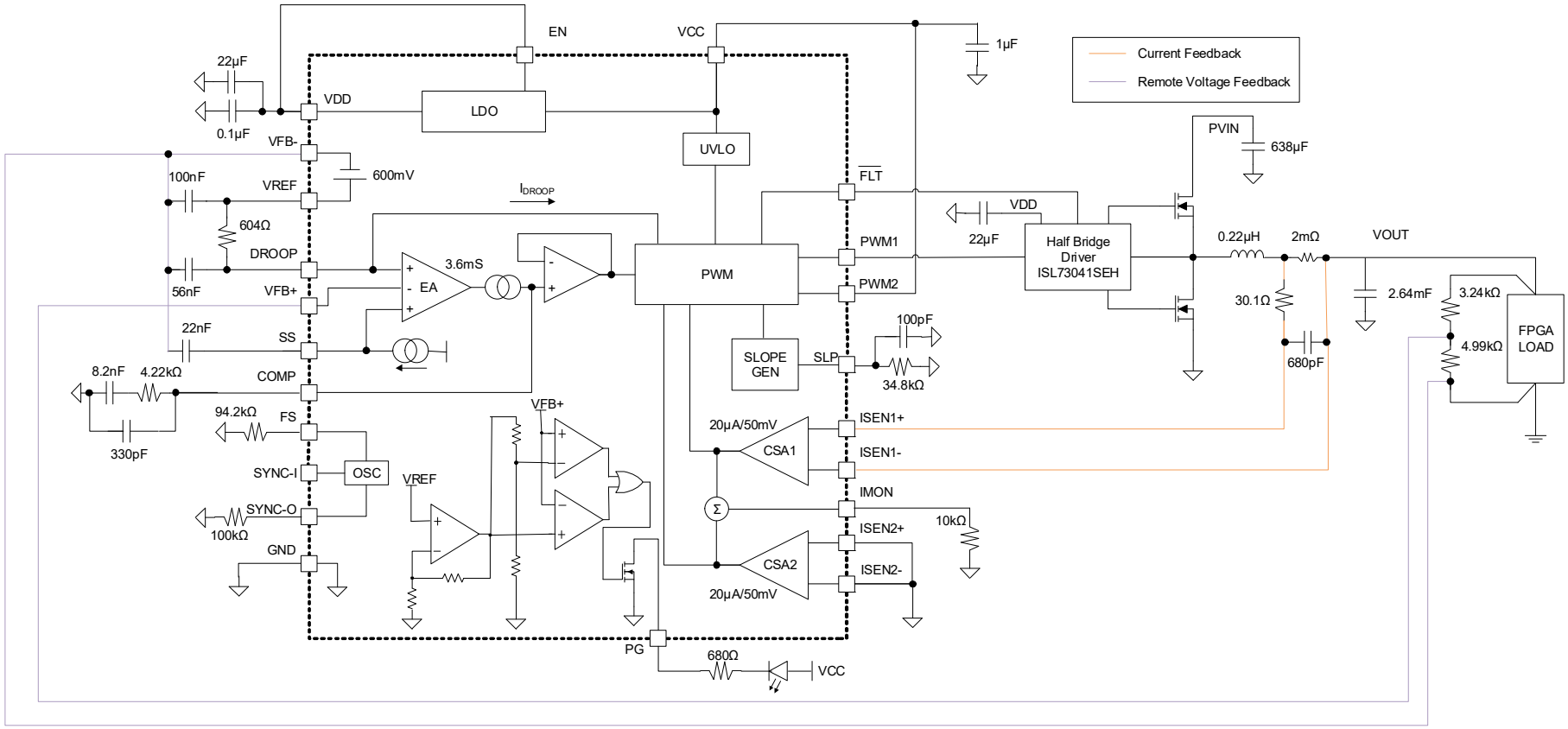


Figure 3. Typical Application (Single Phase)

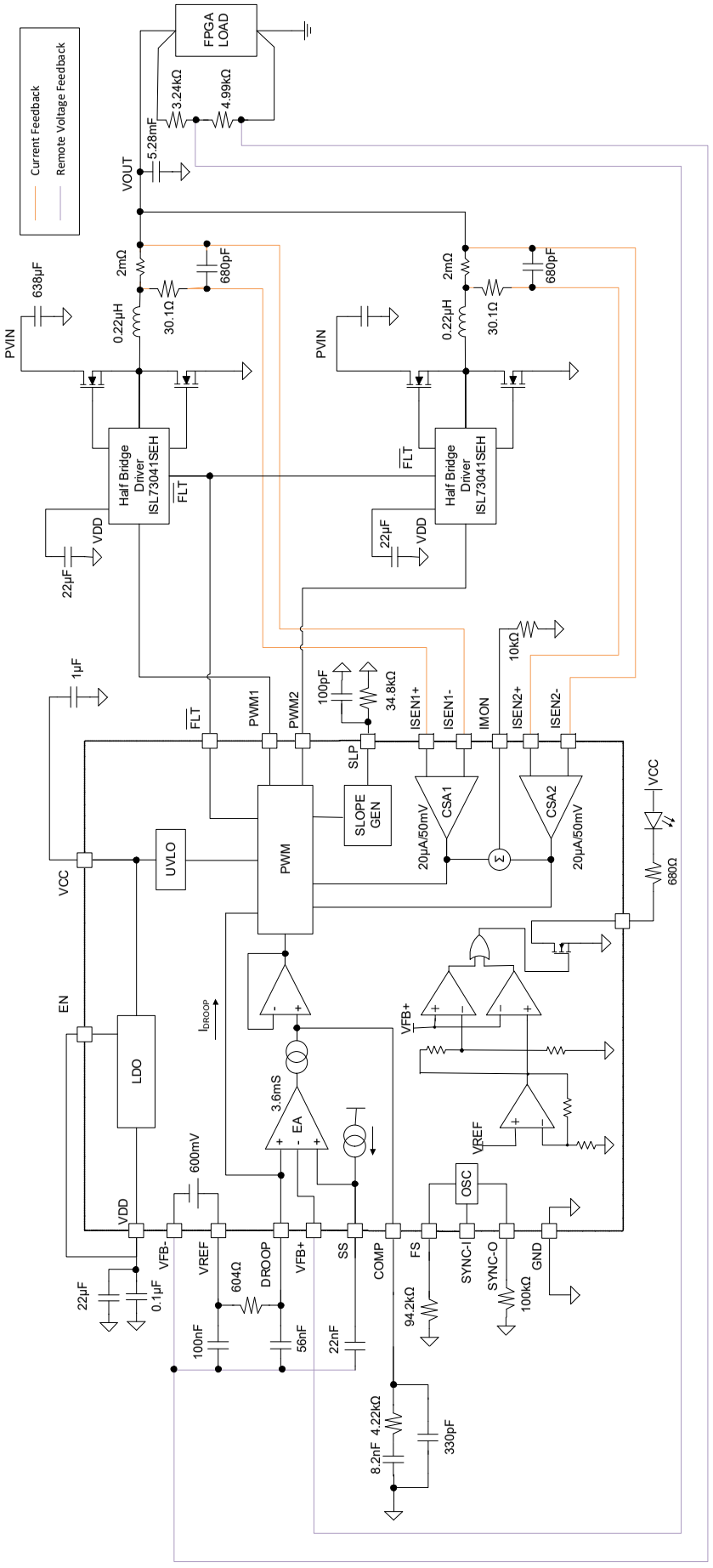


Figure 4. Parallel Configuration to Reduce Resistance or Increase Current Capability

1.2 Functional Block Diagram

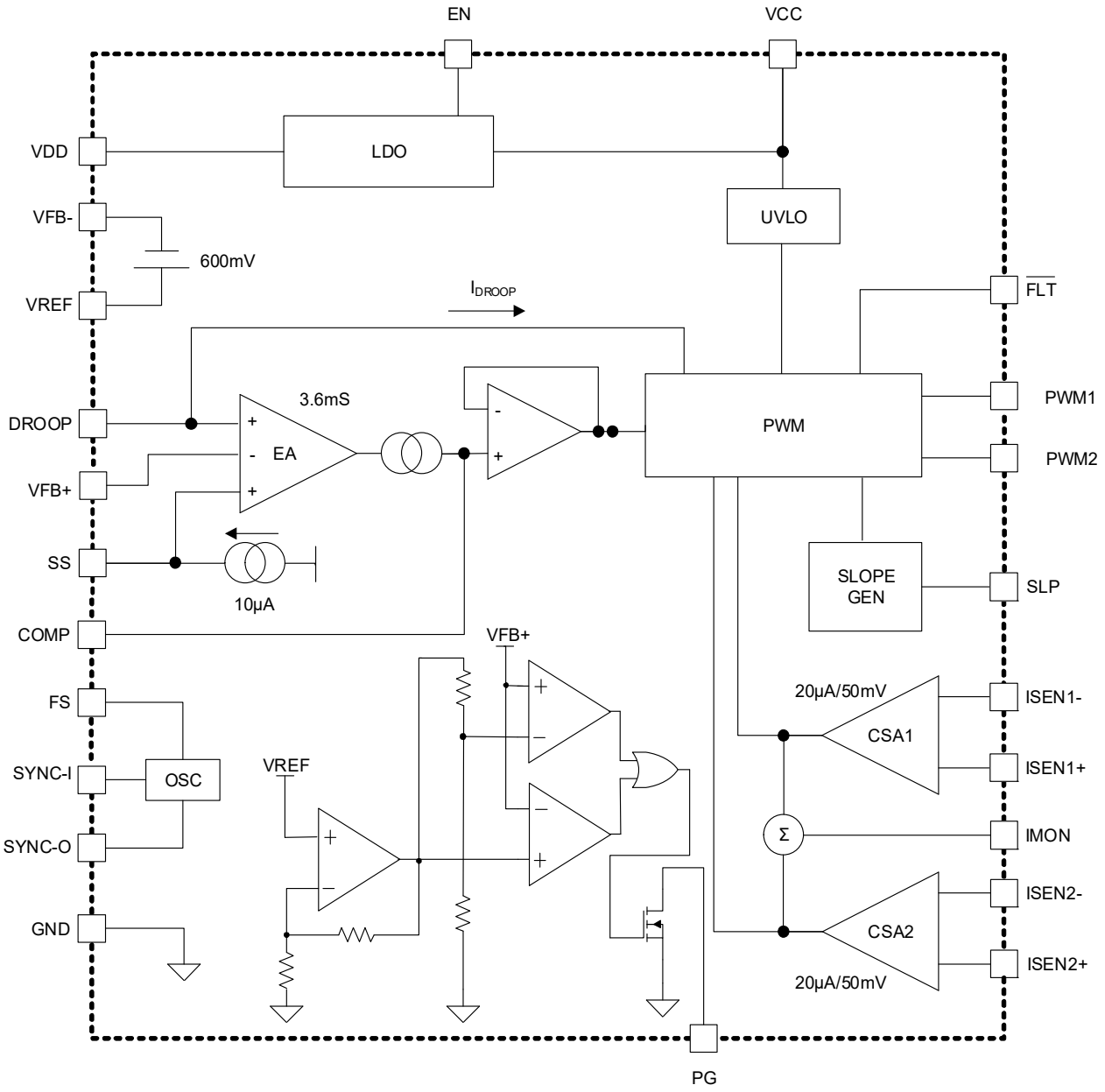
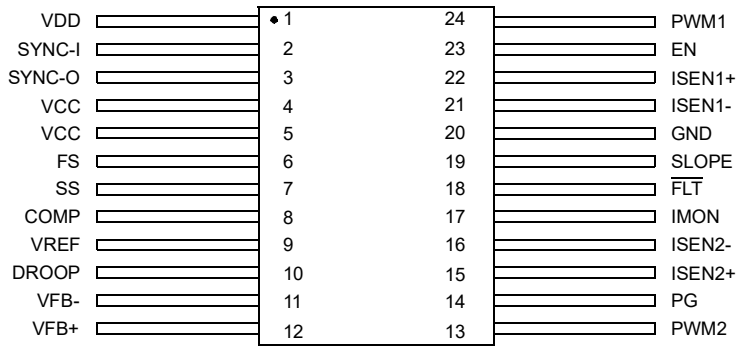


Figure 5. Block Diagram

2. Pin Information

2.1 Pin Assignments

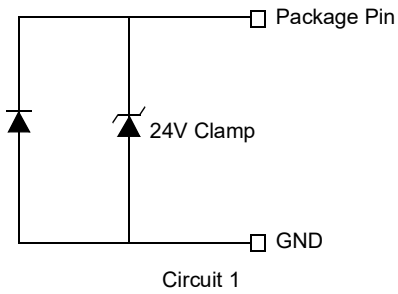


Top View

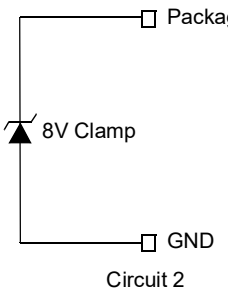
2.2 Pin Descriptions

Pin Number	Pin Name	ESD Circuit	Description
1	VDD	1	The power supply input to the IC. The voltage range on this pin is 4.5V to 19V.
2	SYNC-I	2	This pin is an input that accepts 2x the required output switching frequency (regardless of single or dual phase). Internally the IC divides the clock down to get two clocks 180° from each other for each phase. *Note:* This pin has an internal pull down, leave it floating if SYNC function is not needed.
3	SYNC-O	2	This pin can output either 1x or 2x the output switching frequency depending on the loading present on the pin during power up (before soft-start). When outputting 1x, the SYNC-O is 180° out of phase with phase 1 clock. The 2x SYNC-O output is in phase with the SYNC-I. 100kΩ to VCC: SYNC-O outputs 1x output switching frequency. 100kΩ to GND: SYNC-O outputs 2x output switching frequency.
4	VCC	2	Output of internal LDO for analog circuity, short this pin to pin 5. Connect a 1µF ceramic capacitor from VCC to GND.
5			Output of internal LDO for analog circuity, short this pin to pin 4. Connect a 1µF ceramic capacitor from VCC to GND.
6	FS	2	This pin sets the frequency for the internal oscillator between 0.5MHz and 3MHz. This sets the output between 0.25 MHz and 1.5MHz for each phase. When FS is tied to VCC the oscillator switching frequency (f_{OSC}) is 0.5MHz, a resistor between FS and GND adjusts the frequency between 0.5MHz and 3 MHz. If SYNC-I is being used to sync to an external clock, FS needs to be set to a frequency 15% less than the external clock. Equation 1 can be used to find an what resistor is needed for a given frequency.
7	SS	2	This is the soft-start pin, connect a ceramic capacitor from SS to GND to set the soft-start ramp. The soft-start time is adjustable between 2ms and 200ms. Equation 21 shows the relationship between the soft-start capacitor and soft-start time.
8	COMP	2	Output of error amplifier, connect a resistor and capacitor in series to ground for type 2 compensation adjustment. For type 3 compensation, add an additional capacitor in parallel with the type 2 series RC components.
9	VREF	2	Output for the internal voltage reference. Insert a resistor between VREF and DROOP to enable droop regulation. Short VREF and DROOP pin together to disable droop regulation.

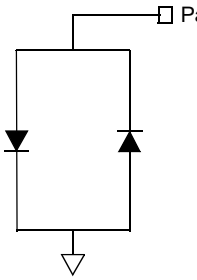
Pin Number	Pin Name	ESD Circuit	Description
10	DROOP	2	This pin is a current mirrored version of the output of the current sense amp output (sum of both phases). This output can be tied to the VREF pin through a resistor to enable droop regulation. The voltage created by the mirrored current and the resistor between VREF and DROOP sets the droop level.
11	VFB-	3	This pin is the negative input for differential voltage feedback.
12	VFB+	5	This pin is the positive input for differential voltage feedback.
13	PWM2	2	This pin is the PWM output for the secondary phase. Needs 100kΩ to GND.
14	PG	1	This pin is the power good indicator. It is an open-drain output, limit the sink current through this pin to below 7.2mA.
15	ISEN2+	4	This pin is the positive input for the secondary phase current sense amplifier.
16	ISEN2-	1	This pin is the negative input for the secondary phase current sense amplifier.
17	IMON	2	This pin outputs the summed average of the current sense amplifiers outputs for telemetry purposes.
18	$\overline{FLT}$	2	This pin sequences the startup between the ISL73847SEH and the ISL73041SEH. On the ISL73847SEH, this pin operates as a bi-directional I/O during power up (before soft-start) and as an input while switching (during and after soft-start). A logic low on this pin indicates that either the ISL73847SEH or ISL73041SEH has encountered a fault or is not ready to start switching. A logic high indicates that there is no faults for either device.
19	SLOPE	2	This pin adjusts the slope compensation of the ISL73847SEH. Place a resistor in the range of 25kΩ to 100kΩ to adjust slope compensation.
20	GND	N/A	This is the ground reference for the ISL73847SEH. This pin is tied to the package seal ring (lid).
21	ISEN1-	1	This pin is the positive input for the primary phase current sense amplifier.
22	ISEN1+	4	This pin is the negative input for the primary phase current sense amplifier.
23	EN	1	This pin is the chip enable for the ISL73847SEH.
24	PWM1	2	This pin is the PWM output for the primary phase. Needs 100kΩ to GND.
-	Lid	N/A	The lid is electrically connected to pin 20 (GND).



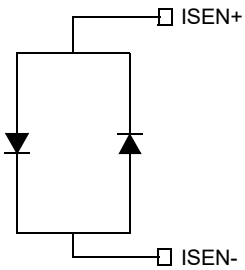
Circuit 1



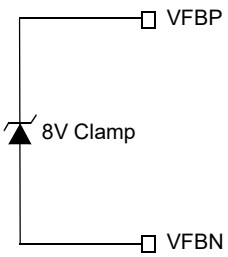
Circuit 2



Circuit 3



Circuit 4



Circuit 5

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VDD, ISENSx, EN, PG	GND - 0.3	GND + 20	V
VDD, EN, PG[1]	GND - 0.3	GND + 20	V
ISENSx[1]	GND - 0.3	GND + 10	V
VCC	GND - 0.3	6.5	V
VCC[1]	GND - 0.3	5.3	V
VREF, DROOP, VFBx, FS, COMP, SLOPE, $\overline{FLT}$, IMON	GND - 0.3	VCC + 0.3	V
PWMx, SYNC-I, SYNC-O	GND - 0.3	VCC + 0.3	V
Differential Voltage Across Current Sense Inputs V(ISENx+) - V(ISENx-)[2]	- 0.3	+ 0.3	V

1. Tested under a heavy ion environment at LET = 86MeV•cm^2/mg at 125°C (T_C) for Single Event Burnout (SEB). See the SEE Test Report for more details.
2. Maximum current through anti-parallel diodes show be ≤10mA.

3.2 ESD Ratings

ESD Model/Test	Rating	Unit
Human Body Model (Tested per MIL-STD-883 TM3015.7)	2	kV
Charged Device Model (Tested per JS-002-2018)	750	V
Latch-Up (Tested per JESD78E; Class 2, Level A)	±100	mA

3.3 Thermal Information

Package Description	Thermal Resistance (Typical)	
	θ_{JA}(°C/W)[1]	θ_{JC}(°C/W)[2]
24 Lead CDFP Package	23	1.7

1. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board (two buried 1 oz copper planes) using direct attach features with package base mounted to PCB thermal land (with thermal vias below) with Epoxy (10 mils thick with a k of 1W/m-K). See TB379.
2. For θ_{JC}, the case temperature location is the center of the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature	-	+150	°C
Storage Temperature Range	-65	+150	°C

3.4 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
VDD, EN, PG	GND + 4.5	GND + 19.0	V
ISENx Common Mode Range	GND - 0.3	10	V
Differential Voltage Across Current Sense Inputs V(ISENx+) - V(ISENx-)	-75	100	mV
PWM Output Switching Frequency	0.5	1.5	MHz
Regulated Output Voltage	0.6	$PVIN\times((T_{SW}-120ns)/T_{SW})$	V
Ambient Temperature	-55	125	°C

3.5 Electrical Specifications

V_{DD} = 4.5V & 19V, C_{VCC} = 1µF and T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Temp.	Min[1]	Typ [2]	Max[1]	Unit
Input Power Supply							
Supply Voltage Range	V_{DD}		-55 to +125°C	**4.5**		**19**	V
Rising V_{DD} UVLO	$VDD_{UV(R)}$	EN = V_{DD}		**4.05**	4.2	**4.4**	V
Falling V_{DD} UVLO	$VDD_{UV(F)}$	EN = V_{DD}		**3.85**	4.0	**4.1**	V
V_{DD} UVLO Hysteresis	$VDD_{UV(HYS)}$	EN = V_{DD}		**150**	220	**300**	mV
Operating Supply Current	I_{DDO}	V_{DD} = 4.5V, 12V, 19V EN = 3.3V, f_{SW} = 500kHz, C_L=100pF		**9**	12	**16**	mA
Shutdown Supply Current	I_{DDSD}	V_{DD} = 4.5V, 12V, 19V EN = GND			11	**35**	µA
Internal LDO							
Output Range	VCC	V_{DD} = 6.0V, 19V I_{OUT} = 0mA, 20mA	-55 to +125°C	**4.7**	5.0	**5.3**	V
Dropout Voltage	VCC_{DO}	V_{DD} = 4.5V, I_{OUT} = 50mA		**85**	160	**250**	mV
Rising V_{CC} UVLO	$VCC_{UV(R)}$	EN = V_{DD}		**3.4**	3.6	**3.7**	V
Falling V_{CC} UVLO	$VCC_{UV(F)}$	EN = V_{DD}		**3.2**	3.3	**3.5**	V
V_{CC} UVLO Hysteresis	$VCC_{UV(HYS)}$	EN = V_{DD}		**150**	210	**300**	mV
V_{CC} Foldback Current	I_{CC-SC}	V_{DD} = 19V, V_{CC} = 0V, EN = 1.6V		**40**	72	**90**	mA
V_{CC} Overcurrent Limit	I_{CC-CL}	V_{DD} = 19V, V_{CC} = 4.3V, EN = 1.6V		**75**	98	**130**	mA

V_{DD} = 4.5V & 19V, C_{VCC} = 1µF and T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp.	Min[1]	Typ [2]	Max[1]	Unit
Output Regulation							
Set Point Voltage[3]	V_{FB+}	$V_{REF} = V_{DROOP}$ $V_{SEN1} = V_{SEN2}$ = 0mV, 50mV	-55°C	0.596	0.597	0.601	V
			+25°C	0.599	0.600	0.603	V
			+125°C	0.597	0.600	0.604	V
			+25°C (Post Rad)	0.597	0.600	0.604	V
Set Point Accuracy Over Line Delta[3],[4]	V_{FB+}	$V_{REF} = V_{DROOP}$ VSEN1 = VSEN2 = 0mV	-55 to +125°C	**-1**	0.2	**0.6**	mV
Set Point Accuracy Over Load Delta[3],[4]	V_{FB+}	$V_{REF} = V_{DROOP}$ $V_{SEN1} = V_{SEN2}$ = 0mV, 50mV		**-0.75**	0.05	**0.75**	mV
FB+ Input Bias Current	$I_{FB+BIAS}$	V(FB+) = 0.6V		**-50**	-0.25	**50**	nA
FB- Input Bias Current	$I_{FB-BIAS}$	V(FB-) = 0V, EN>$V_{IH-EN-G}$ $V_{SEN1} = V_{SEN2}$ = 0mV		**30**	121	**350**	µA
Soft-Start Sourcing Current	$I_{SOFTSTART}$			**9.2**	10	**10.5**	µA
Soft-Start Pull-Down Resistance	$R_{SS-PULLDN}$	EN = 0V		**4**	11	**18**	Ω
Protection Features							
Peak Positive Current Limit Threshold	V_{PCL}	V_{CM} = 0.6V, 5.0V, 19V	-55 to +125°C	**67.5**	75	**82.5**	mV
Peak Positive Overcurrent Threshold	V_{POC}	V_{CM} = 0.6V, 5.0V, 19V		**90**	100	**110**	mV
Peak Negative Overcurrent Threshold	V_{NOC}	V_{CM} = 0.6V, 5.0V, 19V		**-84**	-71	**-60**	mV
Overvoltage Threshold	$V_{(FB, OV)}$	V_{DD} = 4.5V and 19V		**112**	115	**118**	%
Undervoltage Threshold	$V_{(FB, UV)}$	V_{DD} = 4.5V and 19V		**82**	85	**88**	%
$\overline{FLT}$ Drive current	$I_{\overline{FLT}}$	V_{DD} = 4.5V and 19V, $\overline{FLT}$ = 400mV		**20**	50	**75**	mA
$\overline{FLT}$ Mid Threshold Voltage	$V_{\overline{FLT}MID}$	V_{DD} = 4.5V and 19V		**1.6**	2.08	**2.55**	V
$\overline{FLT}$ Leakage Current	$I_{\overline{FLT}LKG}$	$\overline{FLT}$ = 4.5V when V_{DD} = 4.5V $\overline{FLT}$ = 5V when V_{DD} = 19V		**-2**	0.07	**2**	µA
Error Amplifier							
Transconductance	g_{m-EA}		-55°C	3	4.1	4.5	mA/V
			+25°C	3	3.57	4	mA/V
			+125°C	2.5	3.04	3.5	mA/V
			+25°C (Post Rad)	3	3.6	4	mA/V

V_{DD} = 4.5V & 19V, C_{VCC} = 1µF and T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp.	Min[1]	Typ [2]	Max[1]	Unit
DC Gain[5]	A_{V-EA}		-55 to +125°C	66	80		dB
Gain-Bandwidth Product[5]	GBW_{EA}			15			MHz
Output Voltage Range	$V_{COMP(RNG)}$	V_{DD} = 4.5V		**0.4**		**4.1**	V
		V_{DD} = 19V		**0.4**		**4.6**	
Output Slew Rate[5]	SR_{EA}				8.5		V/µs
Current-Sense Amplifier							
Droop Transconductance	$g_{m(CSA, DRP)}$	$V(I_{SEN+}, I_{SEN-})$ = 10mV, 50mV V_{CM} = 0.6V, 5.0V, 19V	-55°C	0.38	0.4	0.42	µA/mV
			+25°C	0.38	0.4	0.42	µA/mV
			+125°C	0.375	0.39	0.41	µA/mV
			+25°C (Post Rad)	0.38	0.4	0.42	µA/mV
Droop Current	$Error_{DRP}$	$V(I_{SEN+}, I_{SEN-})$ = 50mV, V_{CM} = 0.6V, 5.0V, 19V	-55°C	16	18.7	23.5	µA
			+25°C	18.2	19.9	21.8	µA
			+125°C	17.5	20.5	23.5	µA
			+25°C (Post Rad)	16	19.7	23.5	µA
IMON Transconductance	$g_{m(CSA, IMON)}$	$V(I_{SEN+}, I_{SEN-})$ = 10mV, 50mV V_{CM} = 0.6V, 5.0V, 19V	-55 to +125°C	**0.36**	0.39	**0.47**	µA/mV
Gain from CSA input to PWM Comparator input	$A_{CSA-PWM}$	$V(I_{SEN+}, I_{SEN-})$ = 50mV		**7.5**	8	**8.5**	mV/mV
Offset Voltage (Low and High side sense amps are triple redundant)	$V_{OS(CSA)}$	$V(I_{SEN+} - I_{SEN-})$ = 0mV V_{CM} = 0.6V, 5.0V, 19V	-55°C	-4.5	-0.2	4.5	mV
			+25°C	-2	-0.05	2	mV
			+125°C	-4.5	0.15	4.5	mV
			+25°C (Post Rad)	-4.5	-0.13	4.5	mV
Positive Input Leakage Current	$I_{LKG+(CSA)}$	EN = 0V, V_{CM} = 0.6V, 5.0V, 19V	-55 to +125°C	**-50**	4	**50**	nA
Negative Input Leakage Current	$I_{LKG-(CSA)}$	EN = 0V, V_{CM} = 0.6V			1.55	**200**	nA
		EN = 0V, V_{CM} = 5.0V, 19V			0.325	**1.0**	µA
HS CSA Supply Current per Phase (Current into ISENx- pin)	I_{CSA}	EN = 3.3V, V_{CM} = 2.7V			2	**3**	µA
Transition from Low Side to High Side	$V_{CS(TRAN)}$	VDD = 4.5V		**1.95**	2.13	**2.35**	V
Transition from Low Side to High Side	$V_{CS(TRAN)}$	VDD = 19V		**2.25**	2.37	**2.5**	V
Gain-Bandwidth Product[5]	GBW_{CSA}			**10**			MHz

V_{DD} = 4.5V & 19V, C_{VCC} = 1µF and T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp.	Min[1]	Typ [2]	Max[1]	Unit
Oscillator/Slope Generator							
Default Oscillator Frequency	f_{OSC-D}	FS = VC_C, V_{DD} = 4.5V, 19V	-55 to +125°C	**0.90**	1.00	**1.10**	MHz
Oscillator Frequency Range	$f_{OSC-0.5M}$	R_{FS} = 205kΩ, EN = 3.3V, R_{SYNC-O} = 100kΩ to GND		**0.45**	0.5	**0.55**	MHz
	f_{OSC-1M}	R_{FS} = 94.2kΩ, EN = 3.3V, R_{SYNC-O} = 100kΩ to GND		**0.90**	1.00	**1.10**	MHz
	f_{OSC-2M}	R_{FS} = 37kΩ, EN = 3.3V, R_{SYNC-O} = 100kΩ to GND		**1.80**	2.00	**2.20**	MHz
	f_{OSC-3M}	R_{FS} = 16.7kΩ, EN = 3.3V, R_{SYNC-O} = 100kΩ to GND		**2.70**	3.00	**3.30**	MHz
Slope Pin Current	I_{SLOPE}	V_{SLOPE} = 400mV, V_{DD} = 4.5V, 19V		**11.2**	12	**12.6**	µA
Default Slope Compensation Reference Voltage	V_{SLOPE_DFLT}		-55 to +125°C	**1.14**	1.2	**1.26**	V
Ramp Slope	$V_{RAMP-SLOPE}$	f_{SW} = 500kHz, V_{SLOPE} = 0.4V	-55 to +125°C	**0.065**	0.098	**0.150**	V/µs
Enable							
Rising Enable Threshold (Gross)	$V_{IH-EN-G}$	FS = V_{CC}	-55 to +125°C	**0.9**	1.3	**1.6**	V
Falling Enable Threshold (Gross)	$V_{IL-EN-G}$	FS = V_{CC}		**0.6**	1.0	**1.2**	V
Enable Threshold Hysteresis (Gross)	$V_{HYS-EN-G}$	FS = V_{CC}		**200**	350	**500**	mV
Rising Enable Threshold (Fine)	$V_{IH-EN-F}$	FS = V_{CC}		**1.74**	1.8	**1.85**	V
Falling Enable Threshold (Fine)	$V_{IL-EN-F}$	FS = V_{CC}		**1.46**	1.5	**1.54**	V
Enable Threshold Hysteresis (Fine)	$V_{HYS-EN-F}$	FS = V_{CC}		**260**	295	**320**	mV
EN Rising to Boot Refresh Delay	t_{EN}	FS = V_{CC}		**1.9**	2.3	**2.8**	ms
Pull Down Resistance	R_{EN}	EN = 19V			1		MΩ
EN Leakage	EN_{LK}	V_{DD} = EN = 19V		**20**	120	**250**	nA

V_{DD} = 4.5V & 19V, C_{VCC} = 1µF and T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp.	Min[1]	Typ [2]	Max[1]	Unit
Power Good							
Overvoltage Error Threshold	V_{OVH}	EN = 3.3V, FB as a percent of V_{REF}	-55 to +125°C	**106**	108	**110**	%
Overvoltage Error Threshold Recovery	V_{OVL}	EN = 3.3V, FB as a percent of V_{REF}		**104**	106	**109**	%
Overvoltage Error Hysteresis	V_{OVH}	EN = 3.3V, FB as a percent of V_{REF}		**1.2**	2	**3.0**	%
Undervoltage Error Threshold	V_{UVL}	EN = 3.3V, FB as a percent of V_{REF}		**90**	92	**94**	%
Undervoltage Error Threshold Recovery	V_{UVH}	EN = 3.3V, FB as a percent of V_{REF}		**92**	94	**96**	%
Undervoltage Error Hysteresis	V_{UVH}	EN = 3.3V, FB as a percent of V_{REF}		**1.2**	2.05	**3.0**	%
Sink Current	$I_{PG-SINK}$	V_{DD} = 4.5V, V(FB+, FB-) = V_{PG} = 0.4V EN = 0V		**5**	18	**35**	mA
PG Leakage	I_{PG-LKG}	V_{DD} = 4.5V, V(FB+, FB-) = 0.6V, V_{PG} = 19V EN = 0V	-55 to +125°C		0.02	**0.5**	µA
SS Voltage for PG to be Active After Power-Up	V_{SS-PG}	V(SS) = 0V to 1V.		**0.82**	0.9	**0.98**	V
PG Reaction Time to OV Fault	$t_{PG-PROP-OV}$	V(FB+, FB-) = 0.6V to 0.7V		**12**	14.5	**18**	µs
PG Reaction time to UV Fault	$t_{PG-PROP-UV}$	V(FB+, FB-) = 0.6V to 0.5V		**12**	14.6	**18**	µs
Hiccup Retry Delay	$t_{HIC-DLY}$	C_{SS} = 10nF		**2**	2.7	**4**	ms

V_{DD} = 4.5V & 19V, C_{VCC} = 1µF and T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp.	Min[1]	Typ [2]	Max[1]	Unit
PWM Outputs							
PWM Output High	V_{OH}	V_{DD} = 4.5V, I_{PWM} = -500µA	-55 to +125°C	**4.0**			V
		V_{DD} = 19V, I_{PWM} = -500µA		**4.5**			
PWM Output Mid	V_{OZ}	I_{PWM} = ±100µA		**1.8**	2.0	**2.3**	V
PWM Output Low	V_{OL}	I_{PWM} = +500µA			0.05	**0.4**	V
Turn-On Blanking Time	$t_{MINONBLK}$			**90**	99	**115**	ns
Turn-Off Blanking Time	$t_{MINOFFBLK}$			**100**	112	**130**	ns
Minimum Controllable ON-Time	$t_{MINCTRLON}$			**100**	115	**135**	ns
Minimum Controllable OFF-Time	$t_{MINCTRLOFF}$			**100**	116	**135**	ns
Passive Pull-Down	$R_{PWM-PLDN}$				5		MΩ
Current Share between Phase 1 & 2[5]	$I_{PHSHARE}$	V_{CM} = 0.6V, 5V, 19V			8		%
Boot Refresh Repeat Timer	t_{BOOT}			**62**	68	**75**	µs
SYNC							
SYNC-I Input Voltage High	V_{SYNCH}		-55 to +125°C	**1.7**			V
SYNC-I Input Voltage Low	V_{SYNCL}					**0.8**	V
SYNC-I Frequency (Referred to Internal Oscillator)	f_{SYNCI}	FOSC = 500kHz, R_{FS} = 205kΩ		**15**			%
SYNC-I Frequency (Referred to Internal Oscillator)	f_{SYNCI}	FOSC = 2MHz, R_{FS} = 37kΩ		**15**			%
SYNC-I Input Current	$I_{SYNC-IN}$	V_{SYNC} = 5V		**2.5**	5	**7.0**	µA
SYNC-I Pull-Down Resistance	$R_{SYNC-PULLDN}$	V_{SYNC} = 5V			1		MΩ
SYNC-O Output Voltage High	$V_{SYNC-OH}$	V_{DD} = 4.5V, I_{SYNC-O} = -500µA		**4.2**			V
		V_{DD} = 19V, I_{SYNC-O} = -500µA		**4.6**			
SYNC-O Output Voltage Low	$V_{SYNC-OL}$	I_{SYNC-O} = +500µA				**0.4**	V
SYNC-I to PWM2 Delay	$t_{SYNC-I-DEL}$				20		ns
SYNC-O to PWM2 Delay	$t_{SYNC-O-DEL}$				150		ns
SYNC-I to SYNC-O Delay	$t_{SYNC-DLY}$	50% of SYNC-I to 50% of SYNC-O		**215**	240	**275**	ns

V_{DD} = 4.5V & 19V, C_{VCC} = 1µF and T_A = +25°C; unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Temp.	Min[1]	Typ [2]	Max[1]	Unit
SYNC-O to PWM1 Phase Shift	$t_{SYNCO-PWM1}$	Phase shift from PWM1	-55 to +125°C	**178**	180	**184**	°
PWM1 to PWM2 Phase Shift	$t_{PWM1-PWM2}$	Phase shift from PWM1 to PWM2		**174**	180	**186**	°

1. Parameters with Min and/or Max limits are 100% tested in production at -55°C, +25°C, and +125°C, unless otherwise specified.
2. Typical values shown are not guaranteed.
3. This test is conducted in a closed loop circuit as shown in Figure 6 and includes the error amplifier offset.
4. This specification is included within the Set Point Voltage specification.
5. Compliance to datasheet limits is assured by one or more methods by characterization and/or design.

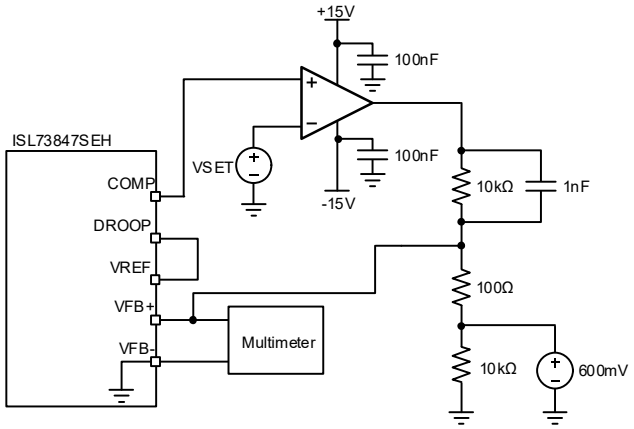


Figure 6. Closed-Loop Circuit

Table 1. Burn-in and Operating Life Test Delta Parameters for the ISL73847SEH

Parameters	Symbol	Conditions	Delta Limits		Limit
			Min	Max	
Shutdown Current 19V	I_{DDSD}	V_{DD} = 19V, EN = GND	-1.5	1.5	µA
Operating Current 19V	I_{DDO}	V_{DD} = 19V	-0.75	0.75	mA
EN Leakage 19V	EN_{LK}	V_{DD} = 19V	-12	12	nA
PG Drive Current 19V	$I_{PG-SINK}$	V_{DD} = 19V	-1.6	1.6	mA
SS Charging I 19V	$I_{SOFTSTART}$	V_{DD} = 19V	-0.5	0.5	µA
SS Charging I 4.5V	$I_{SOFTSTART}$	V_{DD} = 4.5V	-0.5	0.5	µA
ISEN1-I Leak 19V 19V	$I_{LKG-(CSA1)}$	V_{DD} = 19V, V_{CM} = 19V	-0.07	0.07	µA
ISEN2-I Leak 19V 19V	$I_{LKG-(CSA2)}$	V_{DD} = 19V, V_{CM} = 19V	-0.07	0.07	µA
CSA1DROOPI2 0.6V 19V	$Error_{DRP}$	V_{DD} = 19V, V_{CM} = 0.6V	-1.1	1.1	µA
CSA1DROOPI2 5V 19V	$Error_{DRP}$	V_{DD} = 19V, V_{CM} = 5V	-1.1	1.1	µA
CSA2DROOPI2 0.6V 19V	$Error_{DRP}$	V_{DD} = 19V, V_{CM} = 0.6V	-1.1	1.1	µA
CSA2DROOPI2 5V 19V	$Error_{DRP}$	V_{DD} = 19V, V_{CM} = 5V	-1.1	1.1	µA

Table 1. Burn-in and Operating Life Test Delta Parameters for the ISL73847SEH (Cont.)

Parameters	Symbol	Conditions	Delta Limits		Limit
			Min	Max	
PWM1MidSink 19V	V_{OZ1+}	V_{DD} = 19V, I_{PWM1} = +100µA	-0.2	0.2	V
PWM2MidSink 19V	V_{OZ2+}	V_{DD} = 19V, I_{PWM2} = +100µA	-0.2	0.2	V
PWM1MidSource 19V	V_{OZ1-}	V_{DD} = 19V, I_{PWM1} = -100µA	-0.2	0.2	V
PWM2MidSource 19V	V_{OZ2-}	V_{DD} = 19V, I_{PWM2} = -100µA	-0.2	0.2	V
PWM1Vol 19V	V_{OL1+}	V_{DD} = 19V, I_{PWM1} = +500µA	-10	10	mV
PWM2Vol 19V	V_{OL2+}	V_{DD} = 19V, I_{PWM2} = +500µA	-10	10	mV
PWM1Voh 19V	V_{OH1-}	V_{DD} = 19V, I_{PWM1} = -500µA	-0.23	0.23	V
PWM2Voh 19V	V_{OH2-}	V_{DD} = 19V, I_{PWM2} = -500µA	-0.23	0.23	V
OscFS0.5M 19V	$f_{OSC-0.5M}$	V_{DD} = 19V, f_{OSC} = 500kHz	-0.025	0.025	MHz
OscFS3M 19V	f_{OSC-3M}	V_{DD} = 19V, f_{OSC} = 3MHz	-0.16	0.16	MHz
SYNC-I Input Current 19V	$I_{SYNCI-IN}$	V_{DD} = 19V, V_{SYNC} = 5V	-0.32	0.32	µA
SYNC-O Vol 19V	$V_{SYNC-OL}$	V_{DD} = 19V, I_{SYNC-O} = +500µA	-10	10	mV
SYNC-O Voh 19V	$V_{SYNC-OH}$	V_{DD} = 19V, I_{SYNC-O} = -500µA	-0.23	0.23	V

4. Typical Performance Curves

Unless otherwise noted, V_{OUT} = 1V; L_{OUT} = 220nH per phase, C_{OUT} = 2.64mF per phase, C_{DROOP} = 56nF, C_{VREF} = 100nF, R_{DROOP} = 0Ω, R_{FS} = 94.2kΩ, C_{SS} = 22nF, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC}= 1µF, R_{SLP} = 34.8kΩ, C_{SLP} = 100pF, T_A = +25°C

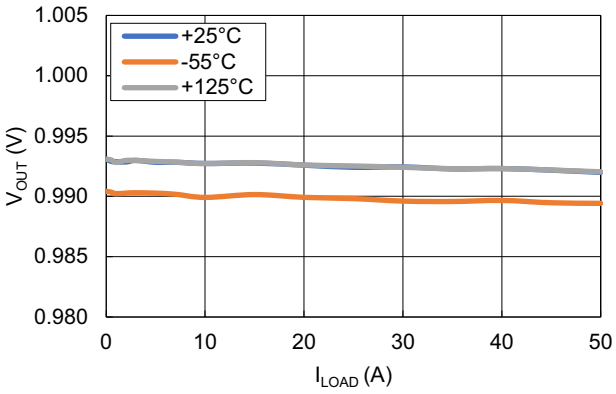


Figure 7. Load Regulation for Various Temperatures (V_{IN} = 5V)

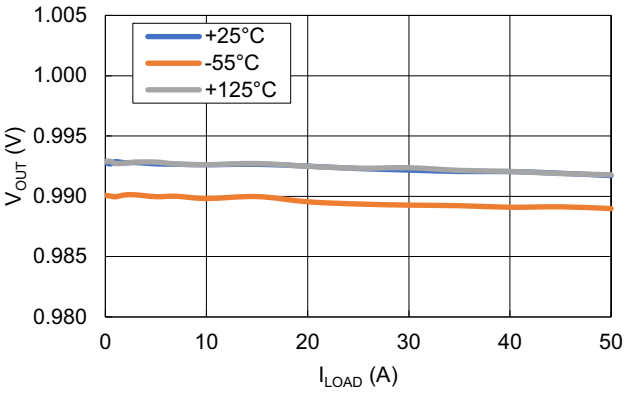


Figure 8. Load Regulation for Various Temperatures (V_{IN} = 12V)

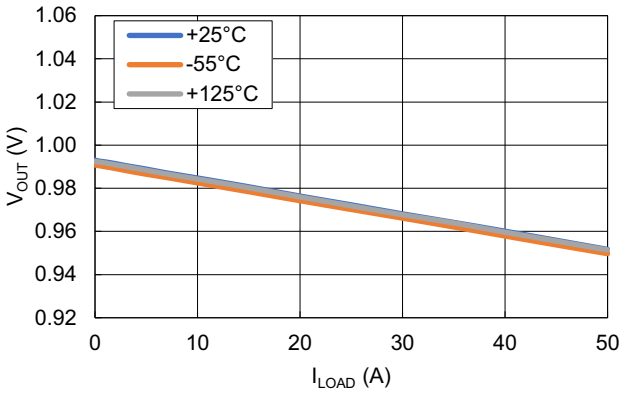


Figure 9. Droop Regulation for Various Temperatures (V_{IN} = 5V, R_{DROOP} = 604Ω)

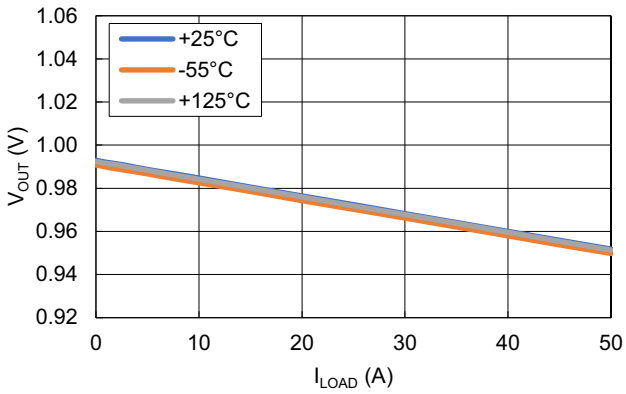


Figure 10. Droop Regulation for Various Temperatures (V_{IN} = 12V, R_{DROOP} = 604Ω)

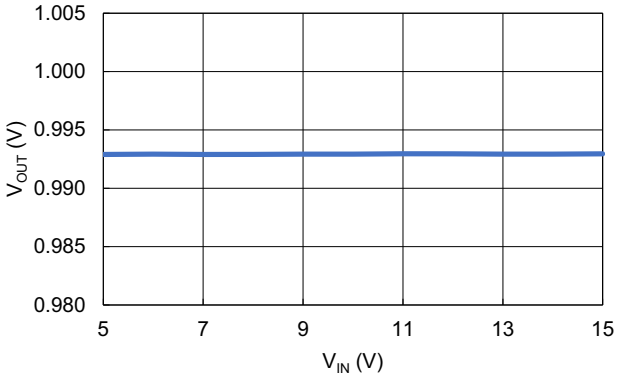


Figure 11. Line Regulation for Various Temperatures (I_{LOAD} = 0A)

Unless otherwise noted, V_{OUT} = 1V; L_{OUT} = 220nH per phase, C_{OUT} = 2.64mF per phase, C_{DROOP} = 56nF, C_{VREF} = 100nF, R_{DROOP} = 0Ω, R_{FS} = 94.2kΩ, C_{SS} = 22nF, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC}= 1µF, R_{SLP} = 34.8kΩ, C_{SLP} = 100pF, T_A = +25°C (Cont.)

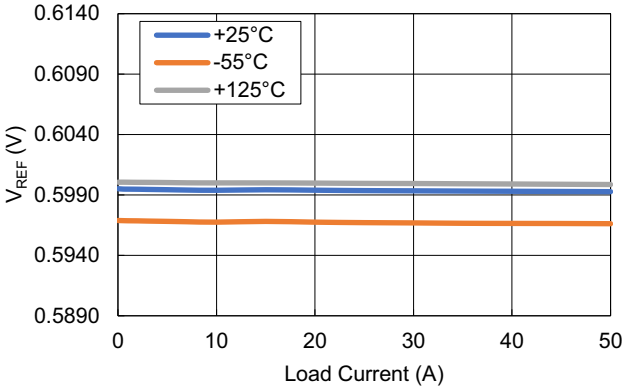


Figure 12. V_{REF} Accuracy for Various Temperatures (V_{IN} = 5V)

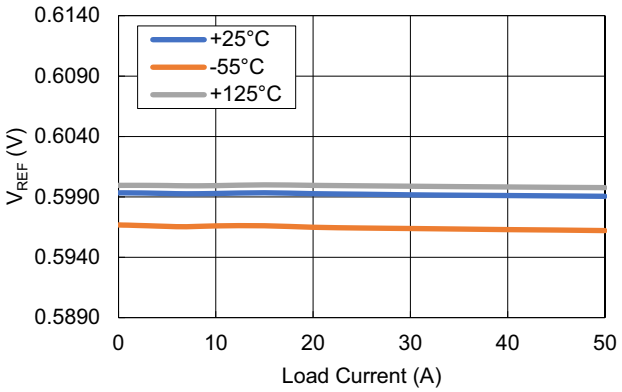


Figure 13. V_{REF} Accuracy for Various Temperatures (V_{IN} = 12V)

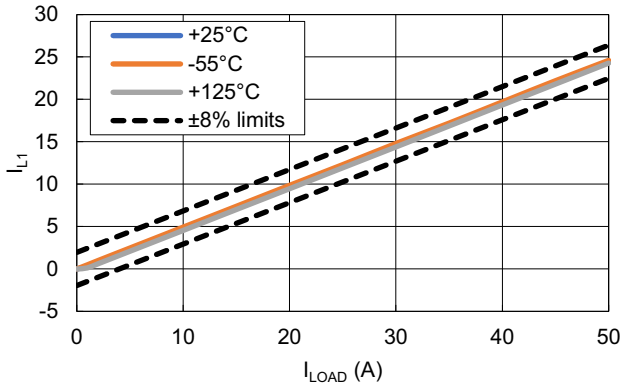


Figure 14. Phase 1 Current Share vs Temperature (V_{IN} = 5V)

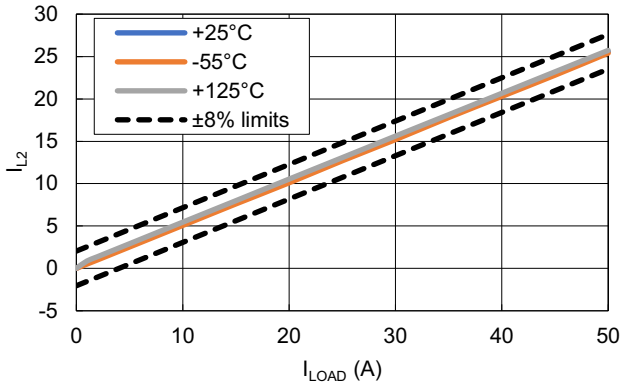


Figure 15. Phase 2 Current Share vs Temperature (V_{IN} = 5V)

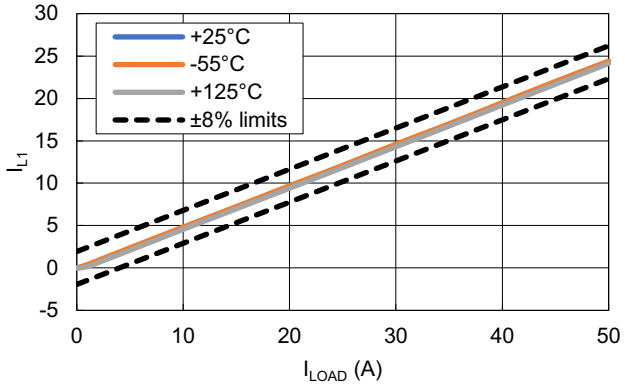


Figure 16. Phase 1 Current Share vs Temperature (V_{IN} = 12V)

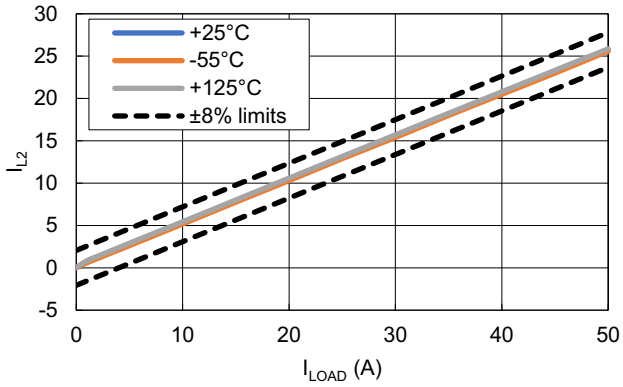


Figure 17. Phase 2 Current Share vs Temperature (V_{IN} = 12V)

Unless otherwise noted, V_{OUT} = 1V; L_{OUT} = 220nH per phase, C_{OUT} = 2.64mF per phase, C_{DROOP} = 56nF, C_{VREF} = 100nF, R_{DROOP} = 0Ω, R_{FS} = 94.2kΩ, C_{SS} = 22nF, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC}= 1µF, R_{SLP} = 34.8kΩ, C_{SLP} = 100pF, T_A = +25°C (Cont.)

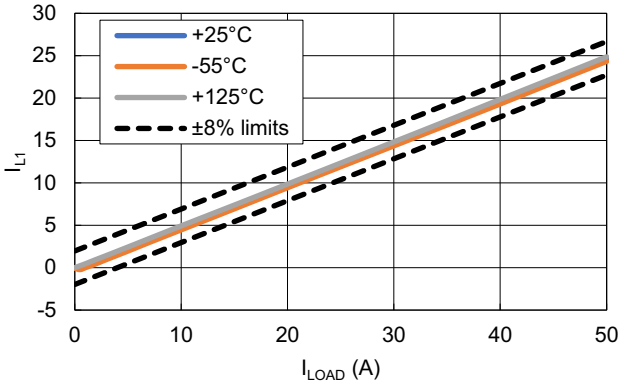


Figure 18. Phase 1 Current Share vs Temperature (V_{IN} = 12V, V_{OUT} = 5V)

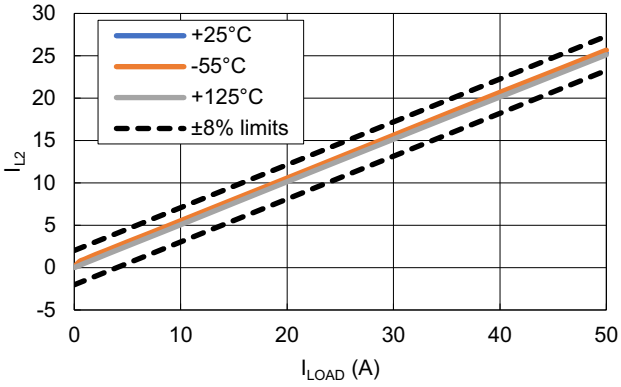


Figure 19. Phase 2 Current Share vs Temperature (V_{IN} = 12V, V_{OUT} = 5V)

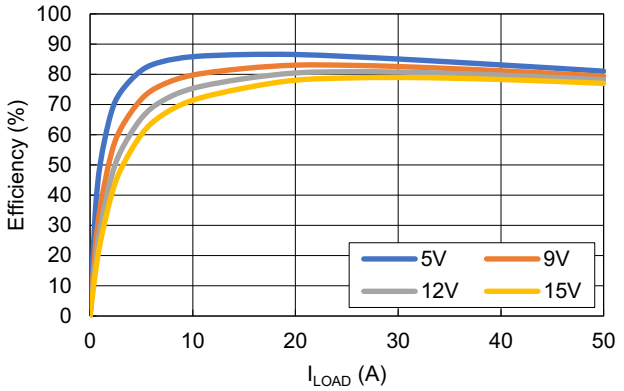


Figure 20. Conversion Efficiency for Various V_{IN} (f_{SW} = 500kHz, ISL70020SEHML, XAL1010-221ME)

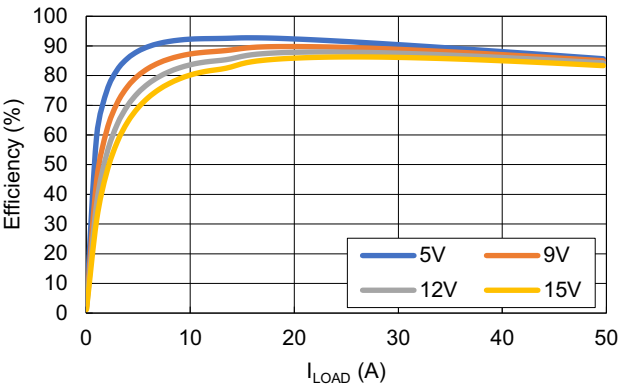


Figure 21. Conversion Efficiency for Various V_{IN} (f_{SW} = 250kHz, ISL70020SEHML, XAL1010-451ME), L_{OUT} = 450nH per phase, C_{OUT} = 5.28mF per phase, C_{COMP} = 15nF, C_{DROOP} = 100nF, R_{FS} = 205kΩ

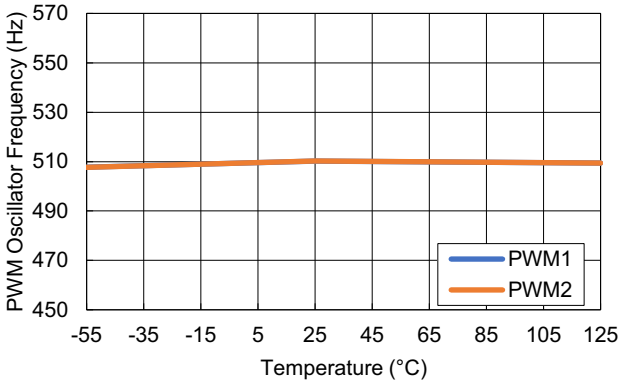


Figure 22. PWMx Frequency vs Temperature (V_{IN} = 12V, I_{LOAD} = 0A, R_{DROOP} = 0Ω)

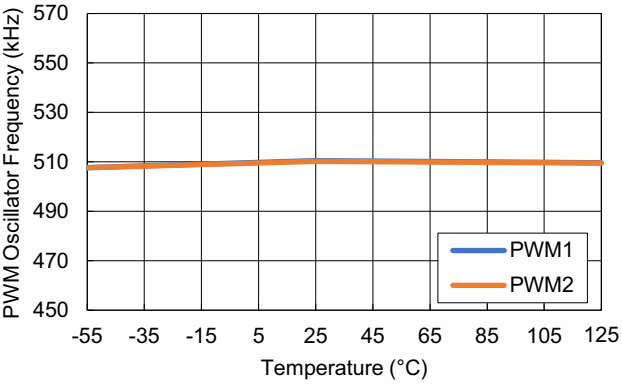


Figure 23. PWMx Frequency vs Temperature (V_{IN} = 12V, I_{LOAD} = 50A, R_{DROOP} = 0Ω)

Unless otherwise noted, V_{OUT} = 1V; L_{OUT} = 220nH per phase, C_{OUT} = 2.64mF per phase, C_{DROOP} = 56nF, C_{VREF} = 100nF, R_{DROOP} = 0Ω, R_{FS} = 94.2kΩ, C_{SS} = 22nF, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC}= 1µF, R_{SLP} = 34.8kΩ, C_{SLP} = 100pF, T_A = +25°C (Cont.)

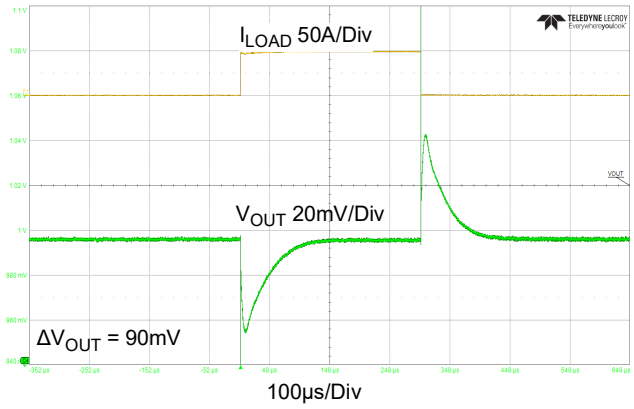


Figure 24. Load Transient Response (V_{IN} = V_{DD} = 5V)

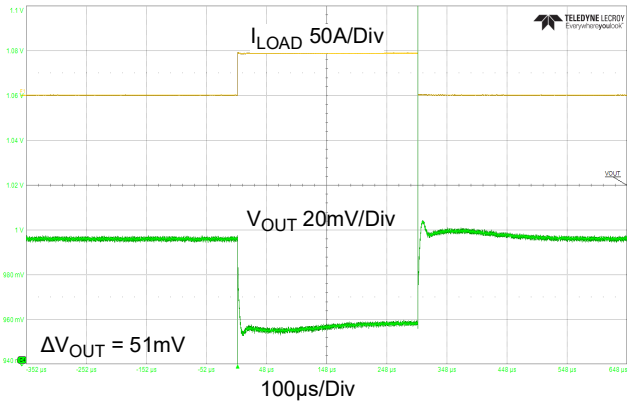


Figure 25. Load Transient Response (V_{IN} = V_{DD} = 5V, R_{DROOP} = 604Ω)

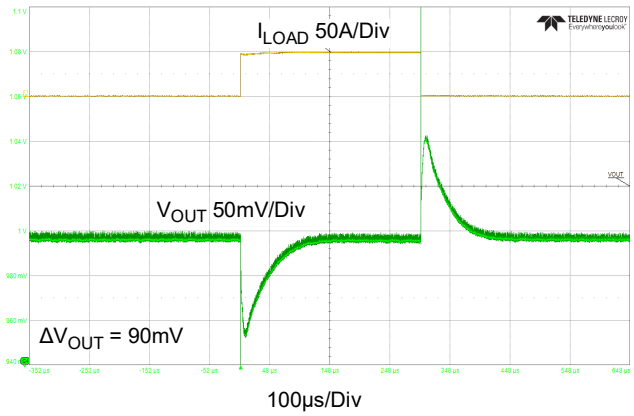


Figure 26. Load Transient Response (V_{IN} = V_{DD} = 12V)

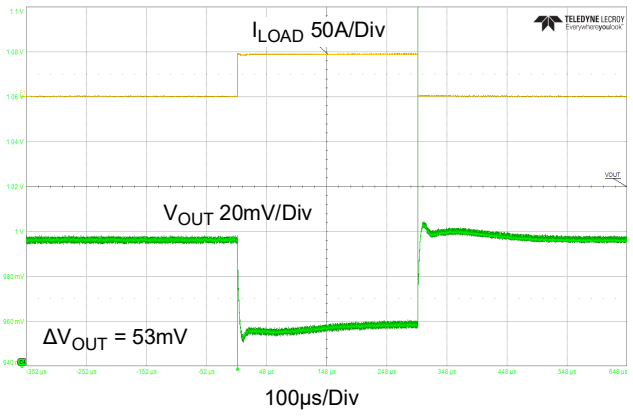


Figure 27. Load Transient Response (V_{IN} = V_{DD} = 12V, R_{DROOP} = 604Ω)

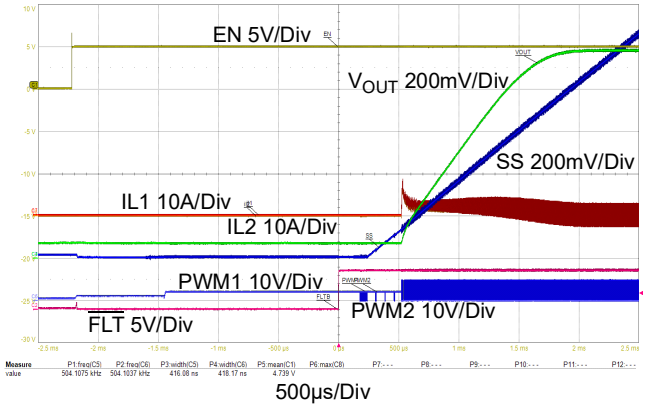


Figure 28. Start-Up with EN (V_{DD} = PVIN = 4.62V, I_{LOAD} = 0A)

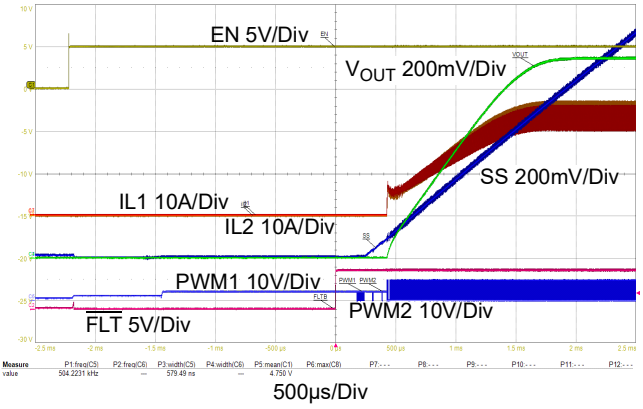


Figure 29. Start-Up with EN (V_{DD} = PVIN = 4.62V, I_{LOAD} = 50A

Unless otherwise noted, V_{OUT} = 1V; L_{OUT} = 220nH per phase, C_{OUT} = 2.64mF per phase, C_{DROOP} = 56nF, C_{VREF} = 100nF, R_{DROOP} = 0Ω, R_{FS} = 94.2kΩ, C_{SS} = 22nF, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC}= 1µF, R_{SLP} = 34.8kΩ, C_{SLP} = 100pF, T_A = +25°C (Cont.)

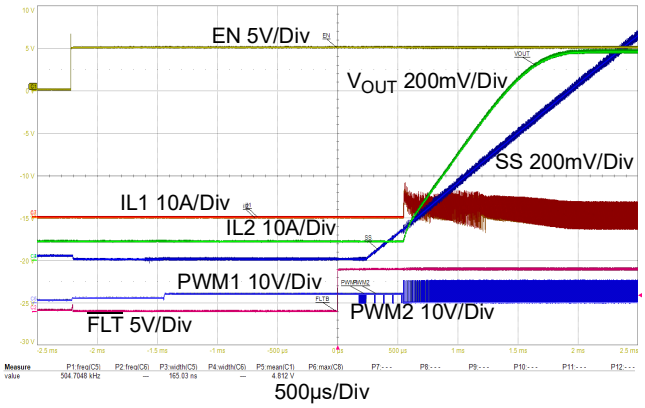


Figure 30. Start-Up with EN (V_{DD} = PVIN = 12V, I_{LOAD} = 0A

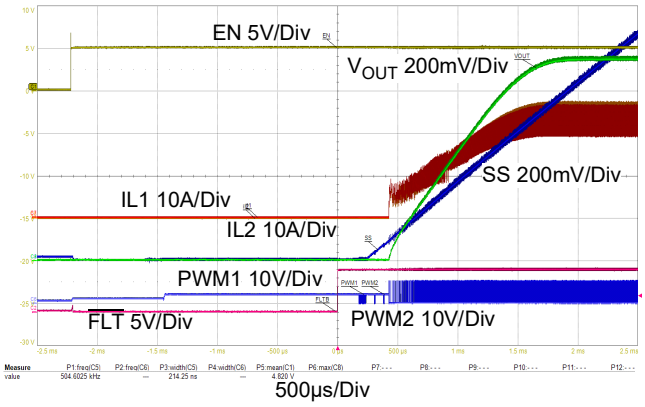


Figure 31. Start-Up with EN (V_{DD} = PVIN = 12V, I_{LOAD} = 50A

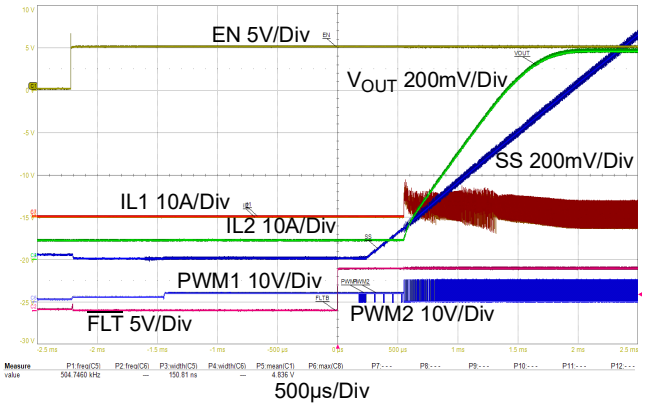


Figure 32. Start-Up with EN (V_{DD} = PVIN = 13.2V, I_{LOAD} = 0A

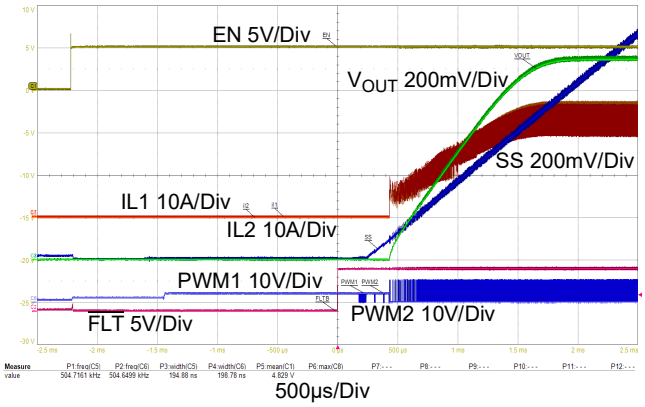


Figure 33. Start-Up with EN (V_{DD} = PVIN = 13.2V, I_{LOAD} = 50A

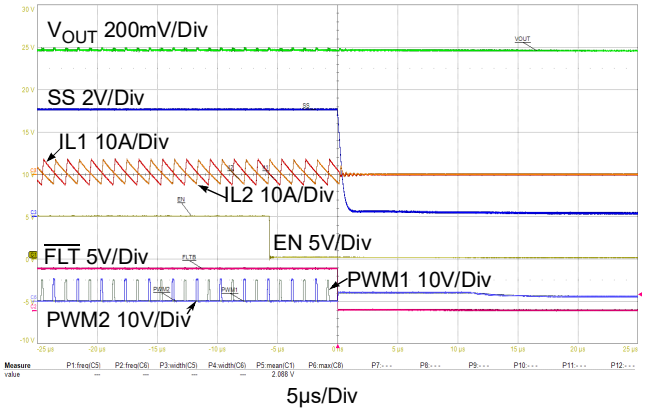


Figure 34. Shutdown with EN (V_{DD} = PVIN = 12V, I_{LOAD} = 0A

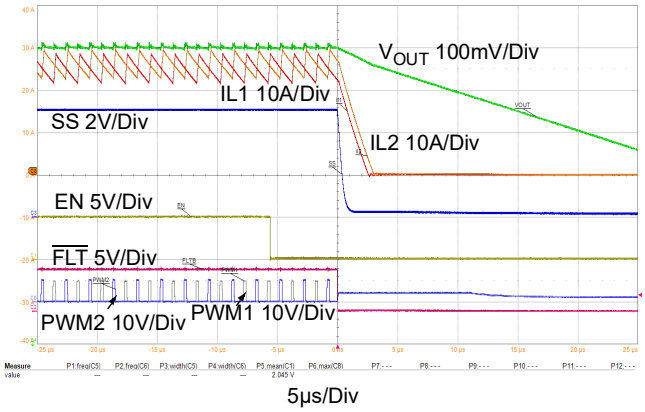


Figure 35. Shutdown with EN (V_{DD} = PVIN = 12V, I_{LOAD} = 50A

Unless otherwise noted, V_{OUT} = 1V; L_{OUT} = 220nH per phase, C_{OUT} = 2.64mF per phase, C_{DROOP} = 56nF, C_{VREF} = 100nF, R_{DROOP} = 0Ω, R_{FS} = 94.2kΩ, C_{SS} = 22nF, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC}= 1µF, R_{SLP} = 34.8kΩ, C_{SLP} = 100pF, T_A = +25°C (Cont.)

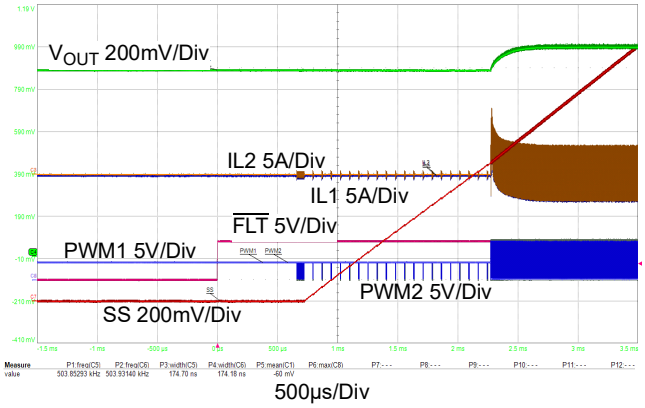


Figure 36. Pre-Biased Start-Up (V_{DD} = 4.62V, PVIN = 12V, I_{LOAD} = 0A, Vpre-bias = 900mV

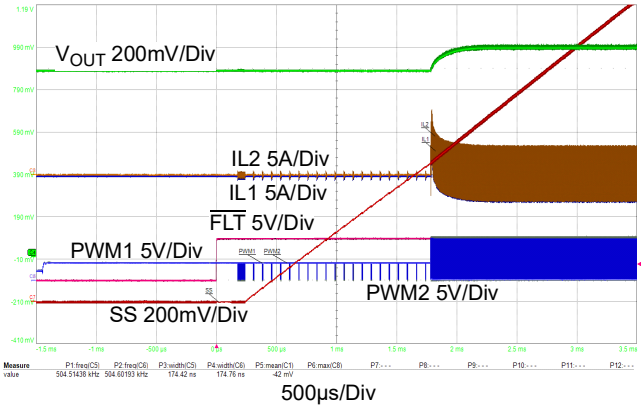


Figure 37. Pre-Biased Start-Up (VDD = PVIN = 12V, I_{LOAD} = 0A, Vpre-bias = 900mV

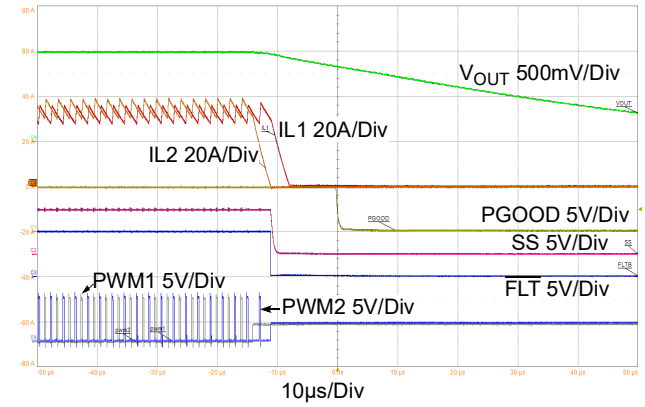


Figure 38. Overcurrent Protection (V_{IN} = 12V, V_{DD} = 5V)

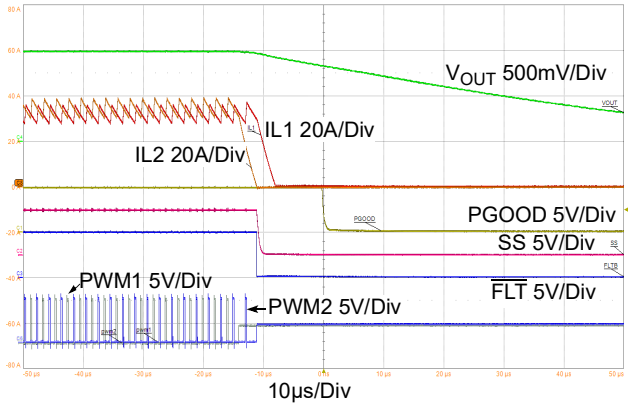


Figure 39. Overcurrent Protection (V_{IN} = V_{DD} = 12V)

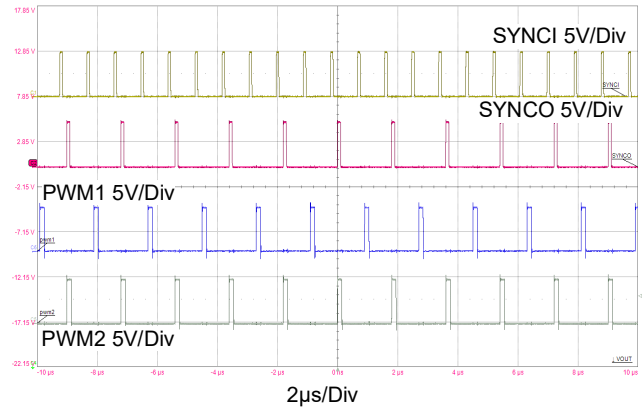


Figure 40. Sync (V_{DD} = 5V, V_{IN} = 12V, RSYNC-O = 100kΩ to VCC)

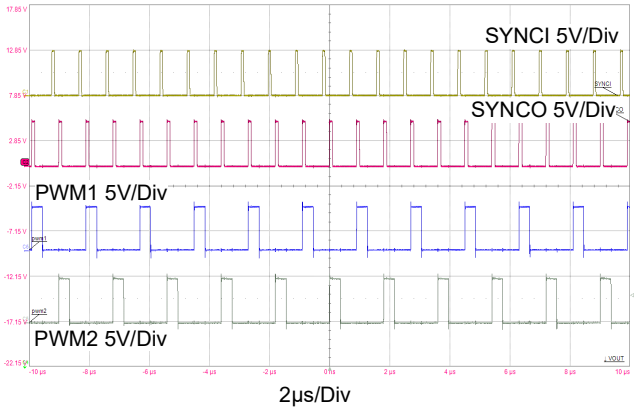


Figure 41. Sync (V_{DD} = 5V, V_{IN} = 12V, RSYNC-O = 100kΩ to GND)

Unless otherwise noted, V_{OUT} = 1V; L_{OUT} = 220nH per phase, C_{OUT} = 2.64mF per phase, C_{DROOP} = 56nF, C_{VREF} = 100nF, R_{DROOP} = 0Ω, R_{FS} = 94.2kΩ, C_{SS} = 22nF, C_{COMP} = 8.2nF, R_{COMP} = 4.22kΩ, C_{POLE} = 330pF, C_{VCC}= 1µF, R_{SLP} = 34.8kΩ, C_{SLP} = 100pF, T_A = +25°C (Cont.)

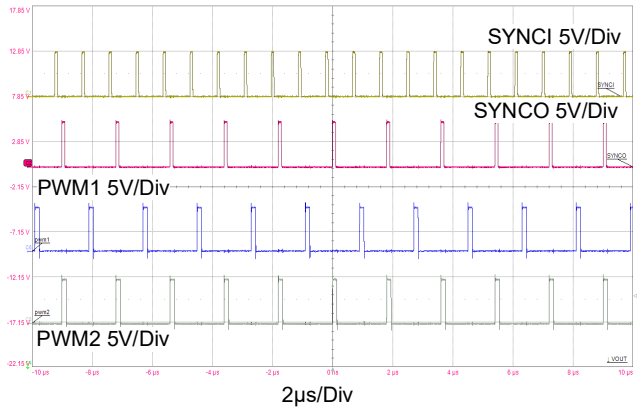


Figure 42. Sync (V_{DD} = 12V, V_{IN} = 12V, RSYNC-O = 100kΩ to VCC)

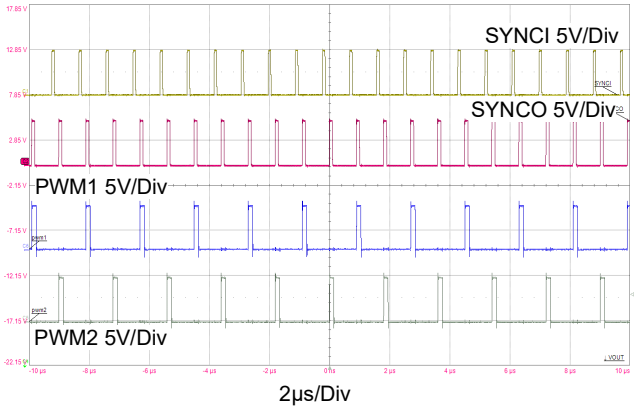


Figure 43. Sync (V_{DD} = 12V, V_{IN} = 12V, RSYNC-O = 100kΩ to GND)

5. Operational Description

5.1 Dual Phase Operation

The ISL73847SEH has the ability to operate in single-phase or dual-phase mode. The part is configured to work in dual-phase mode by default. To operate the in single-phase mode, short the PWM output to VCC. Either PWM1 or PWM2 can be chosen for single-phase operation so long as the other is shorted to VCC. The flexibility of using either output in single-phase can help during layout as it may be easier to route the current-sense feedback signals to one channel or the other.

5.2 Oscillator and Clock Synchronization

The switching frequency of the controller is determined by a resistor to ground on the FS pin (R_{FS}). The ISL73847SEH is capable of operating with an oscillator frequency in the range of 500kHz to 3MHz. If the FS pin is shorted to ground, the ISL73847SEH reads this as a fault and stops switching.

5.2.1 External Synchronization (SYNC-I)

The ISL73847SEH has a SYNC-I pin that allows synchronizing it to an external clock. To use this functionality, it is necessary to set the internal oscillator to 15% less than the required frequency of the external oscillator. This ensures that if the sync input frequency stops at any point in time, the internal oscillator takes over and continues operating. The allowable frequency range for the external clock is 588kHz to 3MHz. The SYNC-I frequency should be twice the required PWM switching frequency. *Note:* The maximum input SYNC frequency should not be greater than the maximum oscillator frequency.

5.2.2 Clock Output (SYNC-O)

The ISL73847SEH has a SYNC-O pin that can output either the oscillator frequency or the PWM switching frequency. To output the oscillator frequency, place a 100kΩ resistor on the SYNC-O pin to ground. To output the PWM switching frequency, place a 100kΩ resistor on the SYNC-O pin to VCC. The choice to use one or the other depends on what is receiving the clock pulse. If the clock output is being used to synchronize another ISL73847SEH, it expects a frequency that is twice the PWM switching frequency (load the pin with 100kΩ). Other PWM regulators such as the ISL7000xSEH family of parts switch at the same frequency as the incoming frequency (tie with 100kΩ to VCC). When SYNC-O is unloaded, it is in phase with PWM2. During a fault condition, the SYNC-O is asserted low.

5.3 Remote Sensing

The ISL73847SEH has the ability to provide differential remote sensing. This allows for the power stage to reside close to the point of load and having the controller further away to reduce the possibility of noise injection because of switching noise from the power stage. In this configuration, the remote sensing also allows the ISL73847SEH to compensate for any loss along the copper planes carrying large currents.

5.4 Droop Regulation

Droop regulation can minimize transient voltages on the regulated output during large load steps. It works by lowering the output voltage as the load current increases, effectively increasing the DC output impedance for the power supply.

Droop is tuned by adding a resistor between VREF and DROOP. The ISL73847SEH sinks a current on DROOP that is proportional to the sum of the differential voltage across both current sense inputs. This current through the resistor between VREF and DROOP changes the reference voltage presented to the error amplifier, thereby changing the DC regulation point. The larger the resistor, the greater the variation in regulated voltage with respect to the load current.

5.5 Peak Current Mode Control

The ISL73847SEH uses peak current mode regulation by presenting the current-sense signal directly to the PWM comparator. The current-sense amplifier has a minimum bandwidth of 10MHz, allowing it to keep up with the ripple current through the inductor. The PWM pulse is terminated when the current crosses the error amplifier output.

5.6 Tri-State PWM Control

The ISL73847SEH features a tri-level PWM output that can output a low-level, high-level, and mid-level voltage. The high-level output turns on the high-side FET, while a low-level output turns on the low-side FET, and the mid-level output turns off both the high-side and low-side FETs. This state is helpful during fault conditions where you want to protect any downstream devices and the power stage. Connect a 100kΩ resistor on PWM1 and PWM2 to GND.

The ISL73847SEH works with drivers that accept a tri-level input, like the ISL73041SEH.

5.7 Boot Refresh

When the ISL73847SEH first powers up before soft-start, it issues a boot refresh command that consists of 32 mid-to-low transitions on the PWM output, allowing sufficient time for the boot capacitor to charge up. The frequency of the boot refresh pulses is determined by the switching frequency and the pulse is equal to the minimum on-time (t_{MIN_ON}). Using the frequency and pulse widths, an appropriate boot capacitor value can be determined.

Whenever the ISL73847SEH is tri-stated it starts an analog timer that lasts 60µs ±60% (tolerance because of process and part-to-part variation). If the timer completes before the next high-level signal, four additional boot refresh pulses are transmitted to ensure the boot voltage is replenished. This would be the case in a pre-biased startup, where there could be a significant amount of time between the boot refresh pulses and the first high-side signal.

5.8 Current Sense Amplifiers and Current Monitoring (IMON)

The ISL73847SEH uses 10MHz (minimum) transconductance amplifiers for each phase to achieve peak current control by sensing the inductor current continuously. Current sensing can be accomplished using a shunt resistor on the output side of the inductor or through inductor DCR sensing. Shunt sensing provides high precision accuracy at the cost of power dissipation while DCR current sensing has little power dissipation because of indirectly senses the inductor current. Its drawbacks include reduced accuracy across the operating temperature

range and the inability to sense when an inductor is saturating; therefore, soft saturation inductors are recommended in this case.

The ISL73847SEH has an IMON pin that monitors the current through the power supply for telemetry purposes. Connect a resistor from the IMON pin to GND. In this configuration, the IMON pin reflects the average of the inductor ripple current. An additional capacitor in parallel with the resistor can be used to improve averaging. The size of the capacitor needed to average the current depends on the ripple seen on the IMON pin.

5.9 Adjustable Slope Compensation

As the ISL73847SEH is a peak current mode controller, it is prone to subharmonic oscillations when the duty cycle is greater than 50%. By adding a compensating ramp equal to the down slope of the inductor current, any subharmonic oscillation can be damped within 1 switching cycle. If the nominal duty is under but close to 50%, Renesas recommends using adequate slope compensation as the duty cycle could cross 50% as the load increases. The slope compensation depends on the SLOPE pin and the FS pin.

If slope compensation is not enough, the converter can experience subharmonic oscillation that could result in noise emissions at half the switching frequency. However, too much slope compensation can deteriorate the phase margin; therefore, the slope compensation must be carefully considered.

5.10 Pulse Skipping

The ISL73847SEH has the ability to skip pulses if the feedback indicates that the minimum pulse width is excessive. One scenario where this can arise would be during a load release when operating close to the minimum on-time. Pulse skipping reduced the overshoot during the unloading in a transient step.

5.11 VDD and VCC Range

The ISL73847SEH has an internal LDO that provides the bias for all internal circuitry. The input of the LDO is VDD, which accepts a range of 4.5V up to 19V. VCC is the output of the LDO which regulates 5V. When VDD is operating in the range of 4.5V to 5.0V, VCC tracks VDD minus the dropout.

5.12 Enable

The ISL73847SEH features a 2-stage enable. When enable is at 1V (gross threshold), the internal circuitry is biased (such as reference voltage, oscillator, and logic) but switching is disabled. When the voltage of EN crosses the fine threshold, switching is enabled and the IC attempts a boot refresh and soft-start. Because of filtering for Single Event Effects (SEE), the EN logic state (high or low) must persist for at least 80µs for the part to recognize it and respond. The enable pin has a pull down that disables the part if the pin is not actively driven.

5.13 Initialization and Startup

When the ISL73847SEH first powers up, it goes through several states before boot refresh and soft-start. After VDD has crossed the rising UVLO threshold, the oscillator waits 128 clock cycles at 500kHz before allowing the digital core to enter its configuration state. The configuration state lasts 886 clock cycles at 500 kHz. When the digital core completes it configuration, it signals the oscillator to switch to the frequency set by the FS pin or

SYNC-I. After an additional 128 clock cycles at the new frequency, boot refresh pulses commence followed by soft-start. Figure 44 and Figure 45 illustrate the start-up sequence.

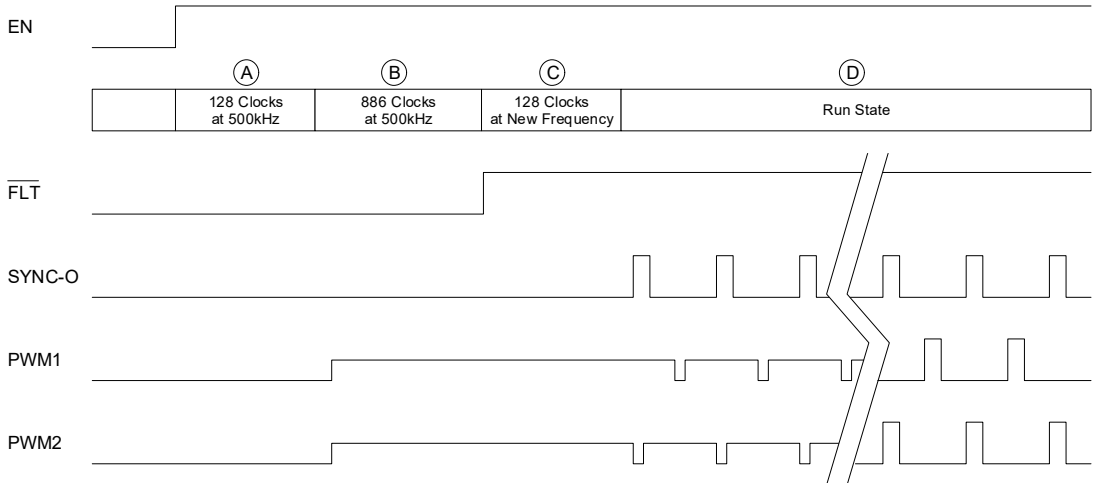


Figure 44. Start-Up Timing Diagram (R_{SYNC-O} = OPEN)

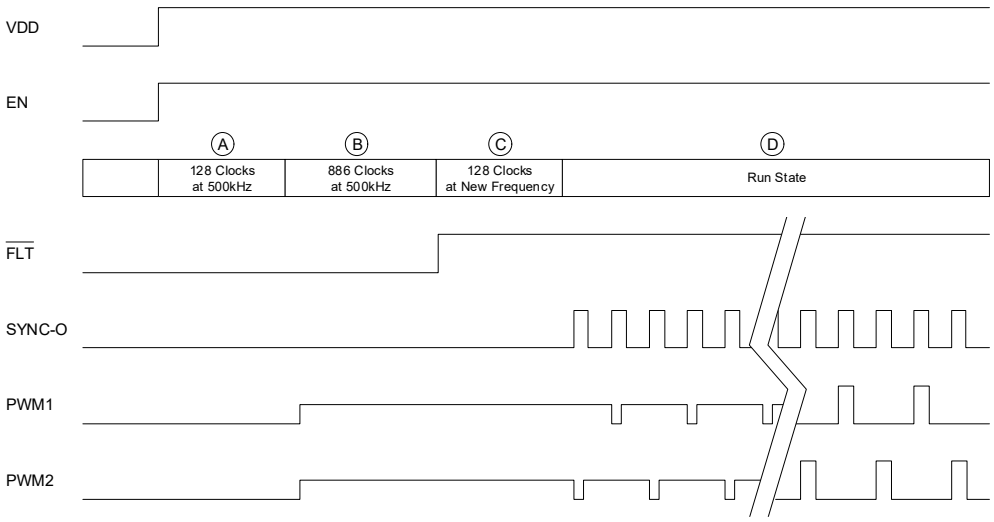


Figure 45. Start-Up Timing Diagram (R_{SYNC-O} = 100kΩ)

During states A and C in Figure 44 and Figure 45, the oscillator blanks the clock signal to the digital core. This is done so that the oscillator has time to stabilize its frequency before entering the configuration state (B) or run state (D). *IMPORTANT:* During states A and C the digital core does not receive a clock; therefore, it is not able to detect a rising edge on EN. Rather the EN signal must persist long enough so that the digital core can read it during states B and D. The ISL73847SEH reacts to a falling edge on EN regardless of what state the controller is in.

5.14 Hiccup

Any time the ISL73847SEH encounters a fault, it enters hiccup. During hiccup, the controller waits 1 soft-start cycle before attempting to start switching again. If the fault has not cleared after the dummy soft-start cycle has completed, the ISL73847SEH continues to wait until it clears and then starts the PWM switching. This would be the case if the fault that tripped was the driver pulling $\overline{FLT}$ low because of an over-temperature fault.

If an output short occurs, the part would hiccup, go through a dummy soft-start cycle, and attempt start up indefinitely until the output short is removed. In this case, as soon as the part starts switching, it would trip the gross overcurrent threshold and go back to hiccup. When the output short is removed, normal operation resumes after the configuration sequence which is 886 clock cycles at 500kHz.

5.15 Fault Handling

5.15.1 Cycle-by-Cycle Current Limit

The current flowing through the inductor is monitored through the current-sense inputs using a sense resistor or DCR sensing. When the input reaches the current limit threshold (V_{PCL}), the PWM pulse is terminated to limit the peak current. A single cycle-by-cycle current limit event does not trigger hiccup but if there are four current limit events in an eight clock cycle window, the ISL73847SEH enters hiccup.

5.15.2 Inductor Peak Overcurrent Protection

If the output current increases even after triggering the cycle-by-cycle current limit, the ISL73847SEH has a second overcurrent protection (V_{POC} and V_{NOC}). If triggered, it drives the PWM outputs to mid-level (tri-state the power stage) and enters hiccup. If the initial fault continues to persist or another fault occurs during the next soft-start, the cycle repeats indefinitely and stays in hiccup. The overcurrent protection protects against both positive and negative overcurrent conditions.

5.15.3 Overvoltage and Undervoltage Fault

The ISL73847SEH has overvoltage and undervoltage protection that is triggered when $V_{(FB, OV)}$ or $V_{(FB, UV)}$ are exceeded. If the $V_{(FB, OV)}$ or $V_{(FB, UV)}$ levels are reached, the part enters hiccup.

5.15.4 $\overline{\text{FLT}}$ Pin

The $\overline{\text{FLT}}$ pin is a bi-directional communication pin between the ISL73847SEH controller and the ISL73041SEH driver. On the ISL73847SEH, the $\overline{\text{FLT}}$ pin is low and is an I/O when the part is not ready (during startup) or when it encounters a fault. The ISL73041SEH uses this pin to communicate if it is not ready to accept input or encountered a fault on its end. In either case, if the $\overline{\text{FLT}}$ pin is pulled low by the ISL73041SEH, the ISL73847SEH tri-states the output (mid level) and enters hiccup. The $\overline{\text{FLT}}$ pin is an input while switching (during and after startup).

5.15.5 Oscillator and Sync Input Fault

If the FS pin is inadvertently shorted to ground, this causes a fault in the controller and switching would be inhibited.

The ISL73847SEH has the ability to synchronize to an external frequency. If the external clock is not present or if the internal clock frequency is not less than 15% of the required external clock frequency, the part reverts to the internal oscillator and continues operation. When the external sync input returns or if the internal clock frequency is less than 15% of the required external clock frequency, the ISL73847SEH immediately switches back to the external clock, as shown in Figure 46.

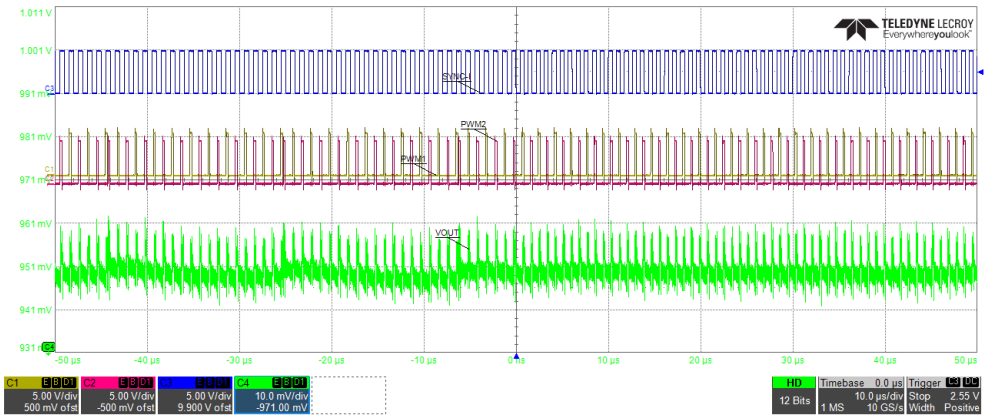


Figure 46. Switching between Internal Oscillator and External Oscillator on SYNC-I (External clock frequency changed from 1MHz to 1.15MHz)

While switching between the internal and external oscillator, there may be a glitch observed on the regulated output. The size of this glitch depends on the frequency difference between the internal and external clock, output capacitance, and output loading.

To ensure that this fail safe works accordingly, the internal oscillator must be configured to operate 15% slower than the minimum external frequency applied to the SYNC-I pin. Setting the internal oscillator to a frequency that is too close to the external sync frequency can result in the clock output alternating between the internal and external clock, resulting in a beat frequency.

If the SYNC-I function is not needed, leave the pin floating as it has an internal pull down. If whatever is driving the SYNC-I pin gets stuck in either a logic high or low and as long as there are no transitions, the ISL73847SEH reverts back to the internal oscillator.

6. Applications Information

6.1 PWM Switching Frequency Selection

The PWM switching frequency is half the frequency of the oscillator. It is determined based on the requirements of transient response time, solution size, power dissipation, ripple voltage, and input and output voltage range. Increasing the switching frequency improves the transient response and solution size but its trade off is increased switching losses. A balance needs to be reached between these parameters to decide the optimal switching frequency.

When the switching frequency is determined, the FS resistor (frequency setting resistor) can be determined by using Equation 1. The use of precision resistors is recommended to set the oscillator frequency as variations in the resistor increases the oscillator frequency spread.

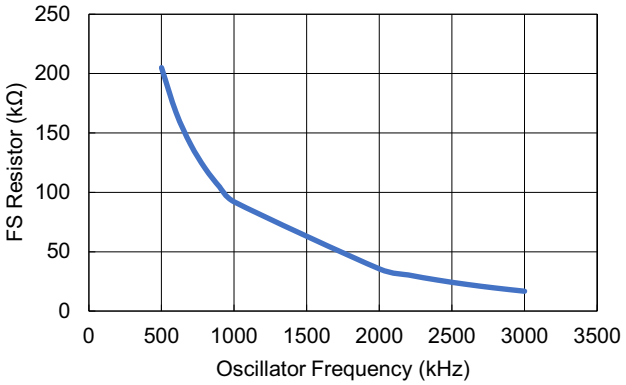


Figure 47. R_{FS} vs Frequency

The oscillator frequency is determined by a resistor to ground on the FS pin where R_{FS} is in ohms (Ω) and f_{OSC} is the oscillator frequency in hertz (this should be twice the PWM switching frequency).

(EQ. 1) $$R_{FS} = 4.5095 \times 10^{12} \bullet f_{OSC}^{-1.2828}$$

IMPORTANT: Equation 1 is an approximation of the real data presented in Figure 47. The data used for Figure 47 is a typical and there is some variation because of temperature and variation. This variation is shown in the electrical specifications table by providing four fixed resistors and the frequency and tolerance achieved with those resistors.

6.2 Output Voltage Setting

The output voltage can be set to the required regulated voltage by using the following Equation 2.

(EQ. 2) $$V_{OUT} = V_{REF} \times \left(1 + \frac{R_2}{R_1}\right)$$

where:

- V_{OUT} is the required regulated voltage
- V_{REF} is the internal reference voltage on the VFB+ pin, which is 0.6V (typical)
- R_1 is the bottom resistor in the feedback divider
- R_2 is the top resistor in the feedback divider

6.3 Resistor Current Sensing and Monitoring Setting

The ISL73847SEH has the ability to sense current either through a shunt resistor or through DCR sensing. Equation 3 can determine what the shunt resistance or minimum DCR of the inductor needs to be. Depending on what PVIN, VOUT and $I_{OUT(MAX)}$ is, DCR sensing might not be practical. For example, in a high current and low output voltage application, it might not be possible to get an inductor that meets both the minimum DCR requirement and the saturation current capability. In this case, shunt sensing is the only option.

(EQ. 3) $$R_{SEN} = \frac{50mV \times n}{I_{OUT(MAX)}}$$

where:

- R_{SEN} is the sense resistor or minimum DCR of the inductor in milliohms (mΩ)
- n is the number of phases
- $I_{OUT(MAX)}$ is the max DC output current for all phases

It is necessary to add RC filters for both the sense resistor and DCR sensing. In the case of the sense resistor, it is to compensate for the parasitic inductance, Equation 4 shows how to calculate the RC filter if the resistance and parasitic inductance of the sense resistor are known. For DCR sensing, the RC filter has to be properly selected such that the voltage across the cap is proportional to the current through the inductor.

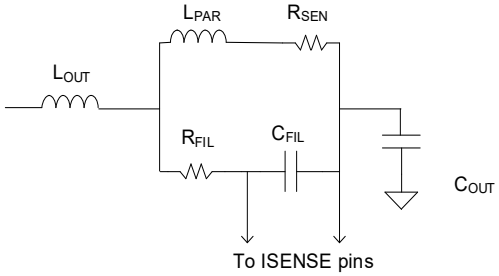


Figure 48. R_{SEN} Parasitic Inductance Compensation RC Circuit

(EQ. 4) $$\frac{L_{PAR}}{R_{SEN}} = R_{FIL} \times C_{FIL}$$

where:

- R_{FIL} is the resistance of resistor in the RC filter.
- C_{FIL} is the capacitance of capacitor in the RC filter.
- R_{SEN} is the sense resistor in mΩ from Equation 3.
- L_{PAR} is the parasitic inductance in Henries (H) of R_{SEN}.

The ISL73847SEH continuously monitors the inductor current of each phase. The IMON pin outputs a current proportional to the summation of current from all phases.

(EQ. 5) $$I_{MON} = \sum_{n=1}^{2} R_{SEN} \times I_{Ln} \times g_{m(CSA, IMON)}$$

where:

- I_{MON} is current out of the IMON pin in µA
- R_{SEN} is the sense resistor in mΩ calculated from Equation 3
- I_{Ln} is the inductor current for a given phase in amps, where n is the phase number
- $g_{m(CSA, IMON)}$ is the transconductance from the input of the current sense amp to the IMON pin in µA/mV

6.4 DCR Current Sensing

The DCR method of current sensing in a buck converter uses the DC resistance of the inductor winding as the current sense element. This eliminates the need for a sense resistor and improves the efficiency. The inductor DCR does vary based on the temperature coefficient of the selected winding material such as Cu. However, these variations are not quite as wide as that of using a MOSFET for $r_{DS(ON)}$ sensing. This method is used more often in low output voltage converters as any voltage drop on a sense resistor negates from the low output voltage. A resistor and capacitor in series is placed in parallel with the inductor. The typical application circuit for a dual phase is shown in Figure 49.

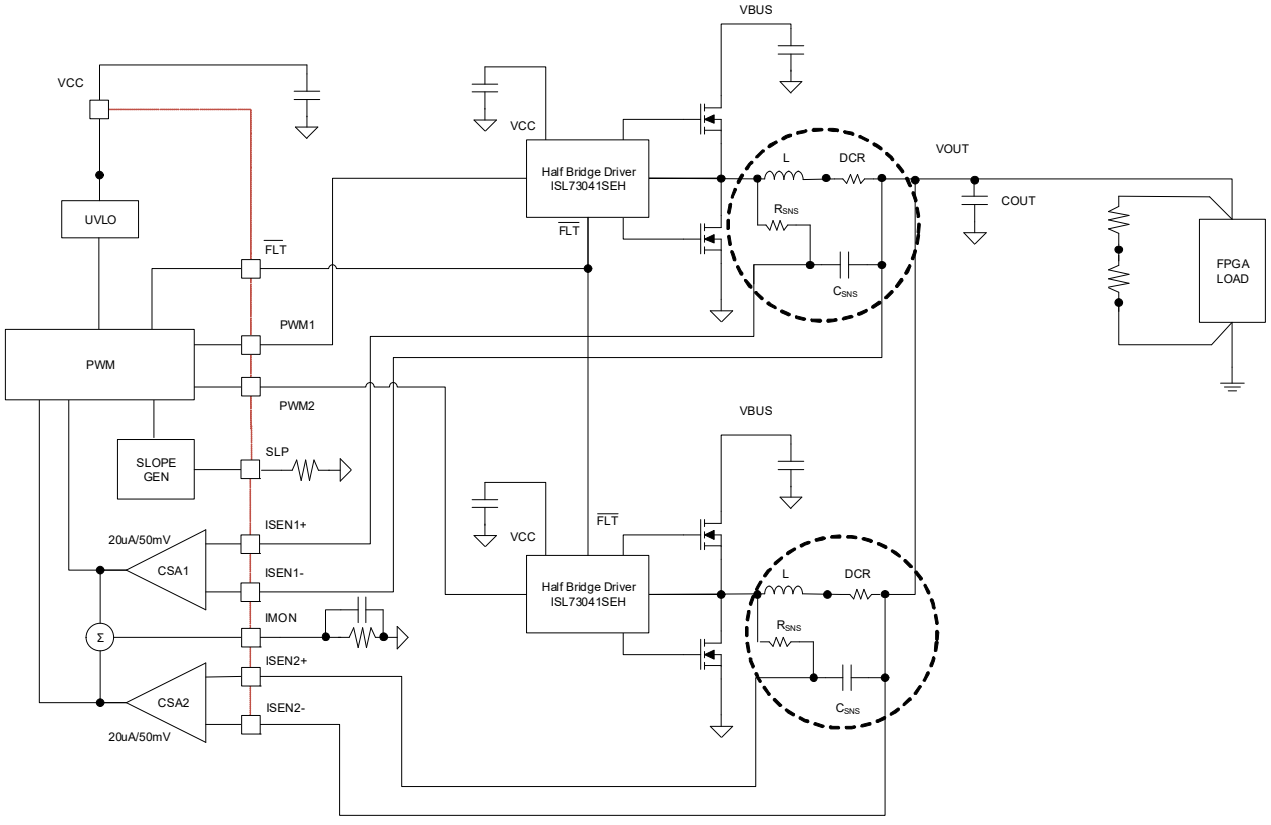


Figure 49. DCR Current Sensing

The component values can be calculated based on Equation 6:

(EQ. 6) $$\frac{L}{DCR} = R_{SNS} \times C_{SNS}$$

where:

- L is the output inductor value
- DCR is DC resistance of inductor winding
- R_{SNS} is the resistor value selected for DCR sensing
- C_{SNS} is the capacitor value selected for DCR sensing

DCR sensing requires that the selected value of $R_{SNS} \times C_{SNS}$ should satisfy the time constant per Equation 6 In which case, the voltage developed across C_{SNS} is proportional to the inductor current and the voltage is given by:

(EQ. 7) $$VC_{SNS} = I_L \times DCR$$

where:

- I_L is the inductor current
- DCR is DC resistance of inductor winding
- VC_{SNS} is the voltage developed across the capacitor C_{SNS}

6.5 Inductor Selection

To select the proper inductance value, you need to determine your input voltage, output voltage, switching frequency, and inductor ripple current. In general, the inductor ripple current is recommended to be 30% of the I_{OUT}. Designing with less ripple current reduces the output voltage ripple but comes at the expense of slower transient response. Therefore, the amount of ripple that is acceptable would need to be decided on a per application basis.

A good first pass estimate for the inductor size can be calculated using Equation 8.

(EQ. 8) $$L_{REC} = \frac{(V_{IN} - V_{OUT}) \times D}{f_{SW} \times \Delta I_L}$$

where:

- L_{REC} is the recommended inductance in Henries
- V_{IN} is the input voltage to the power supply in volts
- V_{OUT} is the output voltage of the power supply in volts
- D is the duty cycle, for a buck converter it is (V_{OUT}/V_{IN})
- f_{SW} is the switching frequency of the power supply in hertz
- ΔI_L is the expected ripple current for the inductor in amps

The adjustable slope compensation pin has a voltage range of 0.3V to 1.2V. The minimum inductance that corresponds to a slope voltage of 1.2V (R_{SLOPE} = 100kΩ) can be calculated using Equation 11.

(EQ. 9) $$R_{CSA} = \frac{0.4}{I_{OUT(MAX)}}$$

(EQ. 10) $$RAMP_{MAX} = \frac{0.4}{f_{SW} \times 1.85 \times 10^{-11} \times R_{FS}}$$

(EQ. 11) $$L_{MIN} = \frac{V_{OUT} \times R_{CSA} \times n}{f_{SW} \times RAMP_{MAX}}$$

where:

- L_{MIN} is the minimum inductance needed to prevent subharmonic oscillations
- V_{OUT} is the output voltage of the power supply
- $I_{OUT(MAX)}$ is the total load current for all active phases
- n is the number of active phases (for the ISL73847SEH this is either 1 or 2)
- f_{SW} is the switching frequency of the power supply in hertz
- R_{FS} is the resistor on the FS pin determined by Equation 1

The maximum inductor value corresponding to a slope voltage of 0.3V (R_{SLOPE} = 25kΩ) is:

(EQ. 12) $$L_{MAX} = L_{MIN} \times 4$$

where:

- L_{MIN} is the minimum inductance needed to prevent subharmonic oscillations in Henries
- L_{MAX} is the maximum inductance needed to prevent subharmonic oscillations in Henries

Using a value lower than what is calculated in Equation 11 might result in subharmonic oscillations, for this reason Renesas recommends staying above it. Exceeding the maximum inductance value results in reduced phase margin and outer loop instability as the sensed ripple current would be much smaller than the compensation ramp.

6.6 Slope Compensation

The slope compensation resistor is calculated using Equation 13:

(EQ. 13) $$R_{SLOPE} = \frac{L_{MIN}}{L_{SEL}} \times 100k\Omega$$

where:

- R_{SLOPE} is the slope compensation resistor in kΩ
- L_{MIN} is the minimum inductance needed to prevent subharmonic oscillations in Henries
- L_{SEL} is the user selected output inductance between L_{MIN} and L_{MAX} in Henries

6.7 Error Amplifier Compensation and Output Capacitance

The error amplifier is a transconductance amplifier that makes it much easier to compensate by placing a series resistor and capacitor on the output of the amplifier (COMP pin). Equation 14 can determine the resistor on the COMP pin (R_{COMP}).

(EQ. 14) $$R_{COMP} = \frac{0.4 \times I_{STEP}}{I_{OUT(MAX)} \times tran_{percent} \times V_{REF} \times g_{m(EA)}}$$

where:

- I_{STEP} is the expected step in output load current in amps
- $I_{OUT(MAX)}$ is the total load current of all phases in amps
- $tran_{percent}$ is the expected percent overshoot in the output voltage during the load step
- V_{REF} is the internal reference voltage on the VFB+ pin which is 0.6V (typ)
- $g_{m(EA)}$ is the transconductance of the error amplifier which is 0.00357S (typ)

To calculate the C_{COMP} value, the output capacitance must first be determined.

(EQ. 15) $$C_{OUT(MIN)} = \frac{1\times10^{4} \times R_{COMP} \times gm \times V_{REF}}{2\pi \times f_{SW} \times R_{CSA} \times V_{OUT}}$$

where:

- $C_{OUT(MIN)}$ is the minimum output capacitance in µH
- R_{COMP} is the COMP pin resistor calculated in Equation 14 in ohms
- V_{REF} is the internal reference voltage on the VFB+ pin which is 0.6V (typical)
- L_{SEL} is the user selected output inductance between L_{MIN} and L_{MAX} in Henries
- f_{SW} is the switching frequency of the power supply in hertz
- R_{CSA} is the effective trans-resistance of the current sensor calculated in Equation 9 in ohms
- V_{OUT} is the output voltage of the power supply in volts

When $C_{OUT(MIN)}$ is calculated, select the next largest standard capacitance value as the output capacitance, hereby referred to as C_{OUT}.

(EQ. 16) $$f_t = \frac{V_{REF} \times g_{m(EA)} \times R_{COMP}}{V_{OUT} \times 2\pi \times C_{OUT} \times R_{CSA}}$$

(EQ. 17) $$C_{COMP(MIN)} = \frac{1}{2\pi \times f_t \times R_{COMP}}$$

where:

- $C_{COMP(MIN)}$ is the minimum compensation capacitance in Farads
- V_{REF} is the internal reference voltage on the VFB+ pin which is 0.6V (typical)
- $g_{m(EA)}$ is the transconductance of the error amplifier which is 0.00357S (typical)
- R_{COMP} is the COMP pin resistor calculated in Equation 14 in ohms
- V_{OUT} is the output voltage of the power supply in volts
- C_{OUT} is the output capacitance of the power supply
- R_{CSA} is the effective trans-resistance of the current sensor calculated in Equation 9 in ohms

To obtain the final error amp compensation capacitor value, select the next highest standard capacitance value above $C_{COMP(MIN)}$, this value is called C_{COMP}.

6.8 Droop Regulation Setting

Droop regulation changes the DC regulation set point inversely to the output load current, which allows for improved transient response. To use droop regulation, place a resistor between the DROOP and VREF pins. If droop regulation is not needed, short the DROOP and VREF pins together. Figure 50 shows the transient response with droop resistor = 0Ω and Figure 51 shows the transient response with droop resistor = 604Ω. The transient response is reduced by 30% with droop regulation, which translates to smaller output capacitance requirements.

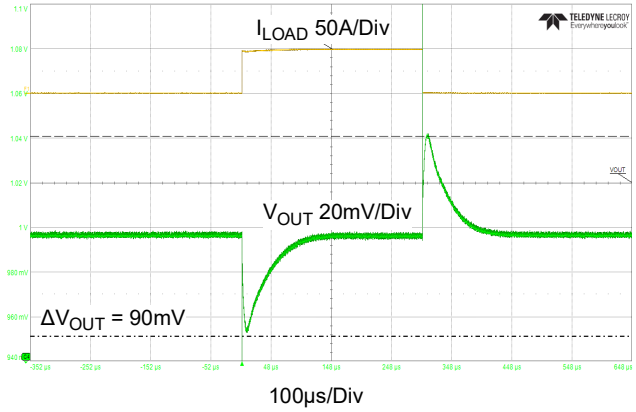


Figure 50. Transient Response without Droop Regulation

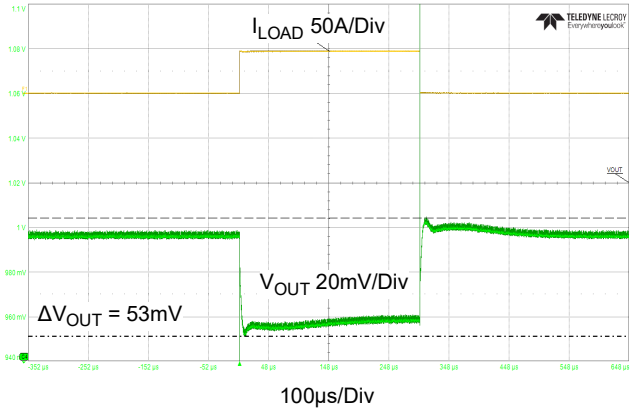


Figure 51. Transient Response with Droop Regulation

The DROOP pin sinks a current proportional to the output loading. The current into the DROOP pin is calculated using Equation 18:

(EQ. 18) $$I_{DROOP} = \sum_{n=1}^{2} R_{SEN} \times I_{OUT(MAX)} \times g_{m(CSA, DRP)}$$

where:

- I_{DROOP} is the current into the DROOP pin in µA.
- R_{SEN} is the sense resistor in mΩ calculated from Equation 3
- $I_{OUT(MAX)}$ is the max DC output current for a given phase in amps

As the output loading increases, the current into the DROOP pin increases and generates a voltage across the resistor between DROOP and VREF. This lowers the reference voltage presented to the error amplifier, which effectively lowers the regulation point. The extent of the droop variation can be tuned by carefully selecting the droop resistor.

When using droop regulation it is important to set the light load regulation point at the highest acceptable voltage using Equation 2. Then, calculate the percent deviation of the regulated voltage that is needed to achieve the lowest acceptable voltage at the maximum DC loading. When the percentage deviation ($DRP_{percent}$) is determined, Equation 19 can calculate the resistance needed between VREF and DROOP.

(EQ. 19) $$R_{DROOP} = \frac{DRP_{percent} \times V_{REF}}{I_{DROOP}}$$

where:

- R_{DROOP} is the resistance between VREF and DROOP
- $DRP_{percent}$ is the percentage variation of VOUT needed at full load

- V_{REF} is the internal voltage reference which is 0.6V (typ)
- I_{DROOP} is the current into the DROOP pin from Equation 18

Because I_{DROOP} follows the inductor current, we need to average the signal to get the DC load current. The value of the capacitance is calculated using Equation 20:

(EQ. 20) $$C_{DROOP} = \frac{R_{COMP} \times C_{COMP}}{R_{DROOP}}$$

where:

- R_{DROOP} is the resistance between VREF and DROOP pins
- R_{COMP} is the resistor in the series RC on the COMP pin from Equation 14
- C_{COMP} is the capacitor in the series RC on the COMP pin (next highest standard value above Equation 17)
- I_{DROOP} is the current into the DROOP pin from Equation 18

6.9 Soft-Start Capacitor Selection

The ISL73847SEH has adjustable soft-start to help control the inrush current during start up. A capacitor to ground on the SS pin controls the startup dynamics of the power supply. A nominal 10µA is sourced out of the SS pin and therefore, the charging rate is equal to 10µA/C, where C is the soft-start capacitance. Equation 21 shows how to calculate the capacitance given the required soft-start time.

(EQ. 21) $$C_{SS} = \frac{t_{SS} \times 1 \times 10^{-5}}{V_{REF}}$$

where:

- C_{SS} is the soft-start capacitance in Farads
- t_{SS} is the required soft-start time in seconds
- VREF is the reference voltage, which is nominally 0.6V

The output should be in regulation when the soft-start capacitor reaches the band gap voltage of 0.6V, however, the ISL73847SEH waits until soft-start reaches 0.9V before allowing PGOOD to reflect the state of the output.

6.10 Layout

6.10.1 Layout Guidelines

The following are recommendations for the best performance on the ISL73847SEH:

- Place the VDD bulk and high-frequency capacitor as close as possible to the VDD pin.
- Place the feedback resistors as close as possible to the VFB+ and VFB- pins to minimize parasitic capacitance.
- Ensure that all feedback traces are routed away from noisy switching nodes.
- Place the RSENSE RC filter as close to the ISENX+ and ISENX- pins as possible.
- Place C_{COMP}, R_{COMP}, and C_{POLE} as close as possible to the COMP pin.
- SS, Droop, and VREF capacitors should be referenced to VFB-.
- Ensure to have a good ground plane.
- Place bulk and high-frequency PVIN capacitors close to the ISL70020SEH FETS drain (Not drawn).
- Minimize the current loop area between the PVIN bulk capacitors and GND and phase node connections
- Connect the feedback traces to the load for point-of-load (POL) regulation.
- Ensure that the traces carrying high load currents are wide enough.

6.10.2 Layout Example

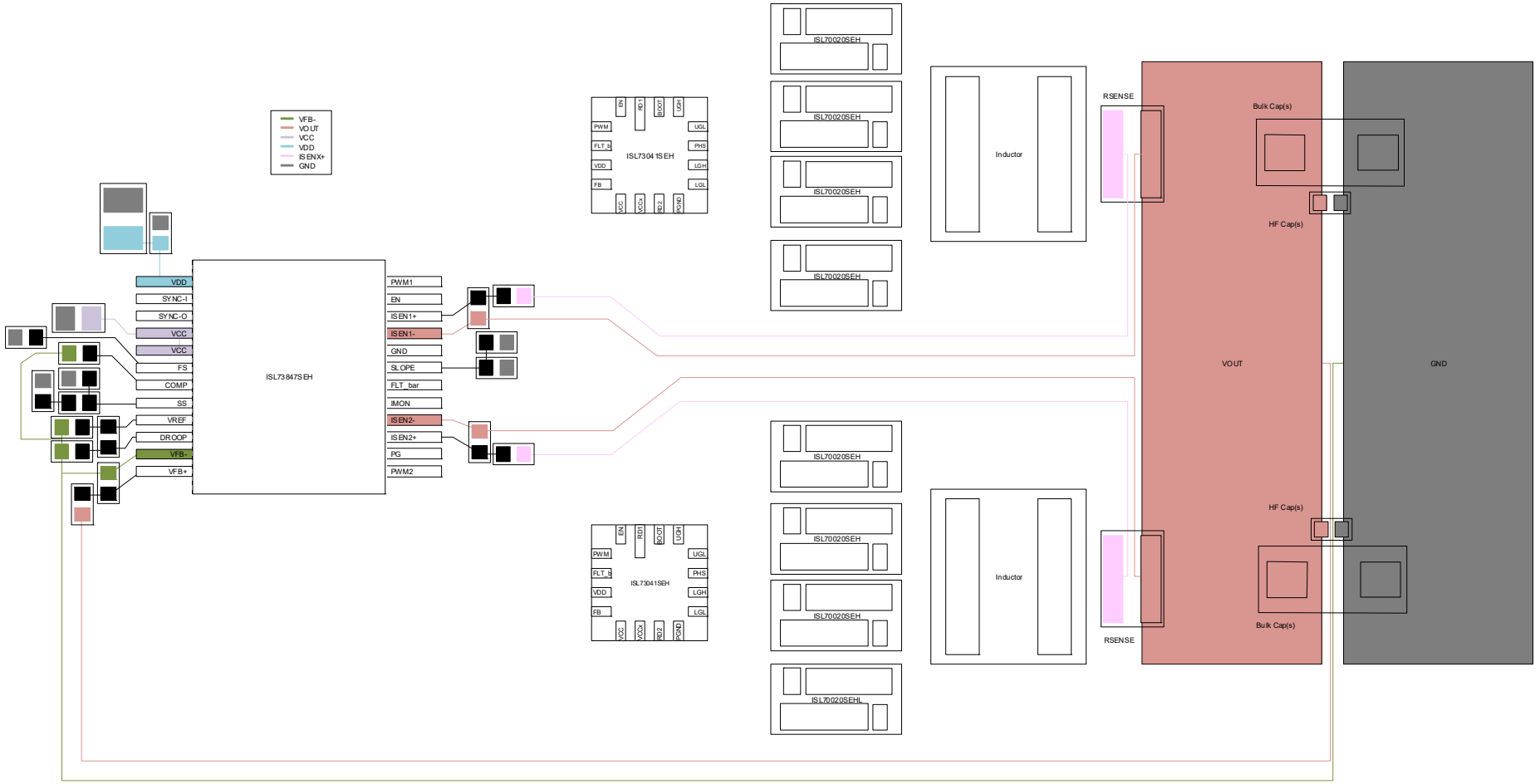


Figure 52. Layout Recommendations

7. Die and Assembly Characteristics

Table 2. Die and Assembly Related Information

Die Information	
Dimension	3710µm (146 mils) × 7110µm (280 mils) Thickness: 483µm ±25µm (19 mils ±1 mil)
Interface Materials	
Passivation	Type: Silicon Dioxide and silicon nitride Thickness: 24.5kÅ
Top Metallization	Type: Top metal/Bond Pad Composition 99.5% Al, 0.5%Cu
Backside Finish	Silicon
Process	0.25µm BiCMOS
Assembly Information	
Substrate Potential	Internal connection to GND
Additional Information	
Worst Case Current Density	31.36mA/µm
Transistor Count	268182
Weight of Packaged Device	1.39 grams
Lid Characteristics	Finish: Gold, Potential: Tied to Pin 20

7.1 Metallization Mask Layout

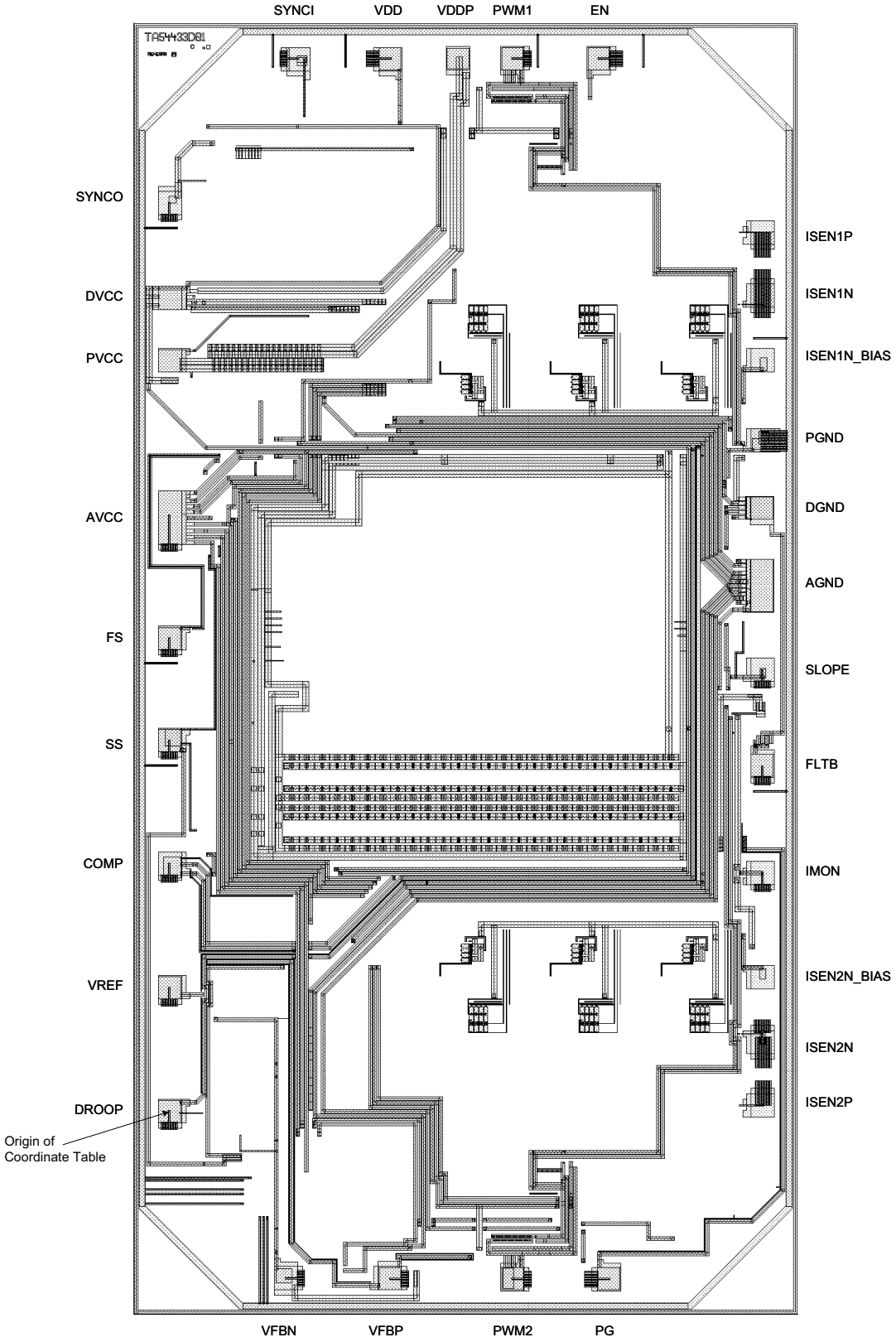
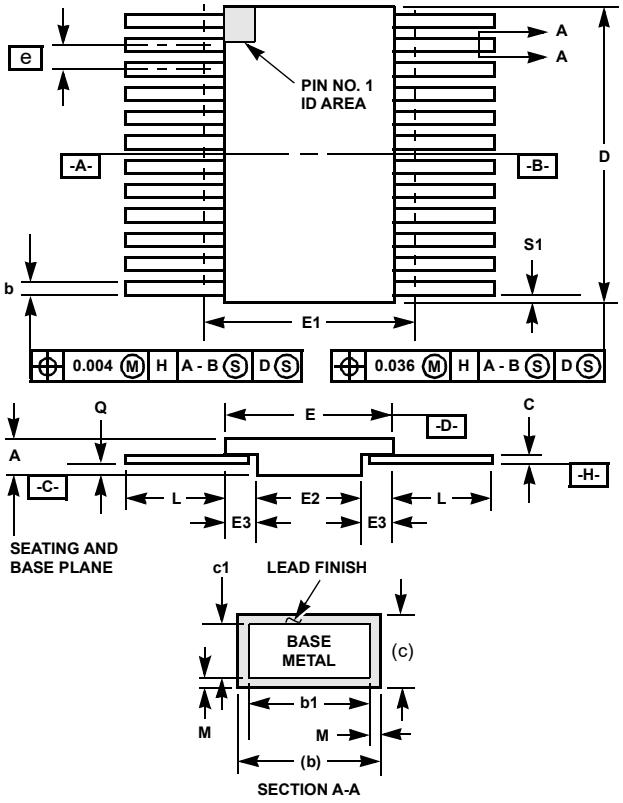


Table 3. Layout X-Y Coordinates (Centroid of Bond Pad)

Pad Name	Pad Number	Pin Number	X-Coordinate (um)	Y-Coordinate (um)	Pad Size X (um)	Pad Size Y (um)	Bond Wire Diameter (0.001”)
VDDP	1	1	1559	5706	117	117	1.25
VDD	2	1	1195	5699	117	117	1.25
SYNCI	3	2	695	5699	117	117	1.25
SYNCO	4	3	0	4924	117	117	1.25
DVCC	5	4	0	4407	117	117	1.25
PVCC	6	5	0	4070	117	117	1.25
AVCC	7	5	0	3216	117	280	1.25
FS	8	6	0	2565	117	117	1.25
SS	9	7	0	2010	117	117	1.25
COMP	10	8	0	1340	117	117	1.25
VREF	11	9	0	670	117	117	1.25
DROOP	12	10	0	0	117	117	1.25
VFBN	13	11	627	-905	117	117	1.25
VFBP	14	12	1191	-905	117	117	1.25
PWM2	15	13	1855	-912	117	117	1.25
PG	16	14	2379	-912	117	117	1.25
ISEN2P	17	15	3211	31	117	117	1.25
ISEN2N	18	16	3211	373	117	117	1.25
ISEN2N_BIAS	19	16	3211	726	117	117	1.25
IMON	20	17	3211	1290	117	117	1.25
$\overline{\text{FLT}}$	21	18	3211	1871	117	117	1.25
SLOPE	22	19	3211	2392	117	117	1.25
AGND	23	20	3211	2848	117	280	1.25
DGND	24	20	3211	3270	117	117	1.25
PGND	25	20	3211	3635	117	117	1.25
ISEN1N_BIAS	27	21	3211	4070	117	117	1.25
ISEN1N	26	21	3211	4421	117	117	1.25
ISEN1P	28	22	3211	4763	117	117	1.25
EN	29	23	2322	5706	117	117	1.25
PWM1	30	24	1855	5706	117	117	1.25

8. Package Outline Drawing

For the most recent package outline drawing, see K24.A.



K24.A MIL-STD-1835 CDFP4-F24 (F-6A, CONFIGURATION B)
24 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.640	-	16.26	3
E	0.350	0.420	9.14	10.67	-
E1	-	0.450	-	11.43	3
E2	0.180	-	4.57	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	24		24		-

Rev. 0 5/18/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

9. Ordering Information

Part Number[1]	Radiation Hardness (Total Ionizing Dose)	Package Description (RoHS Compliant)	Package Drawing	Temperature Range
ISL73847SEHMF	LDR to 75krad(Si)	24 Ld CDFP Packaged Device (QML-V Level Screening)	K24.A	-55 to +125°C
ISL73847SEHMX[2]		Bare Die (QML-V Level Screening)	N/A	
ISL73847SEHF/PROTO[3]	N/A	24 Ld CDFP Packaged Device (For Evaluation Purposes)	K24.A	
ISL73847SEHX/SAMPLE[2][3]	N/A	Bare Die (For Evaluation Purposes)	N/A	
ISL73847SEHEV2Z[4]	Evaluation Board (For Evaluation Purposes)			

1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Die product tested at TA = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in Electrical Specifications. The die is sourced from wafer lots that have been qualified for Group C and Group E per MIL-PRF-38535 (Refer to *R34TB0001: Renesas Radiation Hardened Hermetic Screening and QCI Flow* for more information).
3. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in this datasheet. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in this datasheet. The /SAMPLE parts do not receive 100% screening across temperature to the electrical limits. These part types do not come with a Certificate of Conformance.
4. Evaluation board uses the /PROTO parts and /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

10. Revision History

Rev.	Date	Description
2.00	Apr 20, 2023	Updated $\overline{FLT}$ Drive current maximum spec from 60mA to 75mA. Updated Droop current -55°C maximum spec from 22µA to 23.5µA, Changed the $g_{m(EA)}$ values on page 32 and 33 from 0.001S to 0.00357S.
1.02	Feb 15, 2023	Added new bullets in the Features section. Updated VCC pin descriptions. Updated Figures 3, 4, and 5. Updated Droop Regulation and Droop Regulation Setting sections. Updated Equations 1, 15, and 17. Updated Note 2 and the package description in the ordering information table.
1.01	Dec 15, 2022	Updated Pin Descriptions table. Updated Absolute Maximum Ratings section adding row 3 and fixing typo in the parameter column for first row.
1.00	Nov 21, 2022	Initial Release

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