MP1660

16V, 3A, 600kHz, High-Efficiency, Synchronous, Step-Down Converter with 0.6V V_{REF} in a SOT563 Package

DESCRIPTION

The MP1660 is a fully integrated, high-frequency, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. The MP1660 offers a very compact solution that achieves 3A of output current, with excellent load and line regulation over a wide input range. The MP1660 uses synchronous mode operation for higher efficiency over the output current load range.

Constant-on-time (COT) control operation provides very fast transient response, easy loop design, and very tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The MP1660 requires a minimal number of readily available, standard external components, and is available in a space-saving SOT563 package.

FEATURES

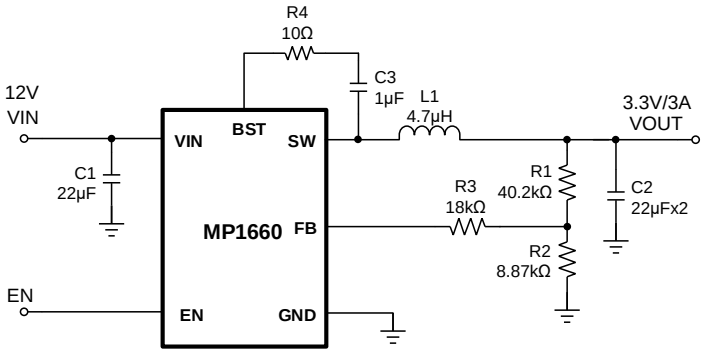
- Wide 4.5V to 16V Operating Input Range
- 110mΩ/60mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- 190μA Low I_Q
- High-Efficiency Synchronous Mode Operation
- Power-Save Mode at Light-Load
- Fast Load Transient Response
- 600kHz Switching Frequency
- Internal Soft Start (SS)
- Over-Current Protection (OCP) and Hiccup Mode
- Thermal Shutdown
- Output Adjustable from 0.6V
- Available in a SOT563 Package

MPL Optimized Performance with MPS Inductor MPL-AL6050 Series

APPLICATIONS

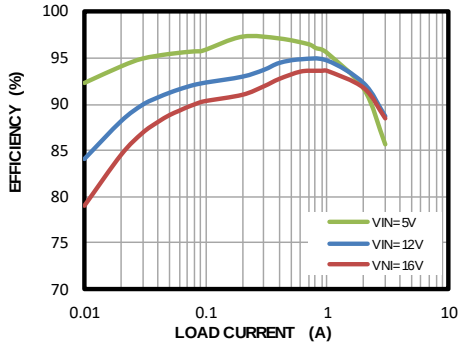
- Security Cameras
- Digital Set-Top Boxes
- Flat-Panel Television and Monitors
- General Purposes

TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT} = 3.3V, L = 4.7μH, DCR = 16.5mΩ



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP1660GTF	SOT563	*See Below*	*1*

* For Tape & Reel, add suffix –Z (e.g. MP1660GTF–Z).

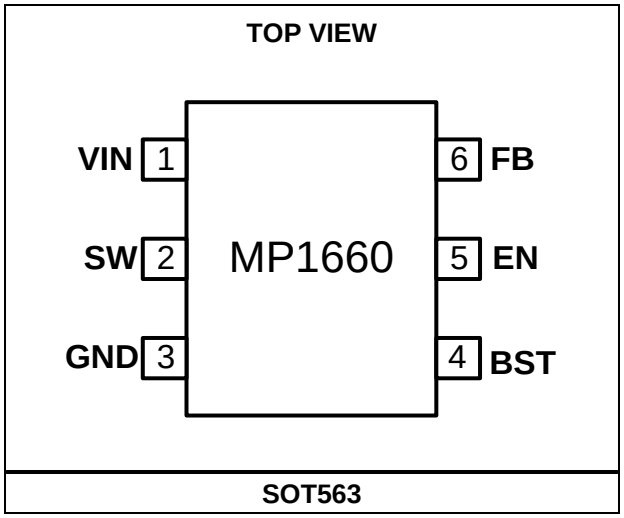
TOP MARKING

BMTY

LLL

BMT: Product code of MP1660GTF
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	VIN	**Supply voltage.** The MP1660 operates from a 4.5V to 16V input rail. A capacitor (C1) is required to decouple the input rail. Connect VIN using a wide PCB trace.
2	SW	**Switch output.** Connect SW using a wide PCB trace.
3	GND	**System ground.** GND is the reference ground of the regulated output voltage. GND requires extra consideration when designing the PCB layout. Connect GND with copper traces and vias.
4	BST	**Bootstrap.** Connect a 1µF BST capacitor and a resistor between SW and BST to form a floating supply across the high-side switch driver.
5	EN	**Enable.** Drive EN high to enable the MP1660. For automatic start-up, connect EN to VIN through a 100kΩ pull-up resistor.
6	FB	**Feedback.** To set the output voltage, connect FB to the tap of an external resistor divider from the output to GND.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to +20V
V_{SW} ..... -0.6V (-6.5V for <10ns) to V_{IN} + 0.3V (21V for <10ns)
V_{BST} ..... V_{SW} + 5V
V_{EN} ..... -0.3V to +5V (2)
All other pins .....-0.3V to +5V
Continuous power dissipation (T_A = 25°C) (3) (5) 2.2W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) 2000V
Charged device model (CDM).....1500V

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) .....4.5V to 16V
Output voltage (V_{OUT}).....0.6V to VIN x D_{MAX} or 10V maximum
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

SOT563
EVL1660-TF-00A (5)..... 55..... 21... °C/W
JESD51-7 (6) ..... 130..... 60... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) For details on EN's ABS max rating, see the Enable Control section.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on EVL1660-TF-00A, 2-layer PCB.
6) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

VIN = 12V, T_J = -40°C to +125°C (7), typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown supply current	I_{IN}	V_{EN} = 0V			10	μA
Quiescent supply current	I_Q	T_J = -40°C to +125°C, V_{EN} = 2V, V_{FB} = 0.65V	0.15	0.19	0.3	mA
		T_J = 25°C, V_{EN} = 2V, V_{FB} = 0.65V	0.16	0.19	0.23	mA
HS switch on resistance	HS_{RDS-ON}	V_{BST-SW} = 3.3V		110		mΩ
LS switch on resistance	LS_{RDS-ON}			60		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 12V			10	μA
Valley current limit	I_{LIMIT}			4		A
Zero-current detection	I_{ZCD}	V_{OUT} = 3.3V, L_O = 4.7μH, I_{OUT} = 0A	-150	-20	+150	mA
Oscillator frequency	f_{SW}		420	600	780	kHz
Minimum on time (8)	t_{ON_MIN}			45		ns
Minimum off time (8)	t_{OFF_MIN}			180		ns
Feedback voltage	V_{REF}	T_J = 25°C	591	606	621	mV
Feedback voltage	V_{REF}	T_J = -40°C to +125 °C	587	606	625	mV
Feedback current	I_{FB}			10	100	nA
FB under-voltage threshold (high to low)	V_{UV_TH}	Hiccup entry		68%		V_{REF}
Hiccup duty cycle (8)	D_{HICCUP}			25		%
EN rising threshold	V_{EN_RISING}		1.14	1.2	1.26	V
EN hysteresis	V_{EN_HYS}			100		mV
EN input current	I_{EN}	V_{EN} = 2V		2		μA
VIN under-voltage lockout rising threshold	$INUV_{VTH}$		3.7	4.1	4.35	V
VIN under-voltage lockout threshold hysteresis	$INUV_{HYS}$			330		mV
Soft-start time	t_{SS}		0.6	1	1.4	ms
Thermal shutdown (8)	TSD			150		°C
Thermal hysteresis (8)	TSD_{HYS}			20		°C

Notes:

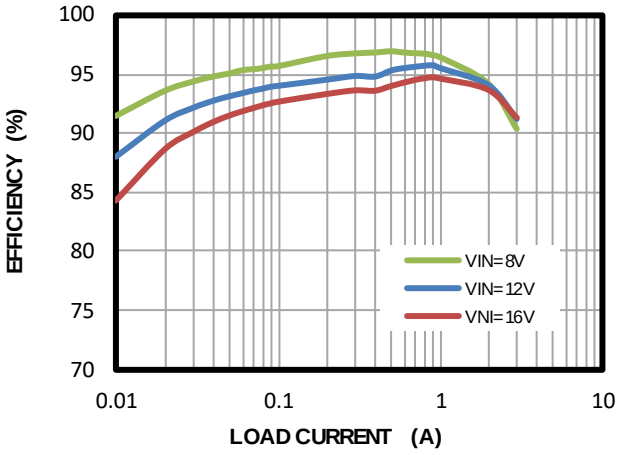
7) Not tested in production. Guaranteed by over-temperature correlation.
8) Guaranteed by design and engineering sample characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

VIN = 12V, V_{OUT} = 3.3V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

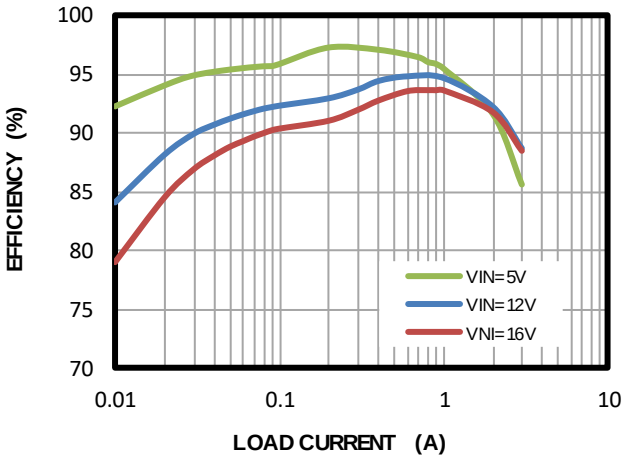
Efficiency vs. Load Current

V_{OUT} = 5V, L = 4.7µH, DCR = 16.5mΩ



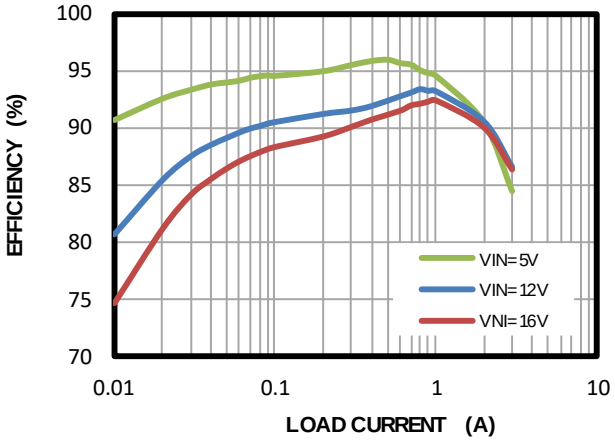
Efficiency vs. Load Current

V_{OUT} = 3.3V, L = 4.7µH, DCR = 16.5mΩ



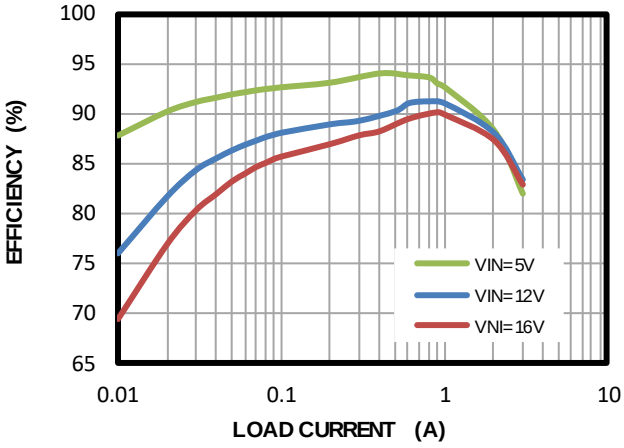
Efficiency vs. Load Current

V_{OUT} = 2.5V, L = 3.3µH, DCR = 11.7mΩ



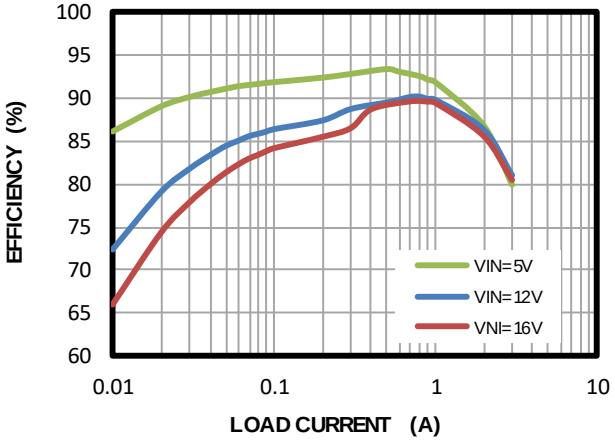
Efficiency vs. Load Current

V_{OUT} = 1.8V, L = 2.2µH, DCR = 8.3mΩ



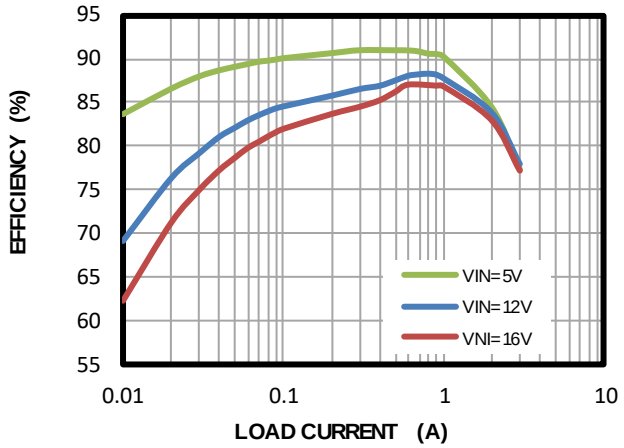
Efficiency vs. Load Current

V_{OUT} = 1.5V, L = 2.2µH, DCR = 8.3mΩ



Efficiency vs. Load Current

V_{OUT} = 1.2V, L = 1.5µH, DCR = 6mΩ

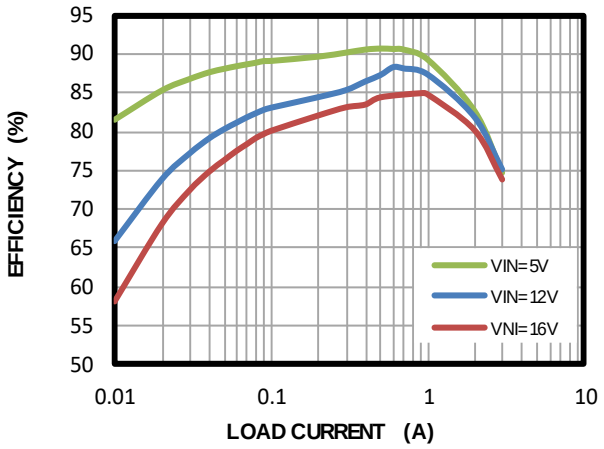


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

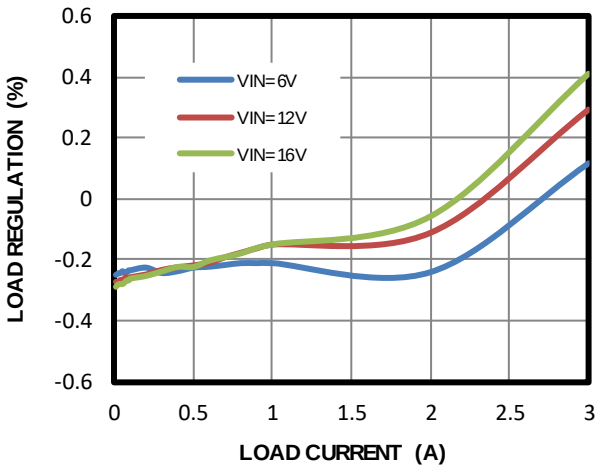
V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

Efficiency vs. Load Current

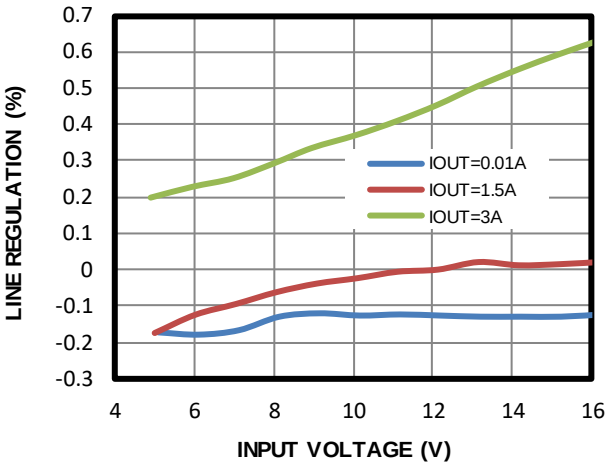
V_{OUT} = 1V, L = 1.5µH, DCR = 6MΩ



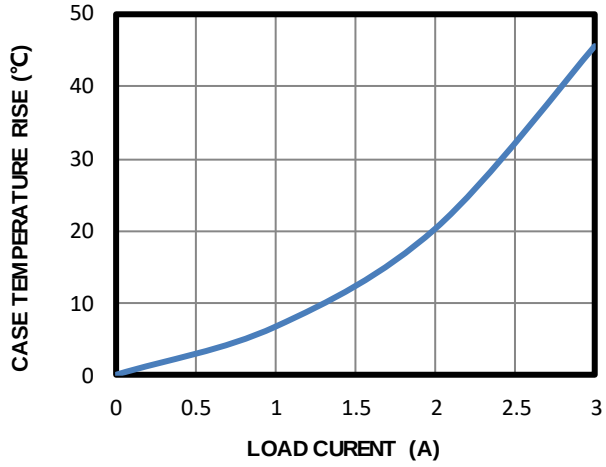
Load Regulation



Line Regulation

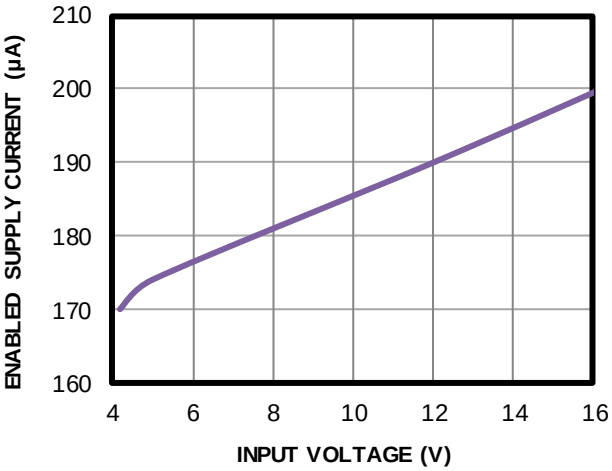


Case Temperature Rise vs. Load Current



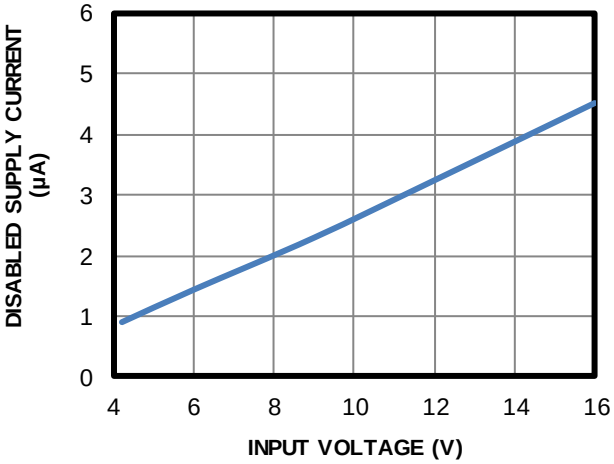
Enabled Supply Current vs. Input Voltage

V_{EN} = 2V, V_{FB} = 0.65V



Disabled Supply Current vs. Input Voltage

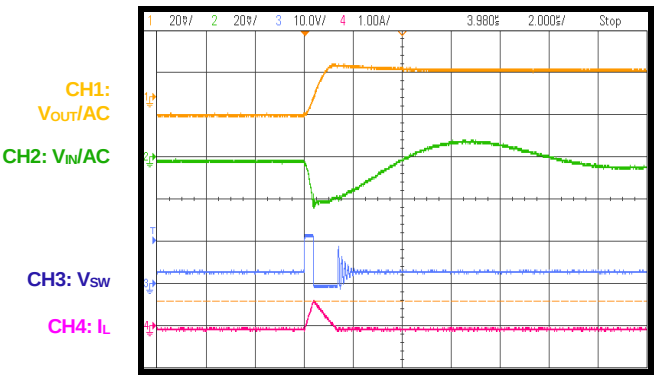
V_{EN} = 0V



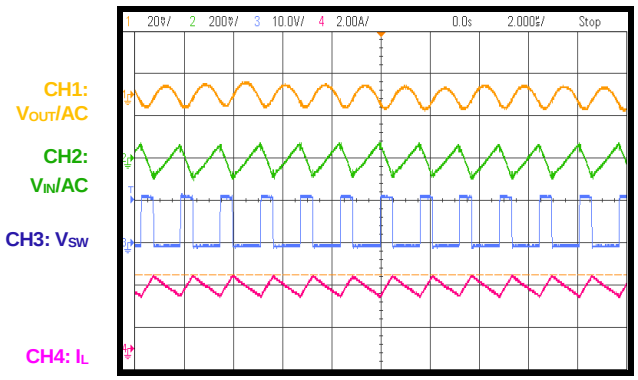
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

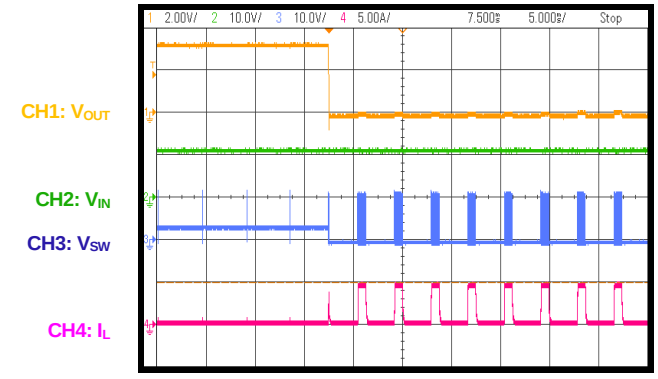
Input/Output Ripple
I_{OUT} = 0A



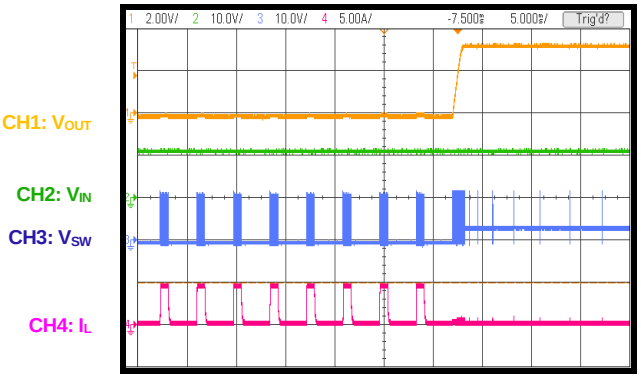
Input/Output Ripple
I_{OUT} = 3A



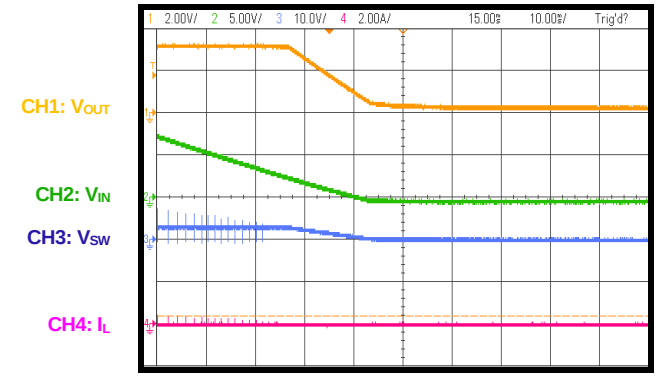
Short-Circuit Entry
I_{OUT} = 0A



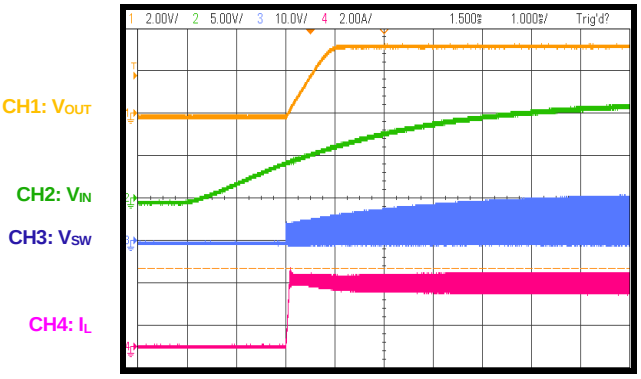
Short-Circuit Recovery
I_{OUT} = 0A



Shutdown through Input Voltage
I_{OUT} = 0A



Start-Up through Input Voltage
I_{OUT} = 3A

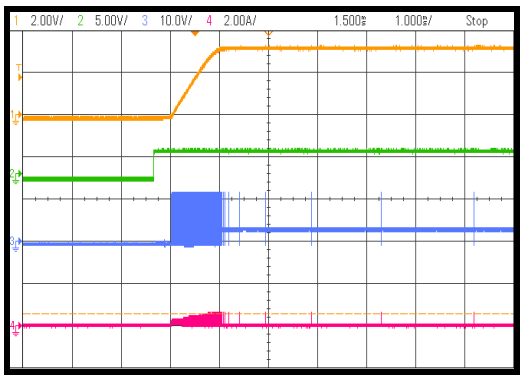


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

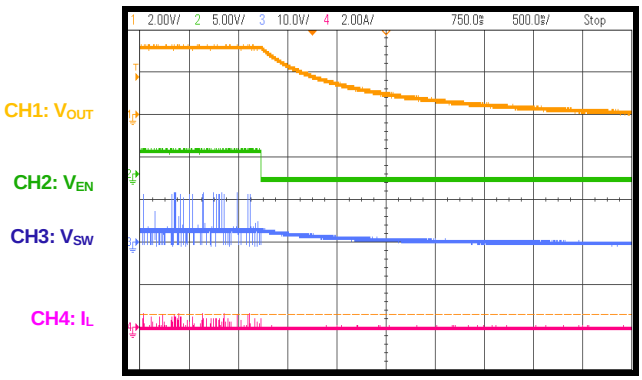
Start-Up through Enable

I_{OUT} = 0A



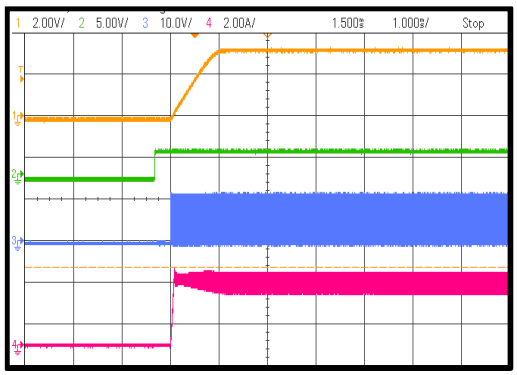
Shutdown through Enable

I_{OUT} = 0A



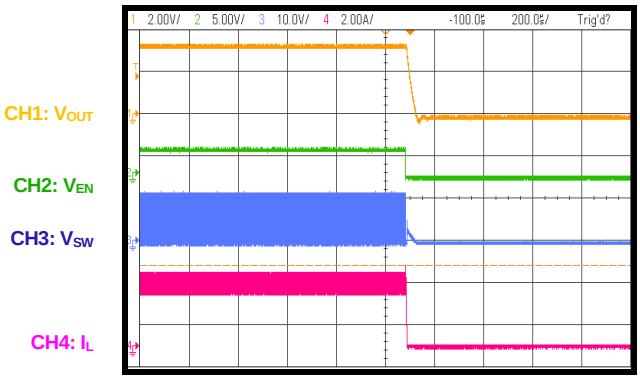
Start-Up through Enable

I_{OUT} = 3A



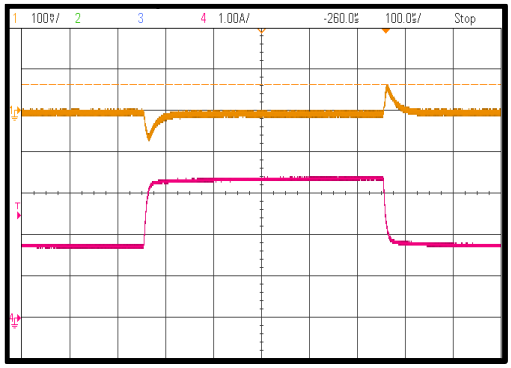
Shutdown through Enable

Iout = 3A



Load Transient

I_{OUT} = 1.5A to 3A, 2.5A/µs



FUNCTIONAL BLOCK DIAGRAM

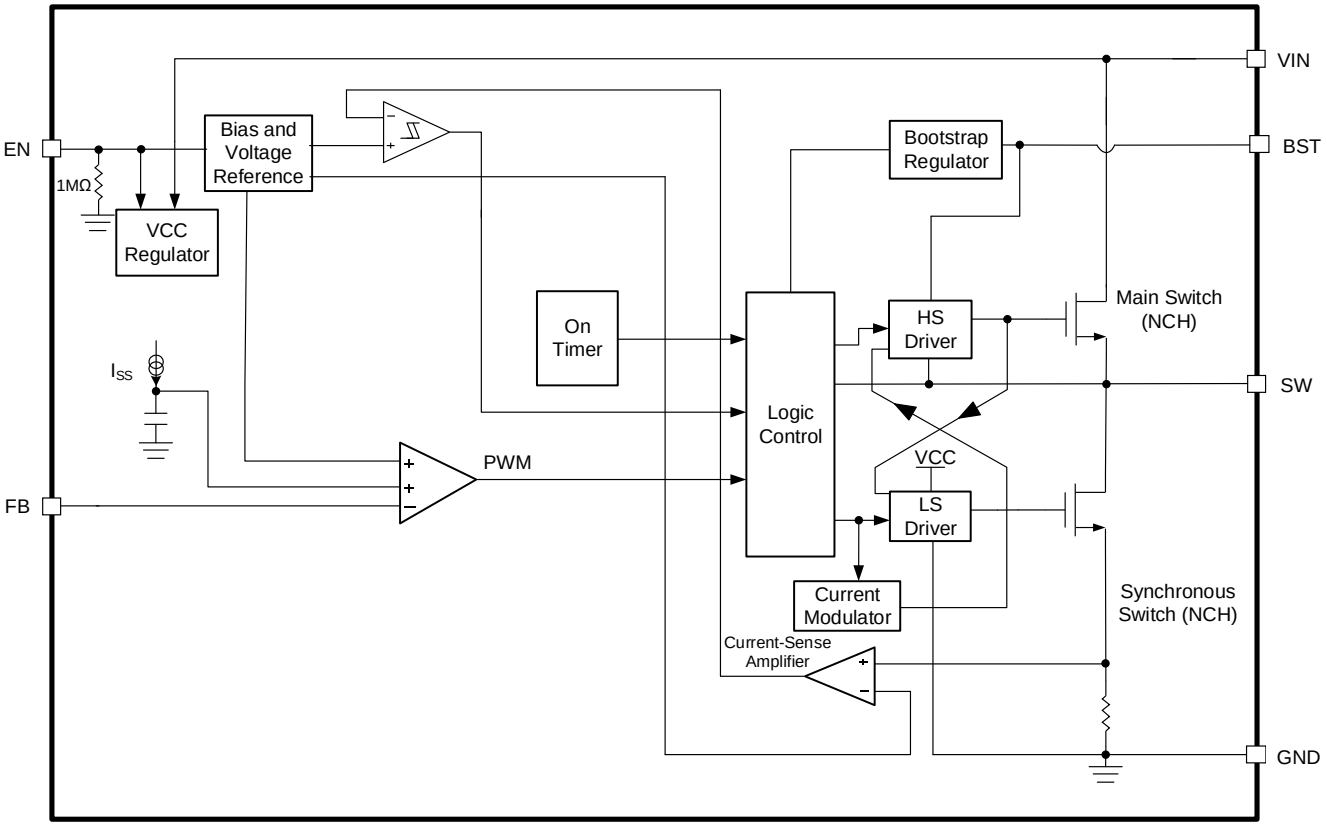


Figure 1: Functional Block Diagram

OPERATION

The MP1660 is a fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and ease loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on when the FB voltage (V_{FB}) drops below the reference voltage (V_{REF}). The HS-FET turns on for a fixed interval, determined by the one-shot on timer. The on timer is determined by both the output voltage and input voltage to keeps the switching frequency fairly constant across the input voltage range.

After the on period elapses, the HS-FET turns off until the next period. By repeating this operation, the converter regulates the output voltage.

The device operates in continuous conduction mode (CCM) when the output current is high and the inductor current is always above 0A. The low-side MOSFET (LS-FET) turns on when the HS-FET is off to minimize conduction loss. A dead short occurs between the input and GND if both the HS-FET and LS-FET turn on at the same time. This is called a shoot-through. To avoid shoot-through, a dead time is generated internally between the HS-FET off and LS-FET on period, and vice versa.

If the MP1660 works in pulse-frequency modulation (PFM) mode during light-load operation, the device reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops almost to zero. If the inductor current reaches zero, the low-side driver goes into tri-state (Hi-Z). The output capacitors discharge slowly to GND through R1 and R2. When V_{FB} drops below V_{REF}, the HS-FET turns on. This greatly improves device efficiency when the output current is low.

Light-load operation is also called skip mode because the HS-FET does not turn on as frequently as it does under heavy-load conditions. The frequency at which the HS-FET turns on is a function of the output current. As the output current increases, the current modulator regulates over a shorter period, the HS-FET turns on more frequently, and the switching frequency increases in turn. The output current (I_{OUT}) reaches its critical level when the current modulator time is zero. I_{OUT} can be calculated with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

The device reverts to pulse-width modulation (PWM) mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant across the output current range.

Enable (EN) Control

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. An internal 1MΩ resistor from EN to GND allows EN to float, which shuts down the IC.

EN is clamped internally using a 2.8V series Zener diode (see Figure 2). Connecting the EN input to VIN through a pull-up resistor limits the EN input current below 100μA to prevent damage to the Zener diode. For example, when connecting a 100kΩ pull-up resistor to 12V V_{IN}, I_{ZENER} = (12V - 2.8V) / (100kΩ + 35kΩ) = 68μA.

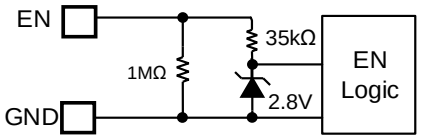


Figure 2: Zener Diode between EN and GND

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP1660 UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 4.1V, while its falling threshold is 3.7V.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V to 1.2V. When V_{SS} is below V_{REF}, V_{SS} overrides V_{REF}, so the error amplifier uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the error amplifier uses V_{REF} as the reference. The SS time is set to 1ms internally.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MP1660 offers valley current limit control. While the LS-FET is on, the inductor current is monitored. When the sensed inductor current reaches the valley current limit, the low-side limit comparator turns over. The device enters over-current protection (OCP) mode, and the HS-FET waits until the valley current limit disappears before turning on again. Meanwhile, the output voltage drops until V_{FB} drops below the under-voltage (UV) threshold (typically 75% below the reference). Once UV is triggered, the MP1660 enters hiccup mode to periodically restart the part.

During over-current protection (OCP), the device attempts to recover from an over-current fault with hiccup mode. The chip disables the output power stage, discharges soft start, and attempts to soft start again automatically. If the over-current condition still remains after soft start ends, the device repeats this operation cycle until the over-current condition is removed and the output rises back to the regulation level. OCP is a non-latch protection.

SCP performance is the same as OCP.

Pre-Biased Start-Up

The MP1660 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the soft start voltage is charged as well. If the BST voltage exceeds its rising threshold voltage and the soft-start voltage exceeds the sensed output voltage at FB, the MP1660 begins working normally.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own under-voltage lockout (UVLO) protection with a rising threshold of 2.2V and a hysteresis of 150mV. VIN regulates the bootstrap capacitor voltage internally through D1, M1, C3, L1, and C2 (see Figure 3). If V_{IN} - V_{SW} exceeds 3.3V, U2 regulates M1 to maintain a 3.3V BST voltage across C3.

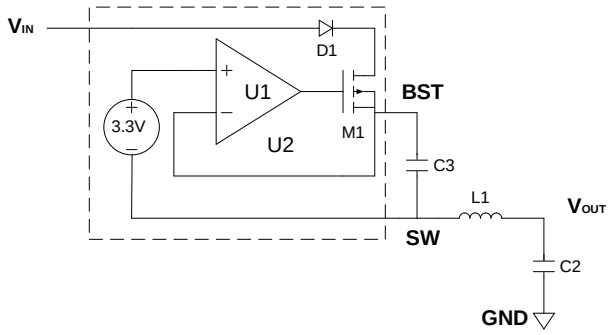


Figure 3: Internal Bootstrap Charger

Start-Up and Shutdown Circuit

If both VIN and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits.

Three events can shut down the chip: EN going low, VIN going low, and thermal shutdown. The shutdown procedure starts by blocking the signaling path initially to avoid any fault triggering. The internal supply rail is then pulled down.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage. First, carefully choose a value for R2. A small R2 leads to considerable quiescent current loss, while a large R2 makes FB noise-sensitive. R2 should be between 5kΩ and 100kΩ. Typically, it is recommended to set the R2 current to be between 5μA and 30μA for a good balance between system stability and no-load loss. R1 can be calculated with Equation (2):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (2)$$

Figure 4 shows the feedback circuit.

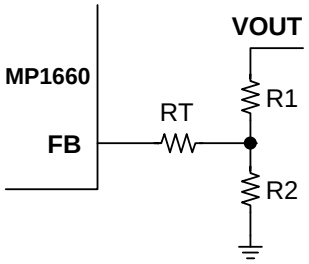


Figure 4: Feedback Network

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Parameters Selection for Common Output Voltages (9)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	RT (kΩ)	L (μH)
5	40.2	5.49	18	4.7
3.3	40.2	8.87	18	4.7
2.5	40.2	12.7	30	3.3
1.8	40.2	20	39	2.2
1.5	40.2	26.7	28	2.2
1.2	40.2	40.2	62	1.5
1	40.2	60.4	82	1.5

Note:

9) For a detailed design circuit, see the Typical Application Circuits section on page 15.

Selecting the Inductor

MPL Optimized Performance with MPS Inductor

An inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current and lower output ripple voltage, but also has a larger physical footprint, higher series resistance, and lower saturation current. A good rule to determine the inductance value is to design the peak-to-peak ripple current in the inductor to be between 30% and 40% of the maximum output current. The peak inductor current should be below the maximum switch current limit. The inductance value can be calculated with Equation (3):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (4):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 2 lists our power inductor recommendations. Select a part number based on your design requirements.

Table 2: Power Inductor Selection

Part Number	Inductor Value	Manufacturer
MPL-AL6050-4R7	4.7μH	MPS
MPL-AL6050-3R3	3.3μH	MPS
MPL-AL6050-2R2	2.2μH	MPS
MPL-AL6050-1R5	1.5μH	MPS

Visit MonolithicPower.com under Products > Inductors for more information.

Selecting the Input Capacitor

The step-down converter has discontinuous input current, and requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for the best performance, and should be placed as close to VIN as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable amid temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (5):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (6):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the specifications.

The input voltage ripple can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, estimated with Equation (8):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (8)$$

Selecting the Output Capacitor

An output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (9)$$

With ceramic capacitors, the impedance at the switching frequency the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

With POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be calculated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

A larger output capacitor can achieve a better load transient response, but consider the maximum output capacitor limitation in the design application. If the output capacitor value is too high, the output voltage cannot reach the design value during the soft-start time, and the device fails to regulate.

The maximum output capacitor value (C_{O_MAX}) can be estimated with Equation (12):

$$C_{O\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times t_{ss} / V_{OUT} \quad (12)$$

Where I_{LIM_AVG} is the average start-up current during the soft-start period, and t_{SS} is the soft-start time.

Design Example

Table 3 lists recommended values when ceramic capacitors are applied.

Table 3: Design Example

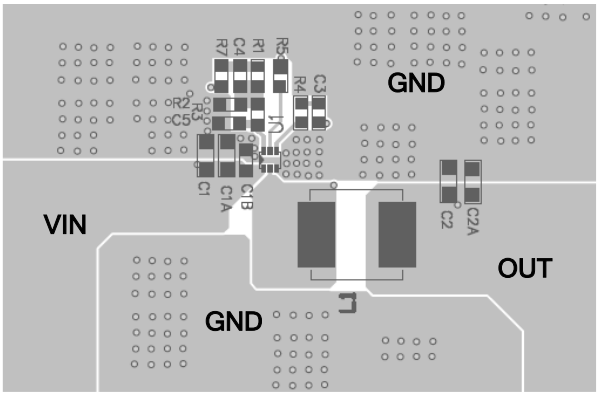
V_{IN}	12V
V_{OUT}	3.3V
I_{OUT}	3A

Figure 7 on page 15 shows the detailed application circuit. For typical performance values and waveforms, see the Typical Performance Characteristics section on page 5. For more device applications, refer to the related evaluation board datasheet.

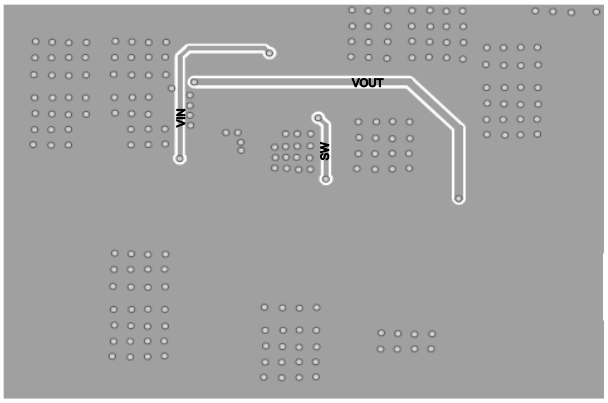
PCB Layout Guidelines

Efficient PCB layout of the switching power supplies is critical for stable function. Poor layout design can result in poor line or load regulation and stability issues. For the best results, refer to Figure 5 and follow the guidelines below:

1. Place the high-current paths (GND, VIN, and SW) very close to the device with short, direct, and wide traces.
2. Place the input capacitor as close to VIN and GND as possible (within 1mm).
3. Place the external feedback resistors next to FB.
4. Keep the switching node (SW) short, and route it away from the feedback network.



Top Layer



Bottom Layer

Figure 5: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

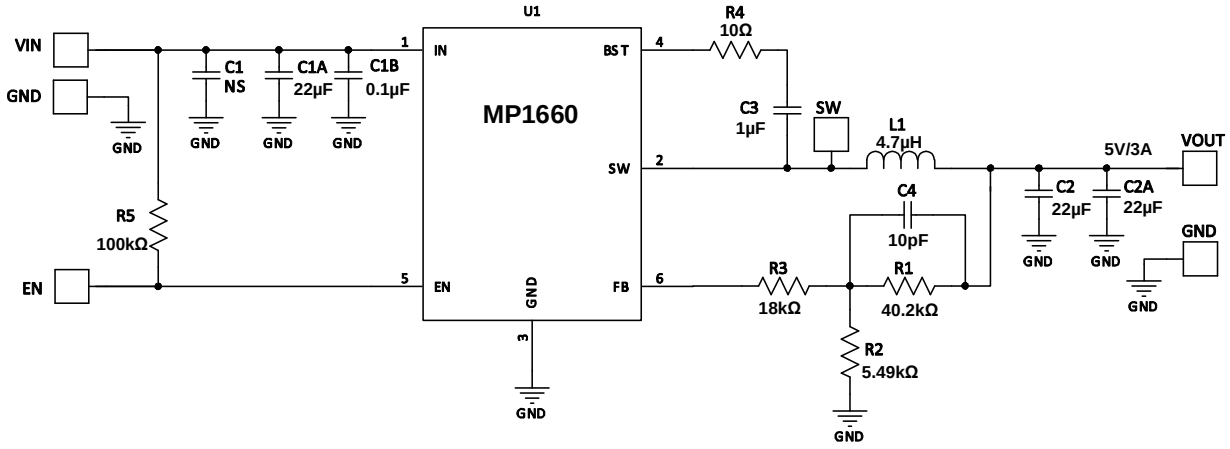


Figure 6: $12V_{IN}$, 5V/3A Output

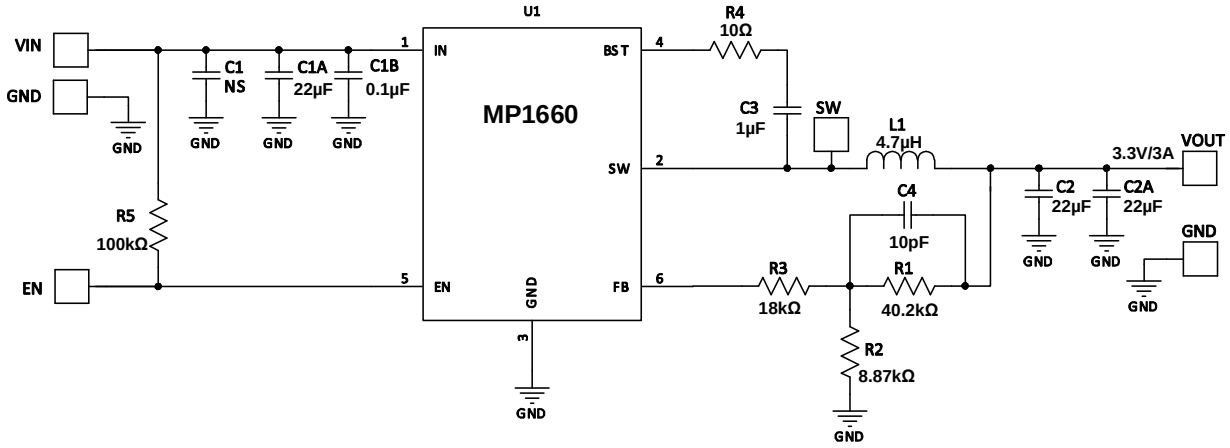


Figure 7: $12V_{IN}$, 3.3V/3A Output

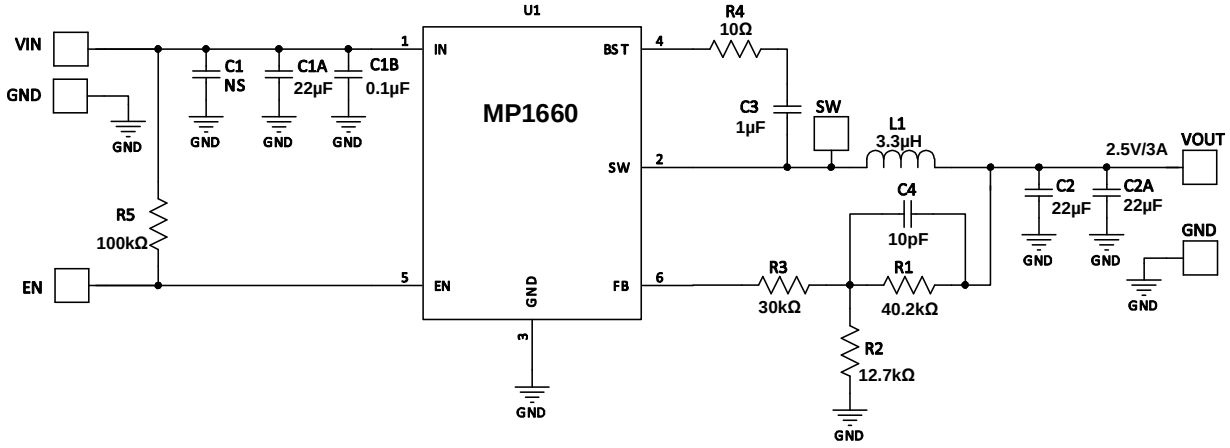


Figure 8: $12V_{IN}$, 2.5V/3A Output

TYPICAL APPLICATION CIRCUITS *(continued)*

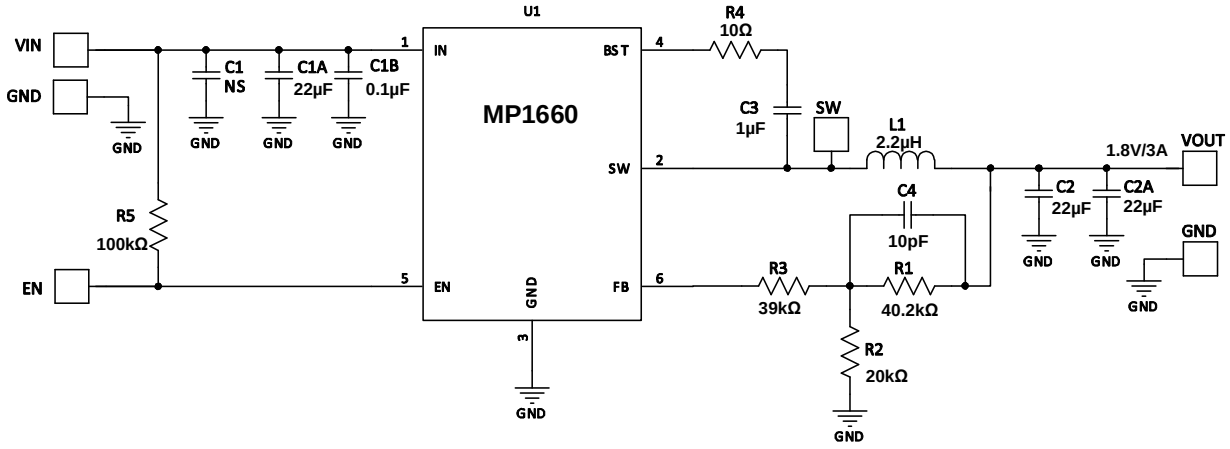


Figure 9: $12V_{IN}$, 1.8V/3A Output

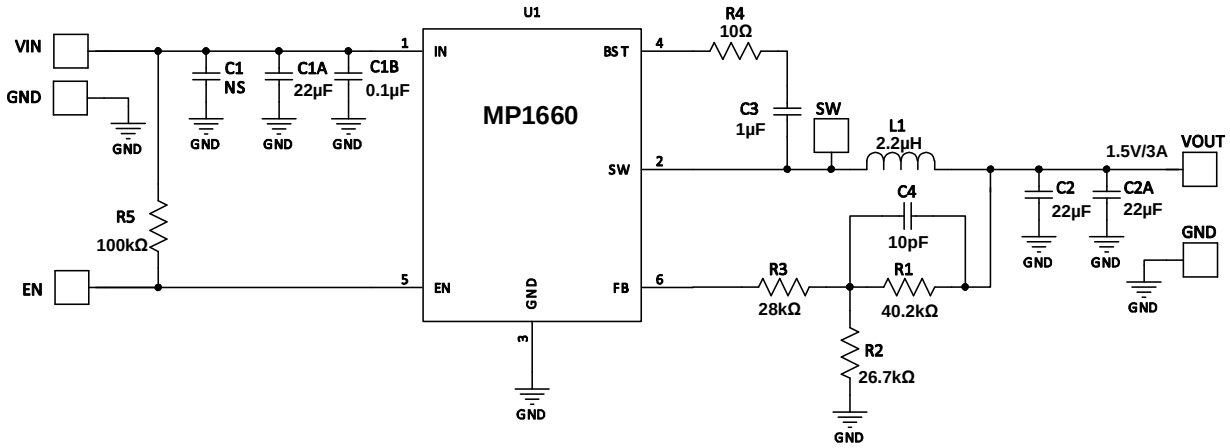


Figure 10: $12V_{IN}$, 1.5V/3A Output

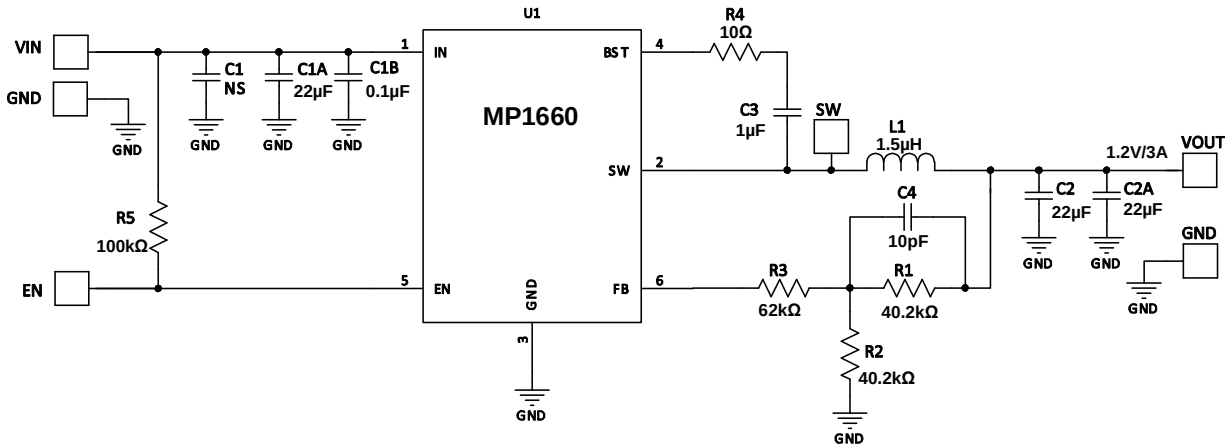


Figure 11: $12V_{IN}$, 1.2V/3A Output

TYPICAL APPLICATION CIRCUITS *(continued)*

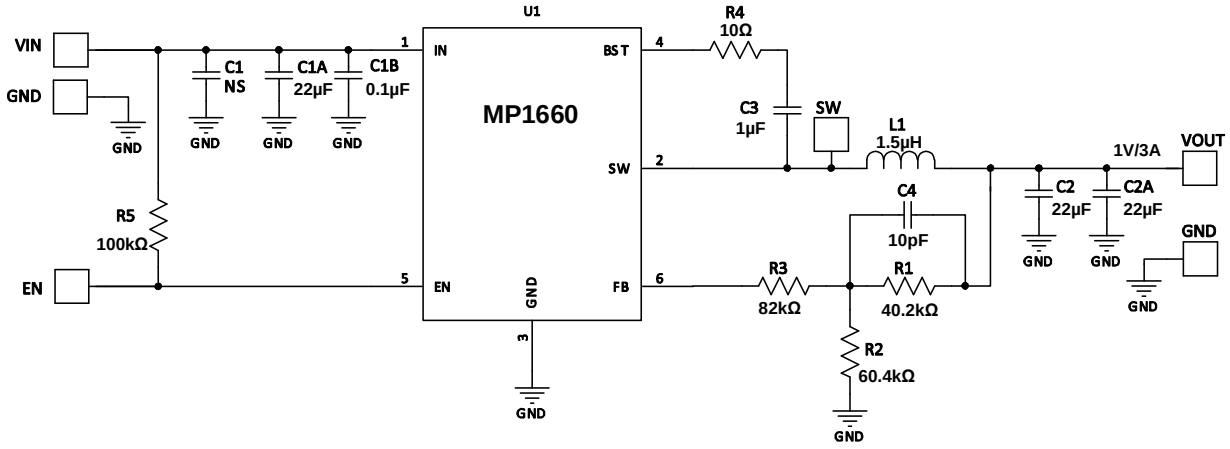
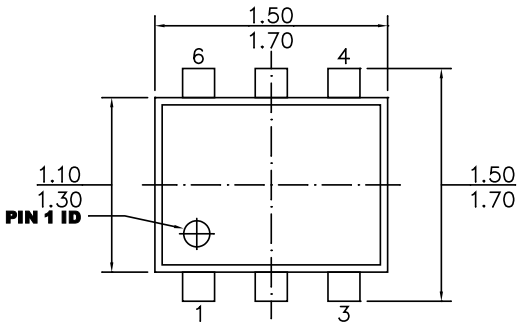


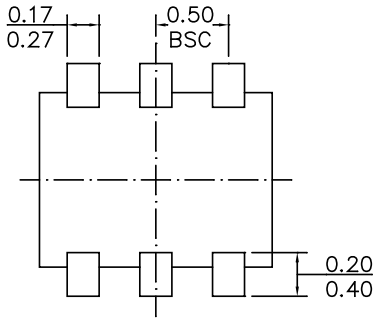
Figure 12: $12V_{IN}$, 1V/3A Output

PACKAGE INFORMATION

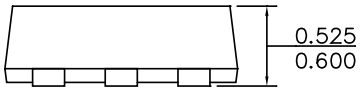
SOT563



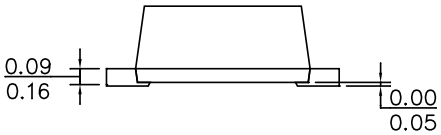
TOP VIEW



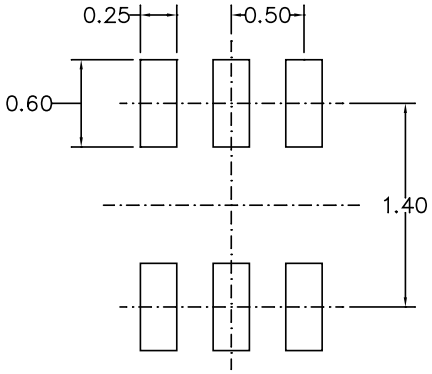
BOTTOM VIEW



FRONT VIEW



SIDE VIEW

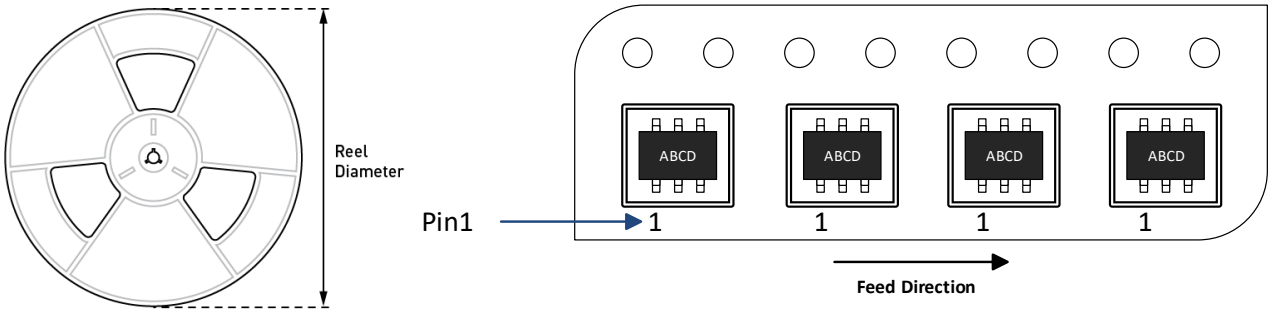


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-293, VARIATION UAAD.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP1660GTF–Z	SOT563	5000	N/A	7in	8mm	4mm

Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	6/9/2020	Initial Release	-