ATMX150RHA

Rad-Hard 150 nm SOI CMOS Cell-based ASIC for Space Use

Introduction

ATMX150RHA is a mixed-signal ASIC offer that provides high-performance and high-density solutions for space applications. With a set of pre-qualified analog IPs, such as DACs, ADCs, PLL, regulators, etc., ATMX150RHA eases the design of mixed-signal ASICs.

ATMX150RHA covers the digital ATC18RHA ASIC offer and extends it up to 22 million gates. The availability of a 5V to 1.8V regulator and the 5V tolerant IO permits easy re-targeting of obsolete or end-of-life ASICs with 5V core supply. In addition, the Physical Design Kit (PDK) enables customers to develop their own analog blocks and use the Microchip Space Multi-Project Wafer (SMPW) foundry services.

ATMX150RHA is manufactured on a 150 nm, five-metal-layer and thick-metal-layer SOI CMOS process intended for use with a supply voltage of 1.8V for core and 2.5/3.3/5V for periphery. This ASIC platform is supported by a combination of state-of-the-art third-party and proprietary design tools from Synopsys®, Mentor® and Cadence®. These tools collectively form the reference tool flows for both the front and back ends.

ATMX150RHA ASICs are available in several quality assurance grades, such as MIL-PRF-38535, QML-Q , QML-V, and ESCC 9000 for the digital domain:

- ESCC DS: 9202/083
- SMD: 5962-20B01

Table of Contents

1. Overview

The *ATMX150RHA Design Manual*, available from your Microchip technical center, provides the information and flows necessary to design a mixed-signal ASIC for space applications. Users can be trained on Microchip-specific or standard commercial tool kits and methodological details for actual implementations.

This offering is CMOS-technology-based, specified with 5/3.3/2.5V and HV 25-45V ranges for the periphery. Core is supplied at 1.8V.

ATMX150RHA is manufactured on a 150nm, five-metal-layers SOI CMOS with Thick Metal technology option - AT77KRHA, a Microchip proprietary process. The digital ATMX150RHA is qualified under the QML-V, QML-Q, and ESCC QML. The domain of qualification covers the main features as follows.

- Comprehensive library of standard logic and I/O cells
- Memory Cells Compiled (ROM, SRAM, DPRAM, and Register File Memory)
- 450 MHz PLL (PLL400MRHA)
- Up to 22 usable Mgates (equivalent NAND2)
- Operating voltage 1.8±0.15V for the core and 5V±0.5V, 3.3±0.3V, 2.5±0.2V for the periphery
- High-speed LVDS buffers 655 Mbps in compliance with the TIA/EIA-644-A standard
- PCI buffers
- Set of analog blocks
- No single event latch-up below an LET threshold of 78 MeV.cm^2/mg at 125°C
- SEU-hardened flip-flops
- TID test up to 150 krads (Si) for 1.8V and 3.3V devices, and 90 krads (Si) for 5V according to MIL-STD 883 TM1019
- CCGA, CLGA, and CQFP qualified package catalog

2. Periphery

2.1 Buffer Descriptions

The peripheral I/O buffer is the electrical interface between the external signals (voltage range from 2.3V to 3.6V and from 4.5V to 5.5V) and the internal core signals (from 1.65V to 1.95V).

I/O libraries are:

- IO5V0 I/O – Powered at 5V
- IO3V3 I/O – Powered at 3.3V
- IO2V5 I/O – Powered at 2.5V, 3.3V tolerant

All I/O buffers are cold sparing and include:

- Bidirectional I/O buffers
- Tristate-output I/O buffers
- Output-only I/O buffers
- Input-only I/O buffers (inverting, non-inverting, Schmitt trigger)

Furthermore, the bidirectional, tristate-output and input-only I/O buffers are available with or without pull-up or pull-down structures.

Specific I/O buffers have been developed in 3.3V and 2.5V:

- LVDS transmitter and receiver differential I/O buffers.
- LVPECL receiver differential I/O buffers
- In 3.3V, PCI-compliant output buffer

I/O buffers are tolerant, that is, the pad signal can be higher than VCCB when it is high impedance (input or bidirectional buffers, tristate buffers in HiZ and LVDS when disable).

I/O buffers are cold sparing, that is, the pad signal can be applied when VCCB is 0V. In both cases, tolerant or cold sparing, there is no impact on core supply, buffer supply, and reliability, if the applied signal respects the recommended operating conditions, and the leakage current is less than 1µA.

2.2 I/O Clusters

The periphery of the chip (pad ring) can be split into several I/O segments (I/O clusters). Some clusters can be unpowered while others are active.

A specific power control line is distributed inside the cluster to force all the I/Os of the cluster in tristate mode regardless of their initial state (i.e., an output-only buffer will also be turned to HiZ mode).

2.3 Double Pad Ring

In case of a large number of IOs, Microchip can provide a double pad ring configuration, where the inner ring is used exclusively for core power supply pads.

3. Core

3.1 Standard Cell Library

The Microchip Standard Cell Library contains a comprehensive set of logic and storage cells, including cells that belong to the following categories:

- Buffers and gates
- Standard and SEU-hardened flip-flops
- Standard and SEU-hardened scan flip-flops
- Latches
- Multiplexers, adders, subtractors

3.2 Memory Hard Blocks

The ATMX150RHA memory libraries are developed from Virage memory compilers. All these memories are synchronous. Four types of memories can be generated on request:

- Single-port synchronous SRAM
- Dual-port memory with two-port read/write synchronous SRAM
- Two-port synchronous register file with one read port and one write port
- ROM with metal programming

For maximum block sizes, refer to *ATMX150RHA Design Manual*, available from your Microchip technical center.

3.3 Analog Blocks

MICROCHIP proposes a catalog of analog IPs qualified that can be delivered with a datasheet and qualpack.

The qualification includes:

- Electrical characterization
- TID and SEE characterization
- HTOL tests

The analog IPs consist of Voltage regulators, a voltage reference and monitoring device, clock synthesizer and signal conditioning IPs.

For more information on a complete list of available analog blocks, please contact the Microchip technical support team in your region.

The following table lists the preliminary IP blocks and their features.

Table 3-1. Analog Blocks Catalog

IP Block	Features
PLL400MRHA	40-450 MHz PLL
ADC12RHA	12-bit 1 Msps ADC
DAC12RHA	12-bit 1 Msps DAC
MUX8RHA	8-channel analog multiplexer, 10 MHz bandwidth
OSCRC10MRHA	Programmable 4/8/10/12 MHZ RC oscillator, ±1% frequency variation over temperature
OSCRC32KRHA	32 kHz RC oscillator
BG1V2RHA	1.215V bandgap voltage reference, max temp. coef 90 ppm/°C

.....continued	
IP Block	**Features**
REG200RHA	Linear voltage regulator from 3-5.5V to 1.8V, 200 mA
POR18RHA	Power-on Reset 1.8V

A Physical Design Kit (PDK), with a full set of basic devices, is also available to design custom analog blocks.

3.4 Array Organization

With the ATMX150RHA, the die size and the package are optimized for each mixed-signal ASIC.

However, for some digital designs, predefined matrix sizes and pad frames are available to ease the assembly of each individual ASIC design by using available package cavity sizes and layouts.

Table 3-2. Standard Array Dimensions

Name	Single Pad Ring		Outer Ring Pads	Double Pad Ring	
	Area (mm^2)	Typical Usable gates(*)		Inner Ring Pads	Typical Usable Gates(*)
ATMX150RHA_216(D)	38	1M	216	88	0.8M
ATMX150RHA_324(D)	77	2.2M	324	140	1.7M
ATMX150RHA_404(D)	114	3.5M	404	180	2.8M
ATMX150RHA_504(D)	170	5.5M	504	232	4.4M
ATMX150RHA_544(D)	199	6.5M	544	252	5.4M
ATMX150RHA_604(D)	237	7.6M	604	284	6.7M
ATMX150RHA_644 (D)	267	8.7M	644	304	7.7M
ATMX150RHA_704(D)	316	10.4M	704	332	9.4M

(*) Based on NAND2 equivalent at 50% density, without memories

4. Advanced Packaging

Microchip proposes advanced multilayer low-noise CQFP and CCGA packages with isolated power and ground planes.

CQFP packages are available with up to 352 leads and CLGA/CCGA packages with up to 896 lands/columns. In addition to the packages listed in the following table, Microchip offers custom package development.

Table 4-1. Packages

Package	Leads/Columns
CQFP	Up to 352
CLGA/CCGA	349, 472, 625, 896

5. Space Multi-Project Wafer (SMPW)

Microchip offers a Space Multi-Project Wafer (SMPW) service, in order to decrease the cost of reticles and silicon by sharing them over several designs. Specific milestones have been created to coordinate the activities and ensure that there will be no interaction between customer designs.

Any questions related to the SMPW service can be addressed to your Microchip technical center.

6. Testability Techniques

For complex designs involving blocks of memory and/or cores, careful attention must be given to design-for-test techniques. The chip size of complex designs, and the number of functional vectors that would need to be created to exercise them fully, strongly suggests the use of more efficient techniques. Combinations of SCAN technique, multiplexed access to memory and/or core blocks, and built-in-self-test logic must be employed, in addition to functional test patterns, to provide both the user and Microchip the ability to test the finished product. Test at speed and transition delay fault patterns are also needed to achieve a good sorting of the dies.

For further information, refer to the *ATMX150RHA TOS Manual*, available from your Microchip technical center.

7. Radiation Hardness

The ATMX150RHA standard cell library encompasses all the specific functions and buffers necessary for space designs, such as LVDS transmitters and receivers, PCI buffers, SEU-hardened DFFs and cold sparing buffers. Key radiation-tolerance parameters are controlled and monitored. Reports are available upon request from your Microchip technical center.

Table 7-1. Radiation Hardness

Parameter	Radiation Hardness Assurance
TID(1) Total Ionizing Dose	100 krads (Si) with 2.5V to 3.3V I/Os
	50 krads (Si) with 5V and HV I/Os
SEU(2) Single Event Upset	Hardened DFF: < $3.22e^{-09}$ errors/bit/day Virage memories with ECC: < $1.18e^{-10}$ errors/bit/day
SEL(3) Single Event Latch-up	Standard results: LETth > 78 MeV.cm²/mg With deep trench isolation LETth > 95 MeV.cm²/mg

Notes:

1. Co-60 testing, in compliance with Mil-Std 883 TM 1019.5: Tested at 25°C, with a total dose rate of 300 rad/h and a total dose up to 150 krads (Si) or 90 krads (Si).
2. Based on worst-case orbit condition (between GEO, ISS LEO, LEO POL, and MEO), at 1.65V for core and 25°C.
3. In worst-case conditions: 1.95V for core, 3.6V or 5.5V for I/Os at 125°C

8. Electrical Characteristics

8.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
TJ	Operating Temperature	–	175	°C
VDD	Core Supply Voltage	-0.3	2	V
VCC	2.5V IO Supply Voltage	-0.3	3	V
VCC	3.3V IO Supply Voltage	-0.3	4	V
VCC	5V IO Supply Voltage	-0.3	6	V
Tstg	Storage Temperature	-65	150	°C
Note: Stresses beyond the ones listed in this table may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.				

8.2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
TJ	Operating Temperature	-55	25	145	°C	–
VDD	Core Supply Voltage	1.65	1.8	1.95	V	–
VCC	2.5V IO Supply Voltage	2.3	2.5	2.7	V	–
VCC	3.3V IO Supply Voltage	3.0	3.3	3.6	V	–
VCC	5V IO Supply Voltage	4.5	5	5.5	V	–
Note: Functional operations beyond those listed in this table are not guaranteed.						

8.3 Consumption

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
ICCSBA	Leakage current per k gate	–	0.003	4.4	µA	–
ICCOPA(*)	Dynamic current per k gate	–	40	57	µA/MHz	–

(*) Average on a mix of cells of different types (regular and hardened flip-flop, simple and complex boolean, multiplexer, adder, buffer and inverter).

8.4 2.5V I/O DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VCC	Buffer Supply Voltage	2.3	2.5	2.7	V	IOs
IIL	Low-level Input Current – With pull-up resistor – With pull-down resistor	-1 60 -5	– 130 –	1 260 5	µA µA µA	Vin=Vss
IIH	High-level Input Current – With pull-up resistor – With pull-down resistor	-1 -5 75	– – 180	1 5 360	µA µA µA	Vin=Vcc
IOZ	High impedance state output current	-1	–	1	µA	Vout=Vcc or Vss No pull resistor
VIL	Low-level input voltage	-0.3	–	0.7	V	–
VIH	High-level input voltage	2	–	Vcc+0.3	V	–
VT+	Positive-going Schmitt trigger threshold	1.11	1.35	1.59	V	–
VT-	Negative-going Schmitt trigger threshold	0.81	0.93	1.17	V	–
Vhyst	Schmitt trigger hysteresis	0.30	0.42	0.54	V	–
IICS	Cold sparing leakage input current	-1	–	1	µA	Vcc=Vss=0V Vin=0 to Vcc
IOCS	Cold sparing leakage output current	-1	–	1	µA	Vcc=Vss=0V Vout=0 to Vcc
VCSth	Supply threshold of cold sparing buffers	–	–	0.5	V	IICS < 4 µA
VOL	Low-level output voltage	–	–	0.4V	V	IOL=1.5, 3, 6, 9, 12 mA
VOH	High-level output voltage	VCC-0.4	–	–	V	IOH=1.5, 3, 6, 9, 12 mA
IOS(*)	Output short-circuit current – IOSN (nn=1) – IOSP (nn=1)	–	–	 14 14	 mA mA	 Vout=Vcc Vout=Vss
Fmax	Maximum frequency, C_{load} = 30 pF	–	–	13 50 80	MHz	nn = 1 nn = 4 nn = 8

(*) Supplied as a design limit but not guaranteed or tested. No more than one output may be shorted at a time for a maximum duration of 10 seconds.

IOSmax = 14, 28, 56, 84, 112 mA for nn = 1, 2, 4, 6, 8

8.5 3.3V I/O DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VCC	Buffer supply voltage	3.0	3.3	3.6	V	IOs
IIL	Low-level input current – With pull-up resistor – With pull-down resistor	-1 110 -5	– 220 –	1 400 5	µA µA µA	Vin=Vss
IIH	High-level input current – With pull-up resistor – With pull-down resistor	-1 -5 140	– – 320	1 5 600	µA µA µA	Vin=Vcc
IOZ	High impedance state output current	-1	–	1	µA	Vout=Vcc or Vss No pull resistor
VIL	Low-level input voltage	-0.3	–	0.8	V	–
VIH	High-level input voltage	2	–	Vcc+0.3	V	–
VT+	Positive-going Schmitt trigger threshold	1.47	1.73	1.95	V	–
VT-	Negative-going Schmitt trigger threshold	1.05	1.25	1.53	V	–
Vhyst	Schmitt trigger hysteresis	0.36	0.48	0.54	V	–
IICS	Cold sparing leakage input current	-1	–	1	µA	Vcc=Vss=0V Vin=0 to Vcc
IOCS	Cold sparing leakage output current	-1	–	1	µA	Vcc=Vss=0V Vout=0 to Vcc
VCSth	Supply threshold of cold sparing buffers	–	–	0.5	V	IICS < 4µA
VOL	Low-level output voltage	–	–	0.4V	V	IOL=2, 4, 8, 12, 16 mA
VOH	High-level output voltage	VCC-0.4			V	IOH=2, 4, 8, 12, 16 mA
IOS(*)	Output short-circuit current IOSN (nn=1) IOSP (nn=1)	–	–	 23 23	 mA mA	 Vout=Vcc Vout=Vss
Fmax	Maximum frequency, C_{load} = 30 pF	–	–	15 70 105	MHz	nn = 1 nn = 4 nn = 8

(*) Supplied as a design limit but not guaranteed or tested. No more than one output may be shorted at a time for a maximum duration of 10 seconds.

IOSmax = 23, 46, 92, 138,184 mA for nn = 1, 2, 4 ,6, 8

8.6 5V I/O DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VCC	Buffer supply voltage	4.5	5.0	5.5	V	IOs

.....continued

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
IIL	Low-level input current – With pull-up resistor – With pull-down resistor	-1 180 -5	– 340 –	1 590 5	µA µA µA	Vin=Vss
IIH	High-level input current – With pull-up resistor – With pull-down resistor	-1 -5 160	– – 490	1 5 1000	µA µA µA	Vin=Vcc
IOZ	High impedance state output current	-1	–	1	µA	Vout=Vcc or Vss No pull resistor
VIL (TTL)	Low-level input voltage	-0.3	–	0.8	V	For TTL inputs
VIH (TTL)	High-level input voltage	2	–	Vcc+0.3	V	For TTL inputs
VIL (CMOS)	Low-level input voltage	-0.3	–	0.3*Vcc	V	For CMOS inputs
VIH (CMOS)	High-level input voltage	0.7*Vcc	–	Vcc+0.3	V	For CMOS inputs
VT+	Positive-going Schmitt trigger threshold	2.69	3.19	3.69	V	–
VT-	Negative-going Schmitt trigger threshold	1.81	2.20	2.70	V	–
Vhyst	Schmitt trigger hysteresis	0.77	0.99	1.1	V	–
IICS	Cold sparing leakage input current	-1	–	1	µA	Vcc=Vss=0V Vin=0 to Vcc
IOCS	Cold sparing leakage output current	-1	–	1	µA	Vcc=Vss=0V Vout=0 to Vcc
VCSth	Supply threshold of cold sparing buffers	–	–	0.5	V	IICS < 4 µA
VOL	Low-level output voltage	–	–	0.4V	V	IOL=2, 8, 16 mA
VOH	High-level output voltage	VCC-0.4	–	–	V	IOH=2, 8 ,16 mA
IOS(*)	Output short-circuit current IOSN (nn=1) IOSP (nn=1)	–	–	 40 40	 mA mA	 Vout=Vcc Vout=Vss
Fmax	Maximum frequency, C_{load} = 30 pF	–	–	11 43 68	MHz	nn = 1 nn = 4 nn = 8

(*) Supplied as a design limit but not guaranteed or tested. No more than one output may be shorted at a time for a maximum duration of 10 seconds.

IOSmax = 140, 420 mA for nn = 4 , 8

8.7 PCI Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VCC	Buffer supply voltage	3.0	3.3	3.6	V	IOs

.....continued						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
VIH	High-level input voltage	0.5 Vcc	–	Vcc + 0.3	V	–
VIL	Low-level input voltage	-0.3	–	0.3 VCC	V	–
IOH	High-level current	16	32	–	mA	VOH=Vcc - 0.4V
IOL	Low-level current	16	32	–	mA	VOL=0.4V
IOS(*)	Output short current	–	112	184	mA	VOH=0; VOL=Vcc
VCSTH	Supply threshold of cold sparing buffers	–	–	0.5	V	IICS < 4 µA

(*) Supplied as a design limit but not guaranteed or tested. No more than one output may be shorted at a time for a maximum duration of 10 seconds.

8.8 LVPECL Receiver Characteristics

DC Specifications

Applicable over recommended operating temperature and voltage ranges unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VCC	Buffer supply voltage	3.0	3.3	3.6	V	–
VCC	Buffer supply voltage	2.3	2.5	2.7	V	–
IIN	Input leakage	-10	–	10	µA	–
ICCstat	Static consumption (ien=0)	–	2.5	4	mA	VCC=3.3±0.3V
ICCstdby	Static consumption (ien=1)	–	–	10	µA	VCC=3.3±0.3V
ICCstat	Static consumption (ien=0)	–	1.5	2.3	mA	VCC=2.5±0.2V
ICCstdby	Static consumption (ien=1)	–	–	5.8	µA	VCC=2.5±0.2V

8.9 LVDS Reference Characteristics

DC Specifications

Applicable over recommended operating temperature and voltage ranges unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VCC	Buffer supply voltage	3.0	3.3	3.6	V	–
VCC	Buffer supply voltage	2.3	2.5	2.7	V	–
Vref	Input voltage	1.25 - 5%	1.25	1.25 + 5%	V	–
Rpd	Pull-down resistance	140	200	260	kOhm	VIN=1.25V
ICCstat	Static consumption (ien=0)	–	260	320	µA	VCC=3.3±0.3V
ICCstdby	Static consumption (ien=1)	–	–	2	µA	VCC=3.3±0.3V
ICCstat	Static consumption (ien=0)	–	150	184	µA	VCC=2.5±0.25V
ICCstdby	Static consumption (ien=1)	–	–	1.2	µA	VCC=2.5±0.25V

8.10 LVDS Transmitter Characteristics

DC Specifications

Applicable over recommended operating temperature and voltage ranges unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VCC	Buffer supply voltage	3.0	3.3	3.6	V	–
VCC	Buffer supply voltage	2.3	2.5	2.7	V	–
VOD*	Output differential voltage	247	350	454	mV	Rload = 100 ohms
VOS*	Output offset voltage	1.125	1.25	1.375	V	Rload = 100 ohms
|DVOD|*	Change in |VOD|	–	–	50		Rload = 100 ohms
|DVOS|*	Change in VOS - steady state Change in VOS - dynamic state	–	–	50 150	mV mV	Rload = 100 ohms
IOS*	Output short current	–	7 4.5	24 12	mA mA	Drivers shortened to ground or VCC Drivers shortened together
ICCstat	Static consumption (ien=0)	–	4	6	mA	VCC=3.3±0.3V
ICCstdby	Static consumption (ien=1)	–	–	10	µA	VCC=3.3±0.3V
ICCstat	Static consumption (ien=0)	–	2.3	3.5	mA	VCC=2.5±0.25V
ICCstdby	Static consumption (ien=1)	–	–	5.8	µA	VCC=2.5±0.25V
IOZ	High Impedance State Output	-1	–	1	µA	Vout=Vcc or Vss

Note: *: Meet or exceed TIA/EIA-644-A standard.

8.11 LVDS Receiver Characteristics

DC Specifications

Applicable over recommended operating temperature and voltage ranges unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VCC	Buffer supply voltage	3.0	3.3	3.6	V	–
VCC	Buffer supply voltage	2.3	2.5	2.7	V	–
VID*	Input differential voltage	100	–	600	mV	–
VCM*	Common mode input voltage	0.05	–	2.35	V	–
IIN*	Input leakage	-10	–	10	µA	–
ICCstat	Static consumption (ien=0)	–	3.5	6	mA	VCC=3.3±0.3V
ICCstdby	Static consumption (ien=1)	–	–	10	µA	VCC=3.3±0.3V
ICCstat	Static consumption (ien=0)	–	2	3.5	mA	VCC=2.5±0.25V
ICCstdby	Static consumption (ien=1)	–	–	5.8	µA	VCC=2.5±0.25V

Note: *: Meet or exceed TIA/EIA-644-A standard.

9. Support

Technical support is available by contacting aerospace@nto.atmel.com.

10. Revision History

Table 10-1. Revision History

Doc Rev.	Date	Comments
C	03/2021	Updated the following sections. • Radiation Hardness. • Absolute Maximum Ratings. • Recommended Operating Conditions. • LVDS Receiver Characteristics.
B	06/2020	Main content updates: • Introduction • Overview • Buffer Descriptions • Analog Blocks • Absolute Maximum Ratings • 2.5V I/O DC Characteristics • 3.3V I/O DC Characteristics • 5V I/O DC Characteristics • LVDS Transmitter Characteristics • LVDS Receiver Characteristics
A	08/2018	Main content updates: operating conditions, analog blocks, IO DC characteristics, radiation. Template update: Moved from Atmel to Microchip template. The datasheet is assigned a new document number (DS60001543) and revision letter is reset to A. ISBN number assigned.
44059 1.1	08/2016	Details on LVDS High Speed LVDS Buffers 655 Mbps according to the TIA/EIA-644-A std.
44059 1.0	01/2015	First issue.

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- Technical Support

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Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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