T-46-13-28

# 24C16

## 16K (8 x 256 x 8) CMOS Serial Electrically Erasable PROM

### FEATURES

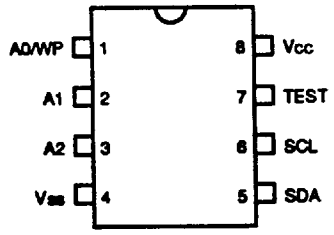
- Single supply with programming operation down to 4.5 volts
- Low power CMOS technology
  - 2 mA active current typical
  - 100 µA standby current at 5.5 V
- Organized as 8 blocks of 256 bytes (8 x 256 x 8)
- Two wire serial interface bus
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 16 bytes
- 2 ms typical write cycle time for page-write
- Hardware write protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000 V
- 10,000 erase/write cycles
- Data retention > 10 years
- 8 pin DIP or 14 pin SOIC package
- Available for extended temperature ranges
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C
  - Automotive: -40°C to +125°C

### DESCRIPTION

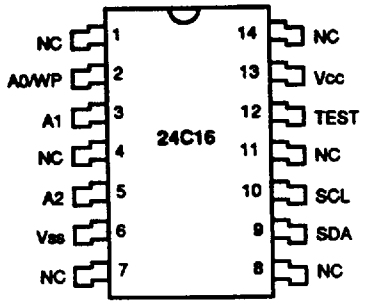
The Microchip Technology Inc. 24C16 is a 16K bit Electrically Erasable PROM. The device is organized as 8 blocks of 256 x 8 bit memory with a two wire serial interface. Advanced CMOS technology allows a significant reduction in power over NMOS serial devices. The 24C16 also has a page-write capability for up to 16 bytes of data. The 24C16 is available in the standard 8-pin DIP and a 14-pin surface mount SOIC package.

### PIN CONFIGURATION

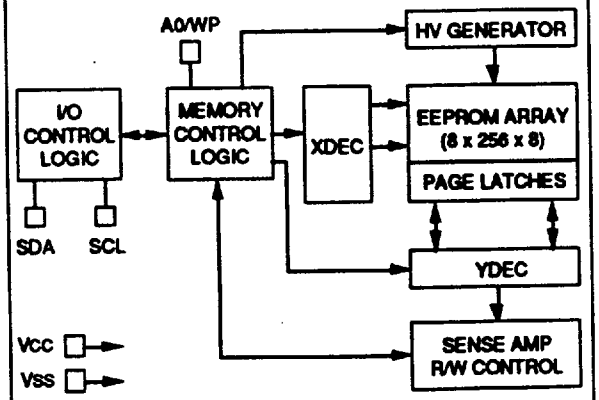
DIP Package




SO Package




### BLOCK DIAGRAM




**Preliminary Information**

## ELECTRICAL CHARACTERISTICS

**Maximum Ratings***

All inputs and outputs w.r.t. Vss .....-0.3 V to +6.25 V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) ..+300°C
ESD protection on all pins .....≥ 4 kV

*Notice: Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**PIN FUNCTION TABLE**

| Name | Function |
|---|---|
| A0/WP | Write Protect Input |
| A1, A2 | Grounded for Normal Operation |
| Vss | Ground |
| SDA | Serial Address/Data I/O |
| SCL | Serial Clock |
| TEST | Grounded for Normal Operation |
| Vcc | +5.0 V Power Supply |
| NC | No Connection |

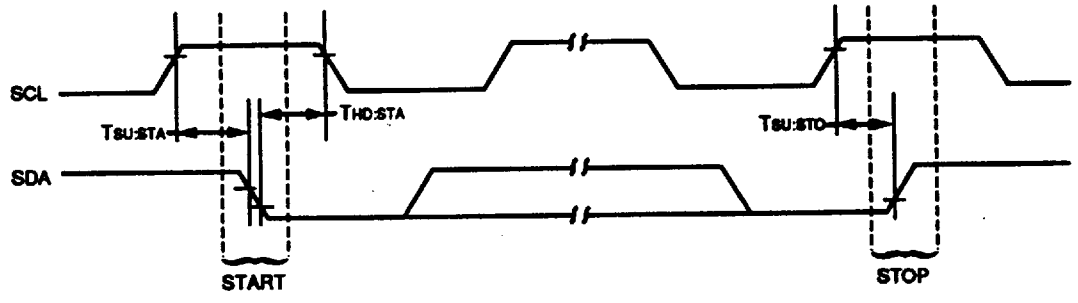
**DC CHARACTERISTICS**

Vcc = +5.0 V ± 10%
Commercial (C): Tamb = 0°C to +70°C
Industrial (I): Tamb = -40°C to +85°C
Automotive (E): Tamb = -40°C to +125°C

| Parameter | Symbol | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| A0/WP, SCL and SDA pins: High level input voltage | VIH | .7 Vcc | | V | |
| Low level input voltage | VIL | | .3 Vcc | V | |
| Low level output voltage | VOL | | .40 | V | IOL = 3.2 mA Vcc = 2.5 V |
| Input leakage current | ILI | -10 | 10 | µA | VIN = .1 V to Vcc |
| Output leakage current | ILO | -10 | 10 | µA | VOUT = .1 V to Vcc |
| Internal capacitance (all inputs/outputs) | CINT | | 10 | pF | Vcc = 5.0 V (Note 1) Tamb = 25°C, FCLK = 1 MHz |
| Operating current | ICCO | | 3 | mA | Vcc = 5.5 V SCL = 100 KHz |
| Standby current | ICCS | | 100 | µA | Vcc = 5.5 V SDA = SCL = Vcc |

Note 1: This parameter is periodically sampled and not 100% tested.

**BUS TIMING START/STOP**



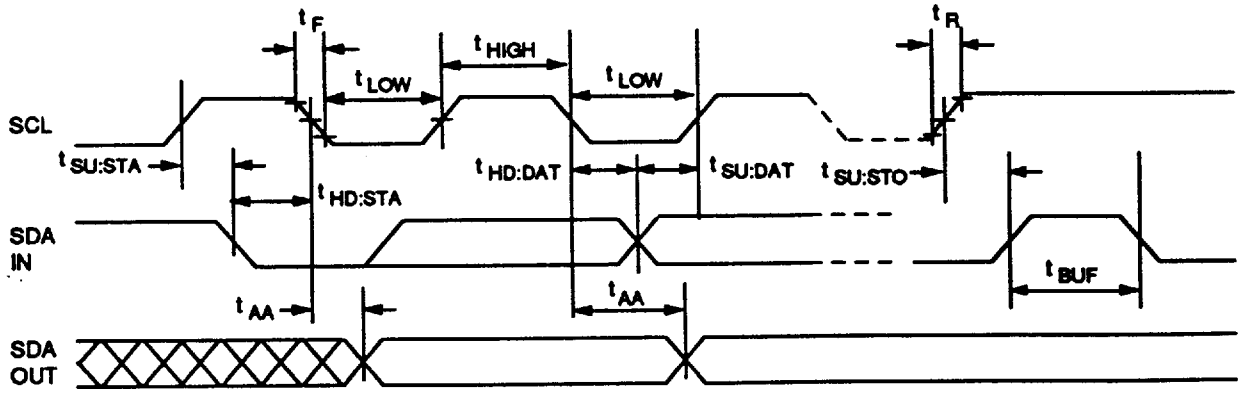
## AC CHARACTERISTICS

| Parameter | Symbol | Min | Typ | Max | Units | Remarks |
|---|---|---|---|---|---|---|
| Clock frequency | FCLK | | | 100 | kHz | |
| Clock high time | THIGH | 4000 | | | ns | |
| Clock low time | TLOW | 4700 | | | ns | |
| SDA and SCL rise time | TR | | | 1000 | ns | |
| SDA and SCL fall time | TF | | | 300 | ns | |
| START condition hold time | THD:STA | 4000 | | | ns | After this period the first clock pulse is generated |
| START condition setup time | TSU:STA | 4700 | | | ns | Only relevant for repeated START condition |
| Data input hold time | THD:DAT | 0 | | | ns | |
| Data input setup time | TSU:DAT | 250 | | | ns | |
| STOP condition hold time | THD:STO | 4000 | | | ns | |
| STOP condition setup time | TSU:STO | 4700 | | | ns | |
| Output valid from clock | TAA | 300 | | 3500 | ns | See Note 1 |
| Bus free time | TBUF | 4700 | | | ns | Time the bus must be free before a new transmission can start |
| Input filter time constant (SDA and SCL pins) | TI | | | 100 | ns | |
| Write cycle time | TWR | | 2 | 10 | ms | Byte or Page mode |

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

Note 2: When writing data to the 24C16, an automatic internal erase then write cycle is executed.

## BUS TIMING DATA



## FUNCTIONAL DESCRIPTION

The 24C16 supports a bidirectional two wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24C16 works as slave. Both, master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

## BUS CHARACTERISTICS

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (see Figure 1):

### Bus not Busy (A)

Both data and clock lines remain HIGH.

### Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

### Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

### Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last sixteen will be stored when doing a write operation. When an overwrite does occur it will replace data in a first in first out fashion.

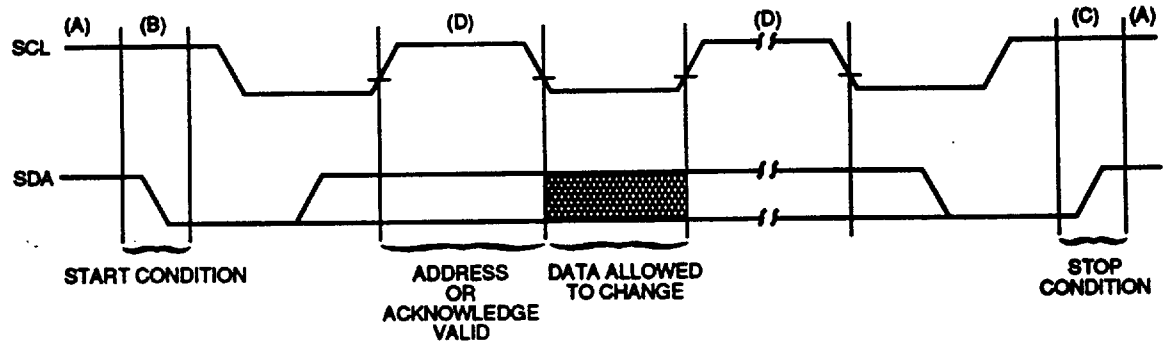
### Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note: The 24C16 does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

**FIGURE 1 - DATA TRANSFER SEQUENCE ON THE SERIAL BUS**



## BUS CHARACTERISTICS

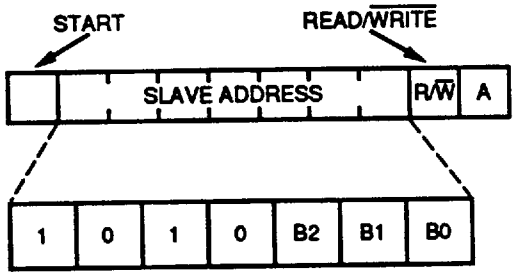
### Device Addressing and Operation

A control byte is the first byte received following the start condition from the master device. The control byte consists of a four bit control code, for the 24C16 this is set as 1010 binary for read and write operations. The next three bits of the control byte are the block select bits (B2, B1, B0). They are used by the master device to select which of the eight 256 word blocks of memory are to be accessed. These bits are in effect the three most significant bits of the word address. It should be noted that the protocol limits the size of the memory to eight blocks of 256 words, therefore the protocol can support only one 24C16 per system.

The last bit of the control byte defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected. Following the start condition, the 24C16 monitors the SDA bus checking the device type identifier being transmitted, upon a 1010 code the slave device outputs an acknowledge signal on the SDA line. Depending on the state of the R/W bit, the 24C16 will select a read or write operation.

| Operation | Control Code | Block Select | R/$\overline{W}$ |
|---|---|---|---|
| Read | 1010 | Block Address | 1 |
| Write | 1010 | Block Address | 0 |

**FIGURE 2 - CONTROL BYTE ALLOCATION**




## WRITE OPERATION

### Byte Write

Following the start condition from the master, the device code (4 bits), the block address (3 bits), and the R/$\overline{W}$ bit which is a logic low is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the 24C16. After receiving another acknowledge signal from the 24C16 the master device will transmit the data word to be written into the addressed memory location. The 24C16 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24C16 will not generate acknowledge signals. (See Figure 3).

### Page Write

The write control byte, word address and the first data byte are transmitted to the 24C16 in the same way as in a byte write. But instead of generating a stop condition the master transmits up to sixteen data bytes to the 24C16 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the four lower order address pointer bits are internally incremented by one. The higher order seven bits of the word address remains constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin. (See Figure 4).

**FIGURE 3 - BYTE WRITE**

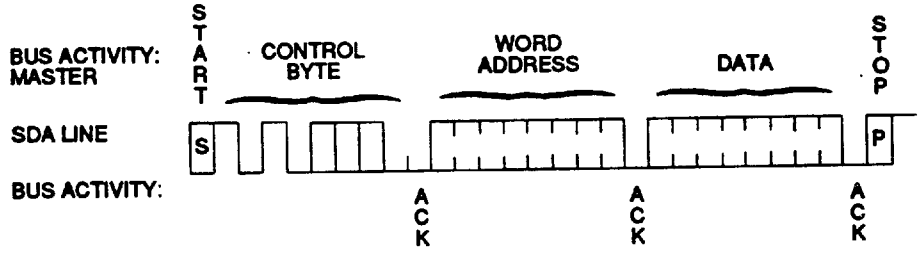


**FIGURE 4 - PAGE WRITE**

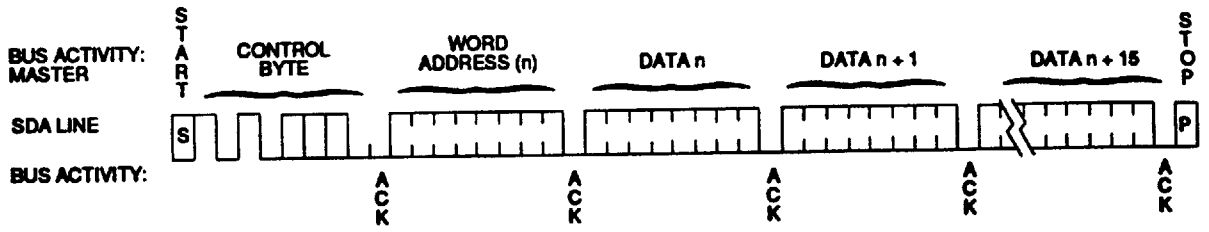



**FIGURE 5 - CURRENT ADDRESS READ**

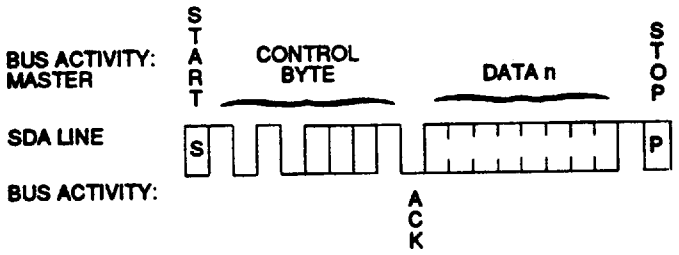



**FIGURE 6 - RANDOM READ**

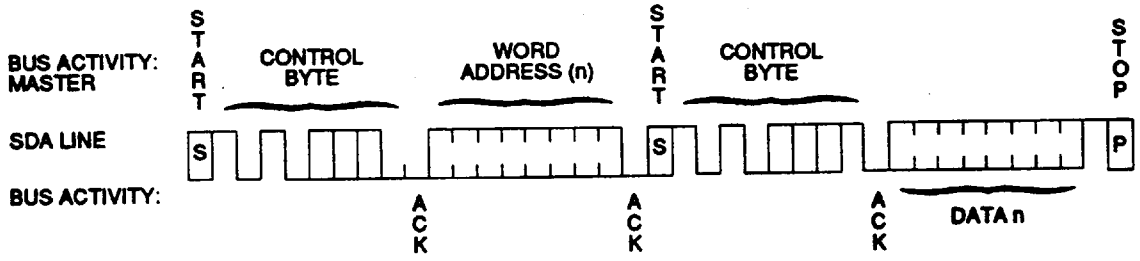
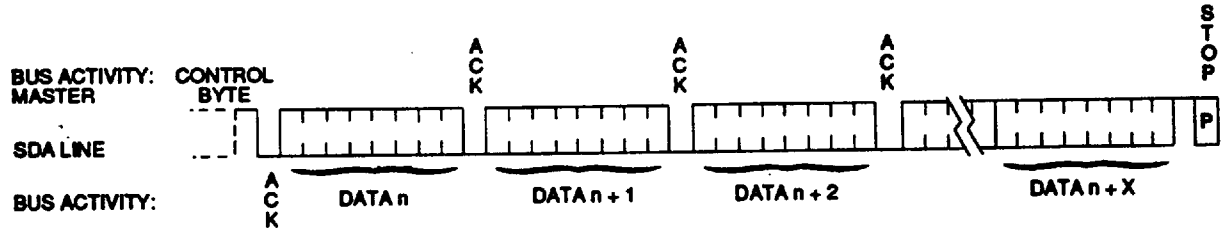



**FIGURE 7 - SEQUENTIAL READ**



## WRITE PROTECTION

The 24C16 can be used as a serial ROM when WP pin is connected to Vcc (+5V). Programming will be inhibited and the entire memory (2K bytes) will be write-protected.

## READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

### Current Address Read

The 24C16 contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ bit set to one, the 24C16 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24C16 discontinues transmission. (See Figure 5).

### Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24C16 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The 24C16 will then issue an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24C16 discontinues transmission. (See Figure 6).

### Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24C16 transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24C16 to transmit the next sequentially addressed 8 bit word. (See Figure 7).

To provide sequential reads the 24C16 contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

### Noise Protection

The SCL and SDA inputs have filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

## PIN DESCRIPTIONS

### A0/WP Write Protect Input

This pin must be connected to either Vss or Vcc.

If tied to Vcc, WRITE operations are inhibited. The entire 2K bytes memory will be write-protected. Read operations are possible.

If tied to Vss, normal memory operation is enabled (read/write the entire memory 000-7FF).

This feature allows the user to use the 24C16 as a serial ROM when WP is enabled (tied to Vcc).

### A1, A2 Chip Address Inputs

The A1 and A2 inputs are unused by the 24C16. They must be connected to Vss to insure proper device operation.

### SDA Serial Address/Data Input/Output

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal.

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

### SCL Serial Clock

This input is used to synchronize the data transfer from and to the device.

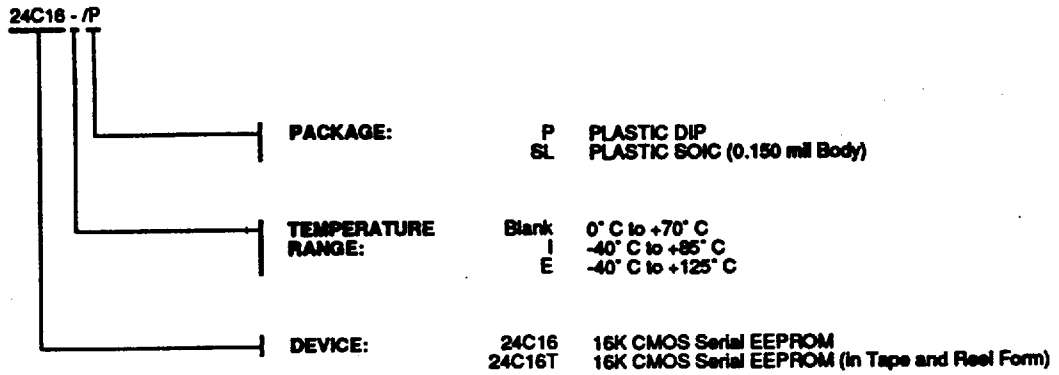
### TEST

This pin must be connected to Vss.

## SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

### PART NUMBERS

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