ADVANCE INFORMATION

DRX 3960A
Digital Receiver
Front-end

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6251-510-2AI

MICRONAS

Contents

Contents, continued

Digital Receiver Front-end

Release Note: Revision bars indicate significant changes to the previous edition.

1. Introduction

The Digital Receiver Front-end DRX 3960A performs the entire multistandard Quasi Split Sound (QSS) TV IF processing, AGC, video demodulation, and generation of the second sound IF (SIF) with only one SAW filter. The IC is designed for applications in TV sets, VCRs, PC cards, and TV tuners.

The alignment-free DRX 3960A needs no special external components. All control functions and status registers are accessible via I^2C bus interface. Therefore, it simplifies the design of high-quality, highly standardized IF stages.

Due to its mixed signal structure and the digital demodulation, the IC offers unique features and is prepared for digital TV.

1.1. Features

- Multistandard QSS IF processing with a single SAW
- Highly reduced amount of external components (no tank circuit, no potentiometers, no SAW switching)
- Programmable IF frequency (38.9 MHz, 45.75 MHz, 32.9 MHz, 36.125 MHz etc.)
- Digital IF processing for the following standards: B/G, D/K, I, L/L', and M/N
- Standard specific digital post filtering
- Standard specific digital video/audio splitting
- Standard specific digital picture carrier recovery:
  - alignment-free
  - quartz-stable and accurate
  - stable frequency lock at 100% modulation and overmodulation up to 150%
  - quartz-accurate AFC information
- Programmable standard specific digital group delay equalizing
- Automatically frequency-adjusted Nyquist slope, therefore optimal picture and sound performance over complete lock in frequency range
- Standard-specific digital AGC and delayed tuner AGC with programmable tuner Take Over Point
- Fast AGC due to linear structure
- Adaptive back porch control, therefore fast positive modulation AGC
- No sound traps needed at video output
- Second SIF output with standard dependent pre-filtering and amplitude controlled output level
- Optimal sound SNR due to carrier recovery without quadrature distortions
- FM radio capability without external components and with standard TV tuner
- Prepared for digital TV (DVB-C, DVB-T, ATSC)
- I^2C bus interface

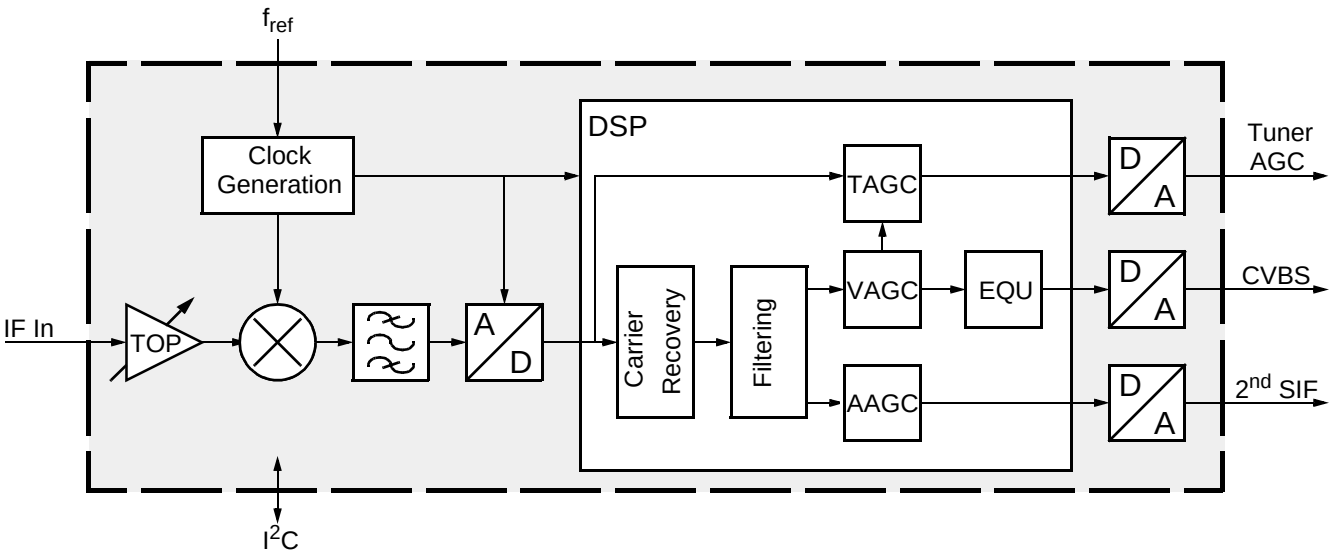


Fig. 1–1: Block diagram of the DRX 3960A

1.2. Quick Reference Data

Parameter	Min.	Typ.	Max.	Unit	Remarks
Supply voltage, analog		5		V	
Current consumption, analog		110		mA	
Supply voltage, digital		3.3		V	
Current consumption, digital		60		mA	
Input frequency	30		47	MHz	
Maximum wanted signal input voltage minimum TOP gain: maximum TOP gain:		 200 20		 mV_{pp} mV_{pp}	
Lock in range	0.8 1.0			MHz MHz	direction adjacent channel direction own channel center freq. quartz stable
Intermodulation ratio $\alpha_{1.07}$	65			dB	blue picture, P_{SC1}=–13dB, no sound shelf
Weighted video S/N (CCIR567, 10 kHz...5 MHz)	56	58		dB	
Unweighted video S/N (10 kHz...5 MHz)	49	51		dB	
Weighted sound S/N (black, CCIR468 quasi peak, SC1/SC2)		62/58		dB	dev. = 27 kHz
Weighted sound S/N (FuBK, CCIR468 quasi peak, SC1/SC2)		55/50		dB	dev. = 27 kHz
CVBS output voltage		2		V_{pp}	programmable
Second IF output voltage		0.8		V_{pp}	programmable
Delayed Tuner AGC external voltage			8	V	

1.3. Analog TV Application

The Digital Receiver Front-end DRX 3960A is able to replace a conventional IF IC including several SAWs. Nevertheless, quasi split sound processing is performed with standard specific internal filtering and group delay equalizing.

The input signal of the DRX 3960A is the TV IF with its carrier at:

- 38.9 MHz (B/G, D/K, I, L, and M/N in multistandard applications)
- 32.9 MHz (L')
- 45.75 MHz (M/N in single standard applications)
- other frequencies are also programmable
- 36.125 MHz (DVB-C or DVB-T in further versions)

These signals are available from conventional tuners. For pre-filtering, one 8-MHz channel SAW filter must be used, e.g. the Epcos X6966M. Nevertheless, the entire multistandard processing is performed. The pre-filter limits the signal bandwidth to 8 MHz and suppresses major parts of the adjacent channels.

After the desired standard information is transferred into the DRX 3960A, the following standard specific procedures are performed:

- Adjacent channel suppression
- Carrier locking including AFC information generation
- Nyquist slope adjustment
- Video/sound splitting
- Video AGC, including delayed tuner AGC
- Group delay post distortion
- Video and sound frequency shaping
- Video demodulation
- Second SIF generation and AGC

Similar to conventional analog front-ends, the tuner gain is controlled by the DRX 3960A. New AGC algorithms have been implemented for superior level tracking for both positive and negative video modulation.

The demodulated CVBS signal and the second sound IF (SIF) are available as analog output signals.

If an FM radio channel is transferred to the IF inputs, down-mixed by means of a standard TV tuner, it can be preselected and further down-mixed by the DRX 3960A. Thus, a succeeding sound demodulator, e.g. the MSP, will be able to demodulate that channel.

The DRX 3960A operates with its own quartz or with appropriate external clocks, e.g.:

- 13.5, 20.25, 27 MHz from an employed video IC
- 1, 4 MHz from the tuner

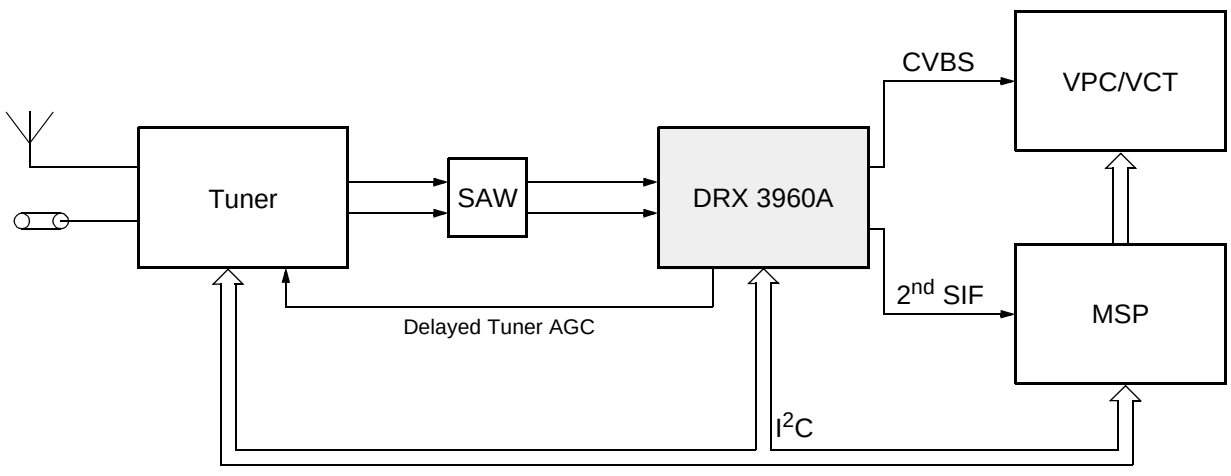


Fig. 1–2: Multistandard video and sound IF processing with DRX 3960A

1.3.1. Initialization for Analog TV

The DRX 3960A is able to operate with different reference frequencies. If 20.25 MHz is used, REF_SW has to be connected to ground; additionally, if a lower frequency is used, SYN_REF (control register) has to be set accordingly. If a higher frequency is used, REF_SW has to be connected to V_{DVDD} and SYN_REF has to be set accordingly. In the 20.25 MHz case, no I^2C command is needed.

The standard which should be processed has to be set via I^2C bus.

Additional controlling is only needed if the default values for the remaining write registers are not applicable.

1.3.2. Multistandard Configuration for B/G, L, I, D/K and M/N

In multistandard applications for B/G, L, I, D/K, and M/N, the picture carrier frequency at the tuner output should be 38.9 MHz. The sound carrier frequencies are below in a distance corresponding to the transmission standard. Thus, all wanted channel components are within the passband of the SAW and forwarded to the DRX 3960A. The demodulated and filtered video signal will be available at the CVBS output and the down-converted sound carriers will be available at the 2nd SIF output.

1.3.3. Multistandard Configuration for L'

In the L standard, the band 1 channels (40 MHz to 65 MHz) have a different frequency configuration. Their sound carriers are below the according picture carrier. This sub-standard is called L'. In that case, the picture carrier frequency at the tuner output should be 32.9 MHz. Using conventional tuners, the sound carrier frequencies in L' at the tuner output are above the picture carrier. Thus, again all wanted channel components are within the passband of the SAW.

1.3.4. FM Radio

In FM radio applications, the tuner has to down-convert the wanted channel to 32.4 MHz. Therefore, the lower slope of the SAW frequency response rejects adjacent carriers on one side of that channel. The DRX 3960A further down-converts the wanted channel to 5.5 MHz. After additional filtering, the signal is fed to the 2nd SIF output.

2. Functional Description

2.1. Input Amplifier with TOP Setting

The first block of the DRX 3960A is a low-noise pre-amplifier. It has a setable gain between 0 and 20 dB for setting the Tuner take Over Point voltage (TOP). This adjustment is responsible for optimal tuner operation.

Note: The TOP is the tuner input voltage at which the IF circuit (e.g. the DRX 3960A) begins to reduce the tuner gain. Thus, above this voltage the tuner output voltage remains nearly constant. Of course, the gain of the tuner is only allowed to be reduced if the S/N is sufficiently high. A level of 60...70 dBµV at the antenna input is a typical value for the starting point of gain reduction.

2.2. Carrier Recovery

A digital PLL performs the tracking of the picture carrier and therefore synchronous demodulation.

The lock in range refers to the desired IF frequency which is chosen according to the programmed TV standard (e.g. 32.9 MHz at L' or 38.9 MHz at all other standards).

The PLL incorporates its own AFC function and provides the frequency offset from the desired IF frequency for external use (CR_FREQ). A special digital validation algorithm allows long frequency lock at 100% modulation. Additionally, the PLL aligns the digital calculated Nyquist slope to the picture carrier frequency.

Due to its digital implementation, the carrier recovery is absolutely offset-free, alignment-free, drift-free, and quartz-accurate.

2.3. Channel Filtering and Audio/Video Splitting

According to the selected standard, channel filtering (suppression of not wanted signals) is performed internally by digital filters. These filters additionally separate the video and sound components of the desired channel and transfer them to the according output. The processing is competitive to conventional QSS systems.

2.4. Video and Tuner AGC

The video AGC controls the CVBS amplitude to a given value (VID_AMP). This value may be set via I^2C bus.

In positive modulation mode, an adaptive back porch control (BPC) is activated. If the detected BP reference is higher than 38% of the CVBS amplitude, or lower than 17%, it is set to the according limit.

If the video AGC gain is to low, the tuner AGC increases its output current. Thus, the tuner reduces its gain.

The actual gain value of both control loops can be read out (VID_GAIN, TAGC_I) as information about the input signal strength.

2.5. Group Delay Equalizing

The group delay is set to compensate the pre-distortion of the transmitter. Additionally, the standard settings can be changed by means of four coefficients to optimize the complete signal path (EQU_0, EQU_1, EQU_2, EQU_3).

2.6. Peaking

To shape the frequency response, a peaking filter is implemented. The following figure indicates the possible frequency responses:

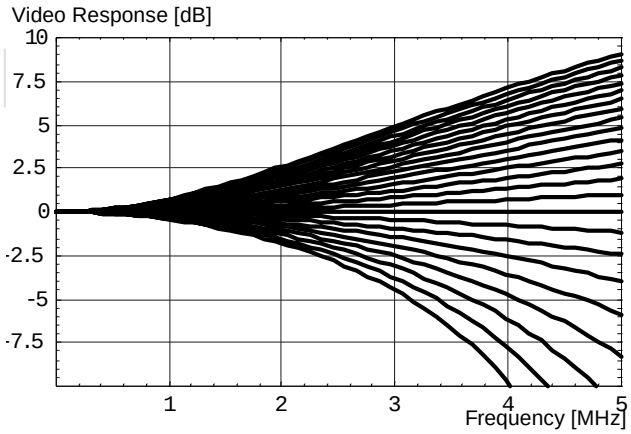


Fig. 2–1: Peaking filter frequency response

The peaking value is setable via I^2C (VID_PEAK).

2.7. SIF AGC

The SIF AGC controls the level of the sound carrier output. Four different reference amplitude values are available (SIF_REF) .
The actual gain (SIF_GAIN) can be read out and set via I^2C.

According to the standard, the time constant is switched to FM/NICAM (fast AGC) or AM (slow AGC).

2.8. Output Ports

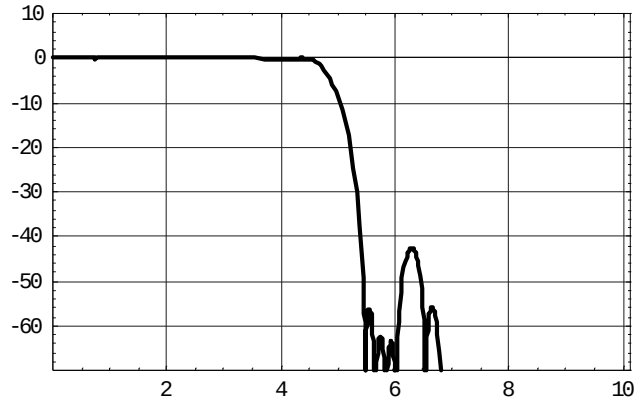
Six general purpose output ports can be switched to high or low level.

3. Standard Specific Filter Curves

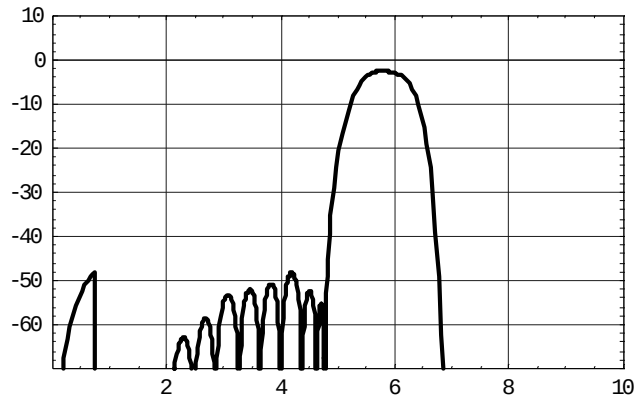
The external SAW only performes a coarse attenuation of major parts of adjacent channels. The main filtering is done by means of the DSP. The following figures indicate the overall filter curves of the DRX 3960A including the SAW.

3.1. Standard B

Video Response [dB]

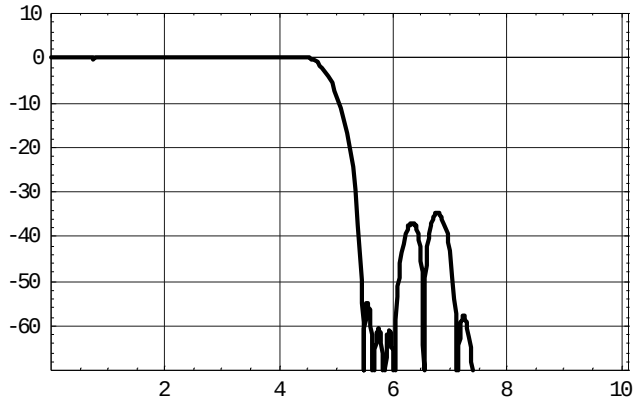


SIF Response [dB]

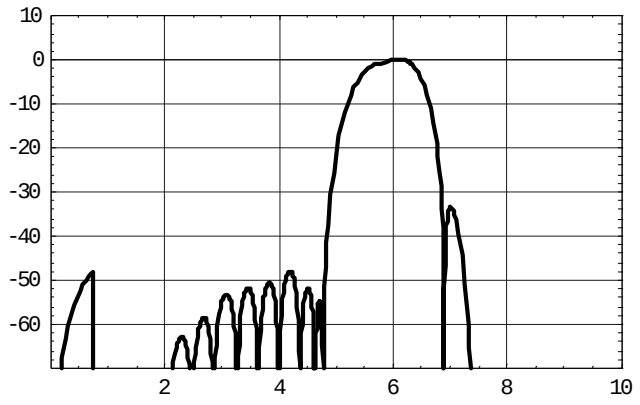


3.2. Standard G

Video Response [dB]

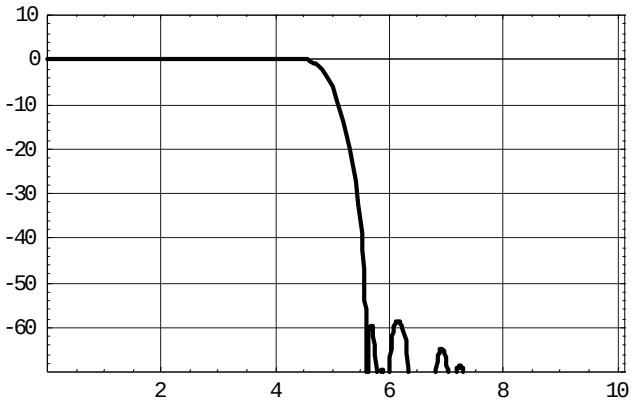


SIF Response [dB]

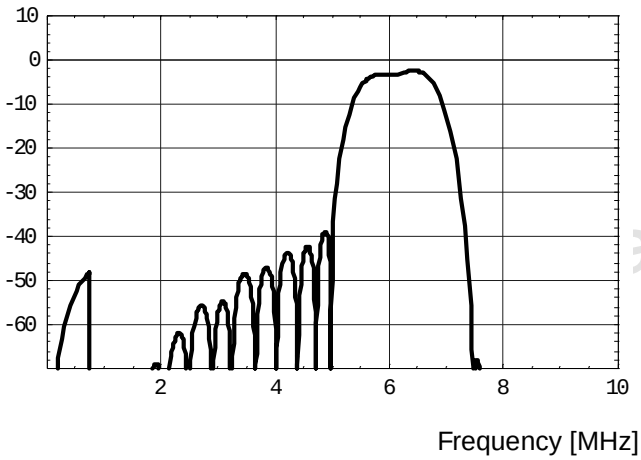


3.3. Standard D/K, I, L/L'

Video Response [dB]

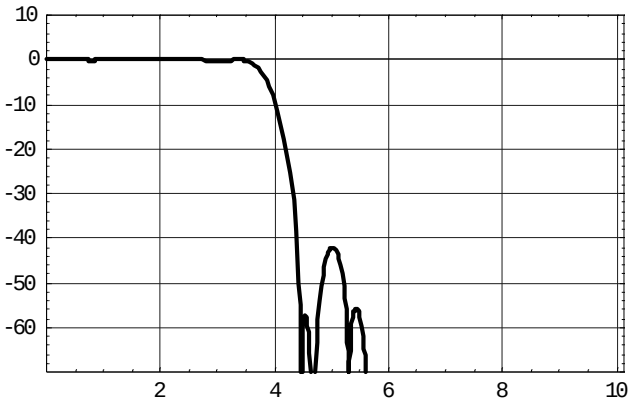


SIF Response [dB]

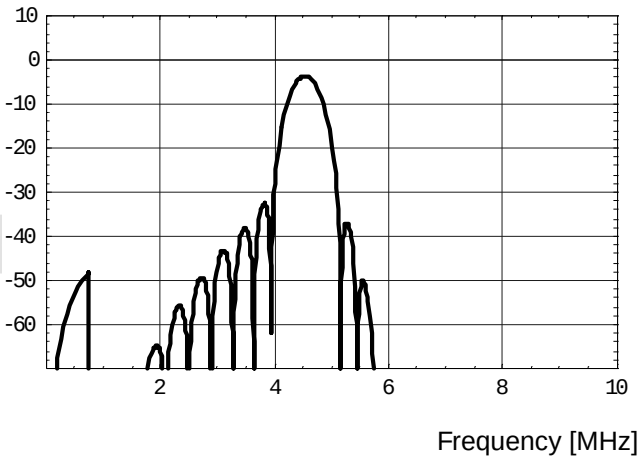


3.4. Standard M/N

Video Response [dB]

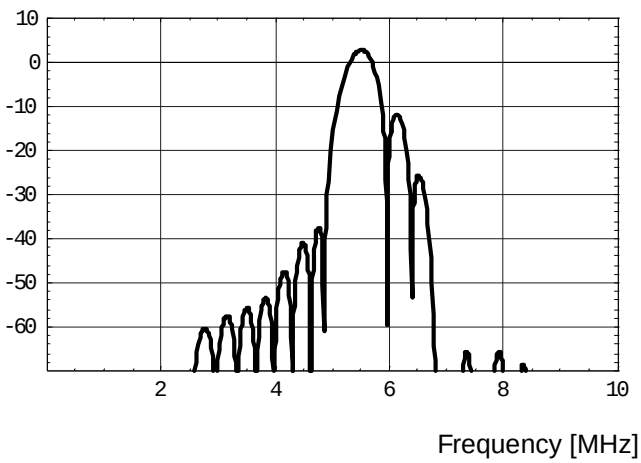


SIF Response [dB]



3.5. Standard FM

SIF Response [dB]



4. Control Interface

4.1. I²C Bus Interface

4.1.1. Device and Subaddresses

The DRX 3960A is controlled via the I²C bus slave interface.

The IC is selected by transmitting one of the DRX 3960A device addresses. In order to allow up to three ICs to be connected to a single bus, an address select pin (ADR_SEL) has been implemented. With ADR_SEL pulled to high, low, or left open, the DRX 3960A responds to different device addresses. A device address pair is defined as a write address and a read address.

Writing is done by sending the device write address, followed by the subaddress byte, two address bytes, and two data bytes. Reading is done by sending the write device address, followed by the subaddress byte and two address bytes. Without sending a stop condition, reading of the addressed data is completed by sending the device read address and reading two bytes of data.

Due to the internal architecture of the DRX 3960A, the IC cannot react immediately to an I²C request. The typical response time is about 0.3 ms. If the DRX 3960A cannot accept another complete byte of data until it has performed some other function (for example, servicing an internal interrupt), it will hold the clock line low to force the transmitter into a wait state. The maximum wait period during normal operation mode is less than 1 ms.

Table 4–1: I²C Bus Device Addresses

ADR_SEL	Low		High		Left Open	
Mode	**Write**	**Read**	**Write**	**Read**	**Write**	**Read**
Device address	82_{hex}	83_{hex}	86_{hex}	87_{hex}	$8A_{hex}$	$8B_{hex}$

Table 4–2: I²C Bus Subaddresses

Name	Binary Value	Hex Value	Mode	Function
CONTROL	0000 0000	00	Read/Write	Write : Software reset of DRX Read : Hardware error status of DRX
PORT	0000 0011	03	Write	output port address
WR_DRX	0001 0000	10	Write	write address
RD_DRX	0001 0001	11	Write	read address

4.1.2. Description of CONTROL Register

Table 4–3: CONTROL as a Write Register

Name	Subaddress	Bit[15] (MSB)	Bits[14:0]
CONTROL	00_{hex}	1 : RESET 0 : normal	0

Table 4–4: CONTROL as a Read Register

Name	Subaddress	Bit[15] (MSB)	Bit[14]	Bits[13:0]
CONTROL	00_{hex}	Reset status after last reading of CONTROL: 0 : no reset occurred 1 : reset occurred	Internal hardware status: 0 : no error occurred 1 : internal error occurred	not of interest
Reading of CONTROL will reset the bits[15,14] of CONTROL. After Power-on, bit[15] of CONTROL will be set; it must be read once to be reset.				

4.1.3. Protocol Description

Write protocol

S	write device address	Wait	ACK	sub-addr	ACK	addr-byte high	ACK	addr-byte low	ACK	data-byte-high	ACK	data-byte low	ACK	P

Read protocol

S	write device address	Wait	ACK	sub-addr	ACK	addr-byte high	ACK	addr-byte low	ACK	S	read device address	Wait	ACK	data-byte-high	ACK	data-byte low	NAK	P

Write to Control or Test Registers

S	write device address	Wait	ACK	sub-addr	ACK	data-byte high	ACK	data-byte low	ACK	P

Write to Port Registers

S	write device address	Wait	ACK	sub-addr	ACK	data-byte	ACK	P

Note: S = I^2C bus Start Condition from master
P = I^2C bus Stop Condition from master
ACK = Acknowledge-Bit: LOW on I2C_DA from slave (= DRX, light gray) or master (= controller dark gray)
NAK = Not Acknowledge-Bit: HIGH on I2C_DA from master (dark gray) to indicate ‘End of Read’ or from DRX indicating internal error state
Wait = I^2C clock line is held low, while the DRX is processing the I^2C command. This waiting time is max. 1 ms

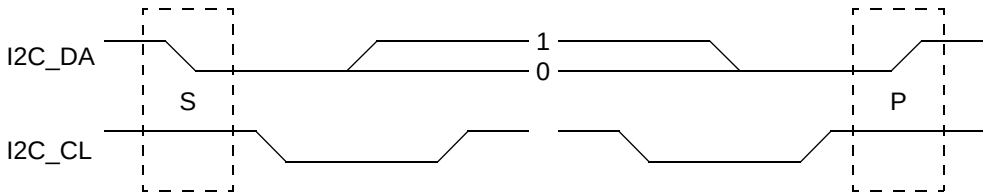


Fig. 4–1: I^2C bus protocol (MSB first; data must be stable while clock is high)

4.1.4. Proposals for General DRX 3960A I²C Telegrams

4.1.4.1. Symbols

`daw` write device address (82_{hex}, 86_{hex} or $8A_{hex}$)
`dar` read device address (83_{hex}, 87_{hex} or $8B_{hex}$)
`<` Start Condition
`>` Stop Condition
`aa` Address Byte
`dd` Data Byte

4.1.4.2. Write Telegrams

`<daw 00 d0 00>` write to CONTROL register
`<daw 10 aa aa dd dd>` write data into DRX

4.1.4.3. Read Telegrams

`<daw 11 aa aa <dar dd dd>` read data from DRX

4.2. List of Control Registers

Table 4–5: List of Control Registers

Write Register	Address (hex)	Bits	Description	Reset (hex)
I²C Subaddress = 03_{hex} ; Register is not readable.				
Output ports	no	[5:0]	Output level of Ports	0
I²C Subaddress = 10_{hex} ; Register are not readable.				
Standard select	00 20	[11:0]	Transmission standard	01 03
Level settings	10 01	[9:0]	[VID_PEAK, SIF_REF, VID_AMP]	
Reference divider	10 10	[8:0]	[for 4 MHz, 13 MHz, 20.25 MHz, 27 MHz or other REF_SW = high REF_SW = low]	 10D 0CA
Tuner take over point	10 12	[3:0]	[0 dB ... 20 dB]	3
Equalizer Coe. 0	10 70	[9:0]	Equalizer coefficient	025
Equalizer Coe. 1	10 71	[8:0]	Equalizer coefficient	197
Equalizer Coe. 2	10 72	[8:0]	Equalizer coefficient	0C5
Equalizer Coe. 3	10 73	[8:0]	Equalizer coefficient	12E

4.3. List of Status Registers

Table 4–6: List of Status Registers

Read Register	Address (hex)	Bits	Description
I²C Subaddress = 11_{hex} ; Register are not writable			
VIDEO_GAIN	10 05	[10:0]	Actual gain of the video AGC
TAGC_I	10 06	[11:0]	Actual tuner current
SIF_GAIN	10 0A	[10:0]	Internal actual gain of the SIF AGC
CR_FREQ	10 0B	[8:1]	Frequency deviation referred to reference IF frequency

4.4. Description of User Registers

4.4.1. Write Register on I²C Subaddress 03_{hex}

Table 4–7: Write Register on I²C Subaddress 03_{hex}

I²C-Sub-address (hex)	Function	Name
no	**Output Port Level** bit[5] Level at output port 5 bit[4] Level at output port 4 bit[3] Level at output port 3 bit[2] Level at output port 2 bit[1] Level at output port 1 bit[0] Level at output port 0	PORT

4.4.2. Write Register on I^2C Subaddress 10_{hex}

Table 4–8: Write Register on I^2C Subaddress 10_{hex}

I^2C-Sub-address (hex)	Function	Name
00 20	**Standard select** Defines TV standard which is to be processed bit[15:0] 00 00_{hex} reserved 00 01_{hex} reserved 00 02_{hex} M/N 01 03_{hex} B (default) 00 03_{hex} G 00 04_{hex} D/K 00 09_{hex} L 01 09_{hex} L' 00 $0A_{hex}$ I 00 40_{hex} FM	STANDARD_SEL
10 01	**Level settings** Defines the different output levels and frequency response bit[4:0]Video frequency response deviation at 5 MHz –8 –11.0 dB –7 –9.0 dB ... ... –2 –2.1 dB –1 –1.0 dB 0 0 dB 1 0.8 dB (default) 2 1.5 dB 3 2.1 dB ... ... 14 8.1 dB 15 8.3 dB bit[6:5] Reference value for SIF maximum amplitude: 0 1000 mV_{pp}(default) 1 700 mV_{pp} 2 500 mV_{pp} 3 350 mV_{pp} bit[8:7] Reference value for video amplitude 0 2.0 V (default) 1 1.5 V 2 1.0 V 3 0.7 V	VID_PEAK SIF_REF VID_AMP

Table 4–8: Write Register on I^2C Subaddress 10_{hex}

I^2C-Sub-address (hex)	Function	Name
10 10	**Reference divider setting** The DRX 3960A is able to operate with different reference frequencies. The reference divider has to be set to the value which divides the reference frequency to 100 kHz. To prevent malfunction after POR, the default value is set for f_{ref} = 27 MHz, if the pin REF_SW is connected to V_{DVDD} or set for f_{ref} = 20.25 MHz, if the pin REF_SW is connected to GND. bit[8:0] External_Ref_Freq / 100 kHz 27 MHz $10D_{hex}$ 20.25 MHz CA_{hex} 4 MHz 28_{hex}	SYN_REF
10 12	**Tuner Take Over Point (TOP) setting** Defines the gain of the internal preamplifier to set the TOP bit[3:0] Gain of Preamplifier 0 0 dB 1 1.33 dB 2 2.67 dB ... 8 10 dB (default) ... 14 18.67 dB 15 20 dB	TOP_SET
10 70	**Equalizer coefficient 0** bit[9:1] Coefficient bit[0] Update bit 0 do not update coefficients 1 update coefficients	EQU_0
10 71	**Equalizer coefficient 1** bit[8:0] Coefficient	EQU_1
10 72	**Equalizer coefficient 2** bit[8:0] Coefficient	EQU_2
10 73	**Equalizer coefficient 3** bit[8:0] Coefficient	EQU_3

4.4.3. Read Register on I^2C Subaddress 11_{hex}

Table 4–9: Read Register on I^2C Subaddress 11_{hex}

I^2C-Sub-address (hex)	Function	Name
10 05	**Actual gain of video AGC** bit[10:0] Video gain 0.05 dB/LSB 0dB = $C8_{hex}$	VID_GAIN
10 06	**Actual gain of tuner AGC** bit[10:0] Tuner current 0.4 µA/LSB	TAGC_I
10 0A	**Actual gain of SIF AGC** bit[10:0] SIF gain 0.05 dB/LSB 0dB = $C8_{hex}$	SIF_GAIN
10 0B	**AFC** bit[8:1] Frequency deviation10 kHz/LSB bit[0] Lock bit: 1 : Carrier Recovery locked 0 : Carrier Recovery unlocked	CR_FREQ
10 0C	**Lock Quality** bit[10:0] < 080_{hex} strong signal 080_{hex}...700_{hex} weak signal > 700_{hex} no signal	CR_LOCK

5. Specifications

5.1. Outline Dimensions

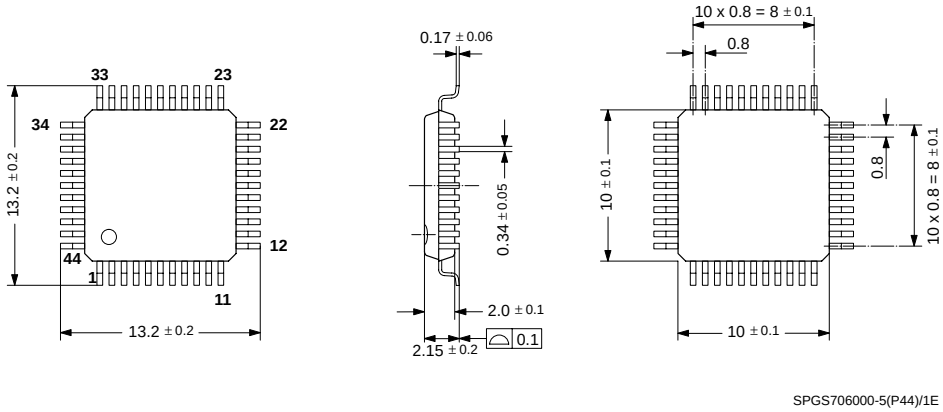


Fig. 5–1:
44-Pin Plastic Metric Quad Flat Pack
(PMQFP44)
Weight approximately 0.4 g
Dimensions in mm

5.2. Pin Connections and Short Descriptions

NC = not connected, leave vacant
LV = if not used, leave vacant
DVSS = if not used, connect to DVSS

X = obligatory; connect as described in circuit diagram
AHVSS = connect to AHVSS

Pin No.	Pin Name	Type	Supply Voltage	Connection (If not used)	Short Description
1	AVSS_ADC			X	Analog ground for ADC
2	AVDD_ADC			X	Analog supply for ADC (+5 V)
3	ANATSTX	I/O	AVDD_FE8	GND	Test pin
4	ANATSTY	I/O	AVDD_FE8	GND	Test pin
5	AVDD_FE8			X	2nd analog supply for the front-end
6	AVSS_FE8			X	2nd analog ground for the front-end
7	AVSS_FE40			X	1st analog ground for the front-end
8	IFINX	IN	AVDD_FE40	X	IF input
9	AVDD_FE40			X	1st analog supply for the front-end (+5 V)
10	IFINY	IN	AVDD_FE40	X	IF input
11	AVSS_FE40			X	1st analog ground for the front-end
12	AVDD_SYN			X	Analog supply for synthesizer (+5 V)
13	AVSS_SYN			X	Analog ground for synthesizer
14	SHIELD	IN		X	Shield GND

Pin No.	Pin Name	Type	Supply Voltage	Connection (If not used)	Short Description
15	TEST0	IN	AVDD_DAC	GND	Test Pin
16	TEST1	IN	AVDD_DAC	GND	Test Pin
17	TEST2	IN	AVDD_DAC	GND	Test Pin
18	CVBS	OUT	AVDD_DAC	X	CVBS output
19	REF_SW	IN	AVDD_DAC	X	Reference frequency switch
20	SIF	OUT	AVDD_DAC	X	2nd SIF output
21	AVDD_DAC			X	DAC supply (+5 V)
22	AVSS_DAC			X	DAC ground
23	TEST_EN	IN	DVDD	GND	Test enable
24	RESETQ	IN	DVDD	X	Reset
25	I2C_SDA	I/O	DVDD	X	I^2C data
26	I2C_SCL	I/O	DVDD	X	I^2C clock
27	DVDD_CAP			X	Digital supply capacitor
28	DVDD			X	Digital supply (+3.3 V)
29	DVSS			X	Digital ground
30	DVSS_CAP			X	Digital capacitor ground
31	PORT0	OUT	DVDD	LV	Digital output port
32	PORT1	OUT	DVDD	LV	Digital output port
33	TUNER_AGC	OUT	DVDD	X	Tuner AGC current output
34	PORT2	OUT	DVDD	LV	Digital output port
35	PORT3	OUT	DVDD	LV	Digital output port
36	PORT4	OUT	DVDD	LV	Digital output port
37	ADR_SEL	IN	DVDD	X	Address select
38	PORT5	OUT	DVDD	LV	Digital output port
39	DVDD_ADC			X	Digital supply for ADC (+3.3 V)
40	DVSS_ADC			X	Digital ground for ADC
41	XTAL_IN	IN	AVDD_ADC	X	Crystal oscillator
42	XTAL_OUT	I/O	AVDD_ADC	X	Crystal oscillator / external reference frequency
43	VREF		AVDD_ADC	X	ADC reference voltage
44	SGND		AVDD_ADC	X	ADC reference ground

5.3. Pin Descriptions

Pin 1, **AVSS_ADC** – Analog ground for ADC

Pin 2, **AVDD_ADC** – Analog supply for ADC
This pin must be connected to 5 V.

Pin 3, **ANATSTX** – Reserved for test
This pin should be connected to analog ground.

Pin 4, **ANATSTY** – Reserved for test
This pin should be connected to analog ground.

Pin 5, **AVDD_FE8** – Analog supply for analog front-end This pin must be connected to 5 V.

Pin 6, **AVSS_FE8** – Analog ground for analog front-end

Pin 7, **AVSS_FE40** – Analog ground for IF input circuitry.
The layout of the IF input should be symmetrical with respect to AVDD_FE40.

Pin 8, **IFINX** – Balanced IF input X
This pin must be connected to SAW output. SAW has to be placed as close as possible. The layout of the IF input should be symmetrical with respect to AVDD_FE40.

Pin 9, **AVDD_FE40** – Analog supply for IF input circuitry
This pin must be connected to 5 V. The layout of the IF input should be symmetrical with respect to AVDD_FE40.

Pin 10, **IFINX** – Balanced IF input Y
This pin must be connected to SAW output. SAW has to be placed as close as possible. The layout of the IF input should be symmetrical with respect to AVDD_FE40.

Pin 11, **AVSS_FE40** – Analog ground for IF input circuitry
The layout of the IF input should be symmetrical with respect to AVDD_FE40.

Pin 12, **AVDD_SYN** – Analog supply for clock synthesizer. This pin must be connected to 5 V.

Pin 13, **AVSS_SYN** – Analog ground for clock synthesizer.

Pin 14, **SHIELD** – Analog ground for shielding analog from digital part.

Pin 15,16,17, **TEST0 1 2** – Pins for factory test

Pin 18, **CVBS** – Video output
Output level is set via I^2C-Bus. An appropriate video processor (e.g. VPC etc.) has to be connected to that pin.

Pin 19, **REF_SW**– Reference frequency switch. This input defines the default setting of the reference divider after POR. For 20.25 MHz applications it has to be connected to ground, for applications with higher frequencies than 20.25 MHz it must be connected to 3.3 V.

Pin 20, **SIF** – 2nd sound IF ouput
Output level is set via I2C-Bus. An appropriate sound processor (e.g. MSP) has to be connected to that pin.

Pin 21, **AVDD_DAC** – Analog supply for the analog output DACs
This pin must be connected to 5 V.

Pin 22, **AVSS_DAC** – Analog Ground for the analog output DACs
This pin must be connected to ground.

Pin 23, **TEST_EN** – Test Enable pin
This pin enables factory test modes. For normal operation it must be connected to ground.

Pin 24, **$\overline{\text{RESET}}$** – Reset input
For normal operation, a high level is required. A low level resets the DRX 3960A.

Pin 25, 26, **I2C_SDA, I2C_SCL**– I2C control bus data and clock

Pin 27, **DVDD_CAP** – Digital supply pin
This pin has to be connected to 3.3 V according to the application circuit.

Pin 28, **DVDD** – Digital supply pin
This pin has to be connected to 3.3 V according to the application circuit.

Pin 29, **DVSS** – Digital ground pin
This pin has to be connected to digital ground according to the application circuit.

Pin 30, **DVSS_CAP** – Digital ground pin
This pin has to be connected according to the application circuit.

Pin 31, 32, 34, 35, 36, 38, **PORT0 1 2 3 4 5** – General purpose output ports
Their states are controlled via I2C bus.

Pin 33, **TUNER_AGC** – This pin controls the delayed tuner AGC. As it is a noise-shaped-I-DAC output, it has to be connected according to the application circuit.

Pin 37, **ADR_SEL** – I^2C Bus address select
By means of this pin, one of three device addresses can be selected.

Pin 39, **DVDD_ADC** – Digital supply pin for ADC
This pin has to be connected to 3.3 V.

Pin 40, **DVSS_ADC** – Digital ground pin for ADC.
This pin has to be connected to digital ground.

Pin 41, **XTAL_IN** – Crystal input pin
If an external clock is used this pin should be left open. A crystal should be placed as close as possible to this pin. External capacitors at each crystal pin to ground are required. It should be verified by layout, that no supply current is flowing through the ground connection point.

Pin 42, **XTAL_OUT** – Crystal output pin
If an external clock is used, it has to be connected to this pin. A crystal should be placed as close as possible to this pin. External capacitors at each crystal pin to ground are required. It should be verified by layout, that no supply current is flowing through the ground connection point.

Pin 43, **VREF** – Analog reference voltage
This pin must be connected to SGND via a circuitry according to the application circuit.

Pin 43, **SGND** – Reference for analog ground
This pin must be connected separately to a single ground point.

5.4. Pin Configuration

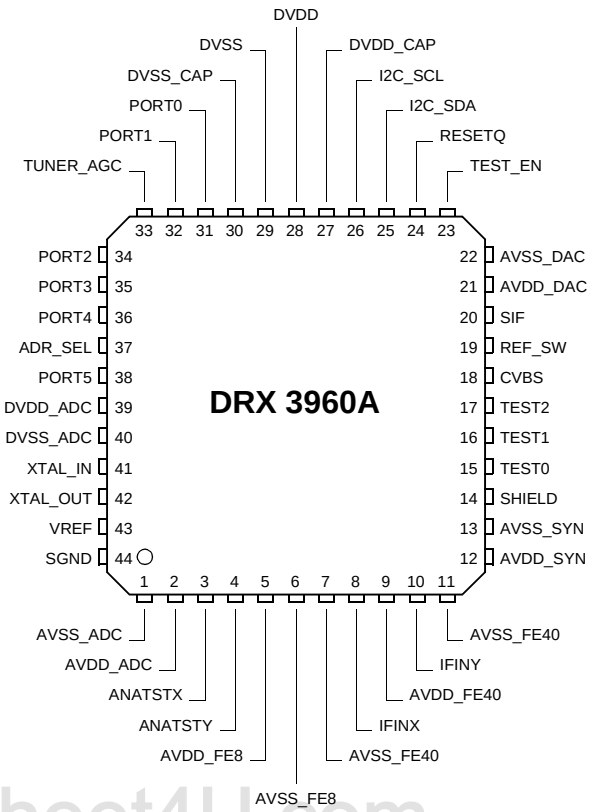


Fig. 5–2: 44-pin PMQFP package

5.5. Electrical Characteristics

5.5.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient Operating Temperature		0	70	°C
P_{TOT}	Maximum Power Dissipation		–	833	mW
T_S	Storage Temperature		–40	125	°C
V_{SUPmax}	Supply Voltage, all Supply Inputs		–0.3	6	V
V_{max}	External Voltage, all V_{ASUP} Pins, (without TUNER_AGC)		–0.3	V_{ASUP}+0.3	V
	External Voltage, all V_{DSUP} Pins		–0.3	V_{DSUP}+0.3	V
	External Voltage, I2C	I2C_SDA I2C_SCL	–0.3	6	V
$V_{SUP-tun}$	TUNER_AGC Voltage	TUNER_AGC	–	8	V

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

5.5.2. Recommended Operating Conditions

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
V_{ASUP}	Voltage, Analog Supply Pins	AVDD_ADC AVDD_FE8 AVDD_FE40 AVDD_SYN AVDD_DAC	4.75	5.0	5.25	V
V_{DSUP}	Voltage, Digital Supply Pins	DVDD DVDD_CAP	3.0	3.3	3.6	V
V_{DSUP_ADC}	Voltage, Digital Supply Pins, ADC	DVDD_ADC	3.0	3.3	3.6	V
V_{ext_I2C}	External Voltage I2C	I2C_SDA I2C_SCL	0.0	–	5.5	V
f_{XTAL}	Clock Frequency	XTAL_IN/ OUT	–	20.25	–	MHz
$f_{external}$	External Clock Frequency Range	XTAL_IN	1	20.25	30	MHz
$f_{ssbnoise}$	SSB-Phase noise of External Clock Frequency fratio = 20*Log10 (40.5 MHz/$f_{external}$)	XTAL_IN			–90 fratio	dBc fm = 1 kHz

The values given under “Characteristics” are valid for these “Recommended Operating Conditions”.

5.5.3. Recommended Crystal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Ambient Temperature	0	–	70	°C
f_P	Parallel Resonance Frequency with Load Capacitance CL = 13 pF	–	20.250000	–	MHz
$\Delta f_P/f_P$	Accuracy of Adjustment	–	–	±100	ppm
$\Delta f_P/f_P$	Frequency Temperature Drift	–	–	±30	ppm
R_R	Series Resistance	–	–	25	Ω
C_0	Shunt Capacitance	3	–	7	pF

5.5.4. Recommended Tuner Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
a_{tuner}	Minimum Gain Control Range	40			dB
S_{tuner}	AGC Control Voltage Sensitivity			50	dB/V

5.6. Characteristics

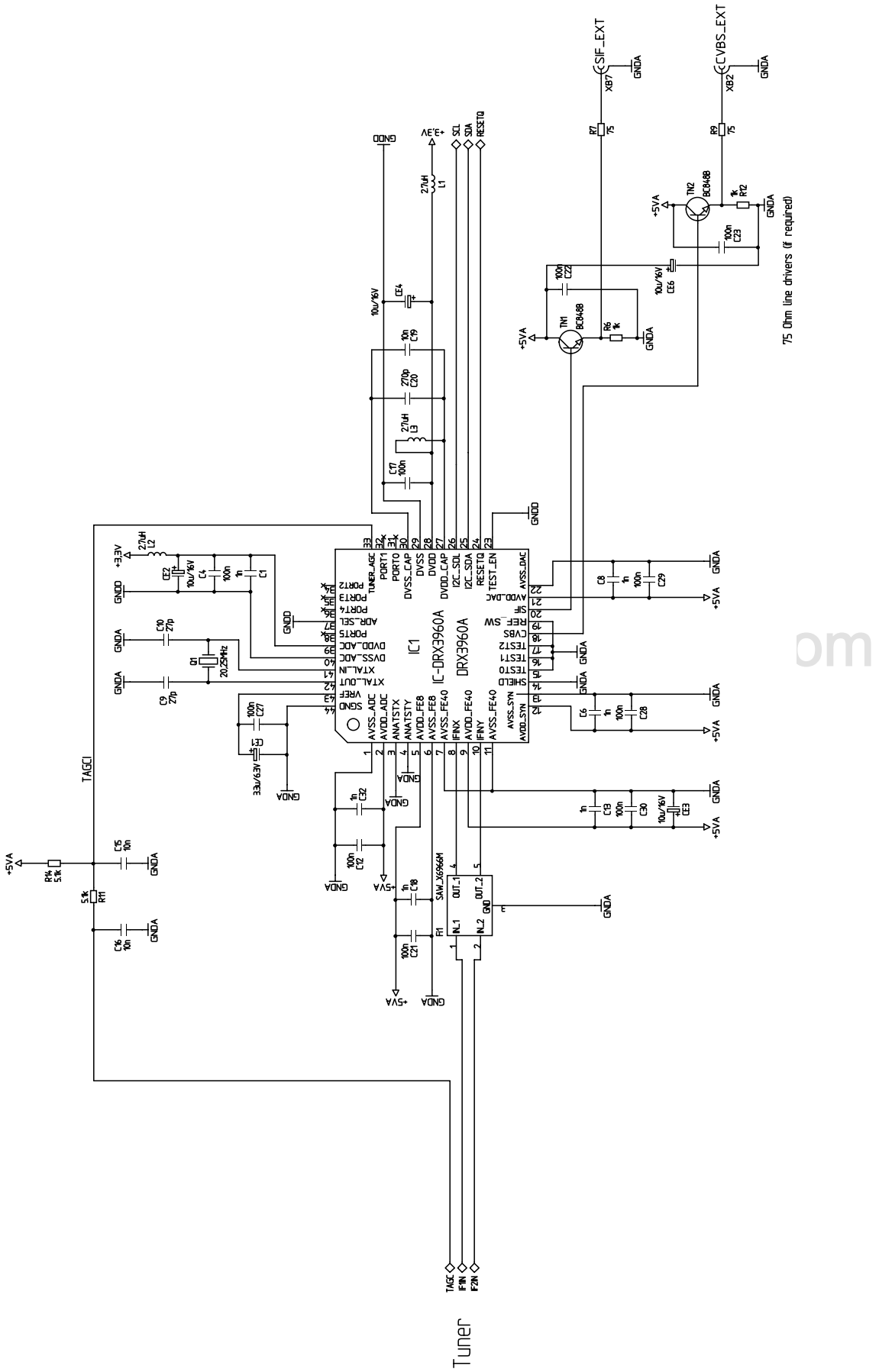
Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Supply							
I_{dig}	Current Consumption, digital			60		mA	
I_{ana}	Current Consumption, analog			110		mA	
P_{tot}	Total Power Consumption			750		mW	
Digital Input Levels							
V_{DIGIL}	Digital Input Low Voltage	TEST_EN REF_SW			0.2	V_{DVDD}	
V_{DIGIH}	Digital Input High Voltage		0.8			V_{DVDD}	
Z_{DIGI}	Input Impedance				5	pF	
I_{DLEAK}	Digital Input Leakage Current		–1		1	µA	$0\ V < V_{INPUT} < V_{DVDD}$
V_{DIGIL}	Digital Input Low Voltage	ADR_SEL			0.2	V_{DVDD}	
V_{DIGIH}	Digital Input High Voltage		0.8			V_{DVDD}	
I_{ADRSEL}	Input Current Address Select Pin		–500	–220		µA	$V_{ADR\_SEL} = V_{DVSS}$
				220	500	µA	$V_{ADR\_SEL} = V_{DVDD}$

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Digital Output Levels							
V_{PORTL}	Digital Output Low Voltage	PORT 0, 1, 2, 3, 4, 5			0.4	V	I_{PORT} = 1.6 mA
V_{PORTH}	Digital Output High Voltage		V_{DVDD} - 0.4			V	I_{PORT} = –1.6 mA
I_{PORT}	Digital Output Current		–2		2	mA	
$\overline{\text{Reset}}$							
V_{RHL}	$\overline{\text{Reset}}$ High Low transition	$\overline{\text{RESET}}$		1.1		V	
V_{RLH}	$\overline{\text{Reset}}$ Low High transition	$\overline{\text{RESET}}$		2.1		V	
I²C-Bus							
V_{I2CIL}	I²C-Bus Input Low Voltage	I2C_CL, I2C_DA			0.3	V_{DVDD}	
V_{I2CIH}	I²C-Bus Input High Voltage		0.6			V_{DVDD}	
t_{I2C1}	I²C Start Condition Setup Time		120			ns	
t_{I2C2}	I²C Stop Condition Setup Time		120			ns	
t_{I2C5}	I²C-Data Setup Time before Rising Edge of Clock		55			ns	
t_{I2C6}	I²C-Data Hold Time after Falling Edge of Clock		55			ns	
t_{I2C3}	I²C-Clock Low Pulse Time	I2C_CL	500			ns	
t_{I2C4}	I²C-Clock High Pulse Time		500			ns	
f_{I2C}	I²C-Bus Frequency				1.0	MHz	
V_{I2COL}	I²C-Data Output Low Voltage	I2C_CL, I2C_DA			0.4	V	I_{I2COL} = 3 mA
I_{I2COH}	I²C-Data Output High Leakage Current				1.0	µA	V_{I2COH} = 5 V
t_{I2COL1}	I²C-Data Output Hold Time after Falling Edge of Clock		15			ns	
t_{I2COL2}	I²C-Data Output Setup Time before Rising Edge of Clock		100			ns	f_{I2C} = 1 MHz
IF Input							
Z_{in}	Differential Input Impedance R C	IFINX, IFINY	 1.6 1	 2	 2.4 4	 kΩ pF	
f_{in}	Input Frequency	IFINX, IFINY		38.9	47	MHz	
V_{wanted}	Maximum wanted Signal Input Voltage TOP = 0 TOP = 15	IFINX, IFINY		 200 97 20 77		 mV_{pp} dBuV mV_{pp} dBuV	FS
S_{IF}	Sensitivity (S/N unweighted = 26 dB)	IFINX, IFINY		1		mV	fin = 38.9 MHz, TOP gain = 10 dB

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Low Noise Preamplifier (with Tuner Take Over Point Setting)							
TOP_{min}	Minimum Gain			0		dB	
TOP_{max}	Maximum Gain			20		dB	
TOP_{step}	Stepsize of Gain			1.33		dB	
Analog Front-end							
G_{tol}	Total Gain Tolerance				±1	dB	matched inputs
Carrier Recovery							
D_{AFC}	Frequency Tolerance = AFC Accuracy				50	kHz	
f_{lock}	Lock in range = frequency true demodulation range		0.8 1.0			MHz MHz	direction: adjacent channel direction: own channel
VIF AGC							
f_{VAGC}	**Control Bandwidth**						
BW_n	negative modulation			200		Hz	
BW_p	positive modulation			1		Hz	
BW_{pinc}	positive modulation increasing signal (white picture)			200		Hz	
BW_{bp}	positive modulation back porch control			200		Hz	
Tuner AGC, Current Output							
I_{TAGC}	Maximum Output Sink Current	TUNER_ AGC	680	800	920	µA	90 % FS
V_{sup_tun}	Maximum Output Voltage				8	V	
Video Output							
V_{sync}	Sync Level (minimum DAC value)	CVBS	1.2	1.4	1.6	V	
V_{vidmax}	Maximum Level (maximum DAC value)		3.8 2.9 2.4 2.0	4.0 3.3 2.7 2.3	4.2 3.7 3.0 2.6	V	@ VID_AMP=0 @ VID_AMP=1 @ VID_AMP=2 @ VID_AMP=3
V_{vidpp}	Full Scale Voltage		2.4 1.7 1.2 0.8	2.6 1.9 1.3 0.9	2.8 2.1 1.4 1.0	V_{pp}	@ VID_AMP=0 @ VID_AMP=1 @ VID_AMP=2 @ VID_AMP=3
$f_{-1dBvid}$	Cutoff Frequency		6			MHz	C_{Load} < 30 pF, R_{Load_AC} > 1 kΩ
R_{outvid}	Output Resistance				50	Ω	f < 6 MHz
SNR_{vidw}	Weighted Video S/N		56	58		dB	Weighted video S/N (CCIR567, 10 kHz...5 MHz)
SNR_{vidu}	Unweighted Video S/N		49	51		dB	Unweighted video S/N (10 kHz...5 MHz)
$\alpha_{1.07}$	Intermodulation ratio		65			dB	blue picture, P_{SC1}=-13dB, no sound shelf $\alpha_{1.07=} P_{CC}$-$P_{1.07}$ +3dB

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Sound IF Output							
V_{sifpp}	Full Scale Voltage	SIF		1.5 1.1 0.8 0.6		V_{pp}	@ SIF_REF=0 @ SIF_REF=1 @ SIF_REF=2 @ SIF_REF=3
$f_{-1dBsif}$	Cutoff Frequency f_{-1dB}		6			MHz	C_{Load} < 30 pF, R_{Load_AC} > 1 kΩ
R_{outsif}	Output Resistance				50	Ω	f < 6 MHz
SNR_b	Weighted Sound S/N SC1/SC2			62/58		dB	black picture, CCIR 468
SNR_w	Weighted Sound S/N SC1/SC2			62/58		dB	white picture, CCIR 468
SNR_{fubk}	Weighted Sound S/N SC1/SC2			55/50		dB	FuBK picture, CCIR 468

6. Application Circuit



7. Data Sheet History

1. Advance Information: “DRX 3960A Digital Receiver Front-end”, Aug. 10, 2000, 6251-510-1AI. First release of the advance information.

2. Advance Information: “DRX 3960A Digital Receiver Front-end”, Feb. 8, 2001, 6251-510-2AI. Second release of the advance information.

Major changes:

– reduction of front-end gain

– positive detection bit removed

– output level setting changed

– lock detection bit added

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