M5M8050H-XXXP/M5M8040HP

SINGLE-CHIP 8-BIT MICROCOMPUTER

DESCRIPTION

The M5M8050H-XXXP/M5M8040HP is an 8-bit parallel microcomputer fabricated on a single chip using N-channel silicon gate ED-MOS technology.

M5M8050H-XXXP	Internal ROM Type (4K Bytes)
M5M8040HP	External ROM Type

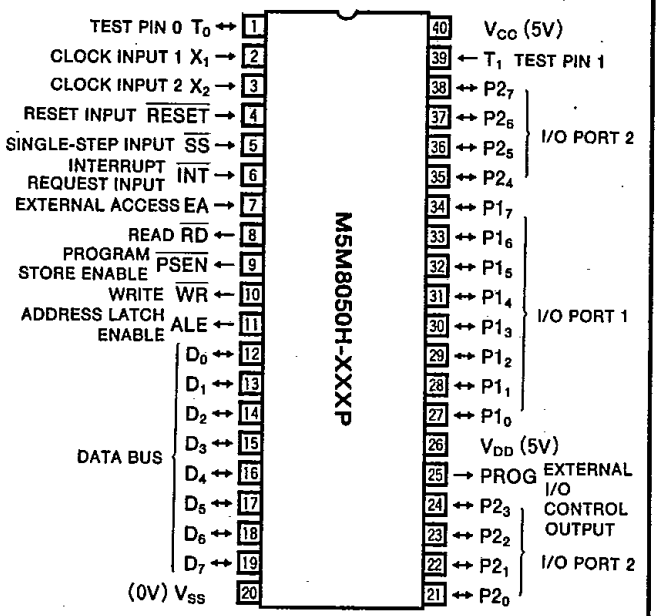
FEATURES

- Single 5V power supply
- Instruction cycle ..... 1.36μs (min)
- Basic machine instructions . . 96 (1-byte instructions: 68)
- 4K-bytes memory addressing possible
  (direct addressing possible in 2K bytes memory)
- Memory capacity: ROM ..... 4K bytes
  RAM ..... 256 bytes
- Built-in timer/event counter ..... 8 bits
- I/O ports ..... 27 lines
- Easily expandable Memory and I/O
- Subroutine nesting ..... 8 levels
- External and timer/event counter interrupt, 1 level each
- Low power standby mode

APPLICATION

Control processor or CPU for a wide variety of applications

PIN CONFIGURATION (TOP VIEW)

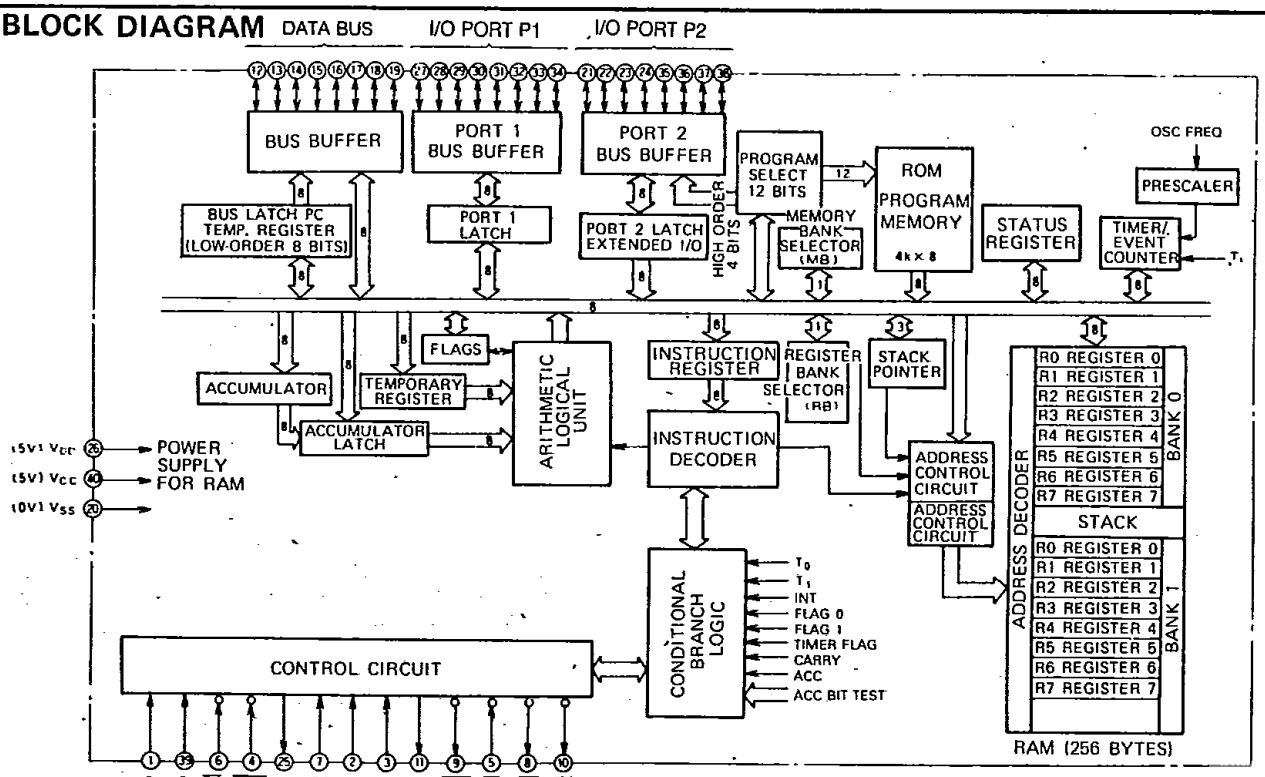


Outline 40P4

FUNCTION

The M5M8050H-XXXP/M5M8040HP is an 8-bit CPU, with memory (ROM, RAM) and timer/event counter interrupt all contained a single chip.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

PIN DESCRIPTION

Pin	Name	Input or output	Function
V_{SS}	Ground		Normally connected to ground (0V).
V_{CC}	Main power supply		Connected to 5V power supply.
V_{DD}	Power supply		①Connected to 5V power supply. ②Used for memory hold when V_{CC} is cut.
T_0	Test pin 0	Input	①Control signal from an external source for conditional jumping in a program. Jumping is dependent on external conditions (JT0/JNT0).
		Output	②Used for outputting the internal clock signal (ENT0 CLK).
X_1, X_2	Crystal inputs	Input	External crystal oscillator or RC circuit input for generating internal clock signals. An external clock signal can be input through X_1 or X_2.
$\overline{RESET}$	Reset	Input	Control used to initialize the CPU.
$\overline{SS}$	Single step	Input	Control signal used in conjunction with ALE to stop the CPU through each instruction, in the single-step mode.
$\overline{INT}$	Interrupt	Input	①Control signal from an external source for conditional jumping in a program. Jumping is dependent on external conditions (JNI). ②Used for external interrupt to CPU.
EA	External access	Input	①Normally maintained at 0V. ②When the level is raised to 5V, external memory will be accessed. The M5M8040HP is raised to 5V.
$\overline{RD}$	Read control	Output	Read control signal used when the CPU requests data from external data memory or external device to be transferred to the data bus. (MOVX A, @R_r, and INS A, BUS)
$\overline{PSEN}$	Program store enable	Output	Strobe signal to fetch external program memory.
$\overline{WR}$	Write control	Output	Write control signal used when the CPU sends data through the data bus to external data memory or external device. (MOVX @R_r, A and OUTL BUS, A)
ALE	Address latch enable	Output	A signal used for latching the address on the data bus. An ALE signal occurs once during each cycle.
D_0~D_7	Data bus	Input/output	①Provides true bidirectional bus transfer of instructions and data between the CPU and external memory. Synchronizing is done with signals $\overline{RD}$/$\overline{WR}$. The output data is latched.
			②When using external program memory, the output of the low-order 8 bits of the program counter are synchronized with ALE. After that, the transfer of the instruction code or data from the external program memory is synchronized with $\overline{PSEN}$.
			③The output of addresses for data using the external data memory is synchronized with ALE. After that, the transfer of data with the external data memory is synchronized with $\overline{RD}$/$\overline{WR}$. (MOVX A, @R_r, and MOVX @R_r, A)
$P2_0$~$P2_7$	Port 2	Input/output	①Quasi-bidirectional port. When used as an input port, FF_{16} must first be output to this port. After reset, when not used as an output port, nothing needs to be output.
		Output	②$P2_0$~$P2_3$ output high-order 4 bits of the program counter when using external program memory.
		Input/output	③$P2_0$~$P2_3$ serve as a 4-bit I/O expander bus for the M5L8243P.
PROG	Program	Output	Strobe signal for M5L8243P I/O expander.
$P1_0$~$P1_7$	Port 1	Input/output	Quasi-bidirectional port. When used as an input port, FF_{16} must first be output to this port. After reset, when not used as an output port, nothing needs to be output.
T_1	Test pin 1	Input	①Control signal from an external source for conditional jumping in a program. Jumping is dependent on external conditions (JT1/JNT1). ②When enabled, event signals are transferred to the timer/event counter (STRT CNT).

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.5～7	V
V_{DD}	Supply voltage		−0.5～7	V
V_I	Input voltage		−0.5～7	V
V_O	Output voltage		−0.5～7	V
Pd	Power dissipation	Ta＝25℃	1.5	W
Topr	Operating free-air temperature range		0～70	℃
Tstg	Storage temperature range		−65～150	℃

RECOMMENDED OPERATING CONDITIONS (Ta＝0～70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH1}	High-level input voltage, except X_1, X_2 and $\overline{RESET}$	2		V_{CC}	V
V_{IH2}	High-level input voltage, X_1, X_2 and $\overline{RESET}$	3.8		V_{CC}	V
V_{IL1}	Low-level input voltage, except X_1, X_2 and $\overline{RESET}$	−0.5		0.8	V
V_{IL2}	Low-level input voltage, X_1, X_2 and $\overline{RESET}$	−0.5		0.6	V

ELECTRICAL CHARACTERISTICS (Ta＝0～70℃, $V_{CC}=V_{DD}=5V\pm10\%$, $V_{SS}=0V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OL}	Low-level output voltage (BUS)	$I_{OL}=2mA$			0.45	V
V_{OL1}	Low-level output voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	$I_{OL}=1.8mA$			0.45	V
V_{OL2}	Low-level output voltage (PROG)	$I_{OL}=1mA$			0.45	V
V_{OL3}	Low-level output voltage (for other outputs)	$I_{OL}=1.6mA$			0.45	V
V_{OH}	High-level output voltage (BUS)	$I_{OH}=-400\mu A$	2.4			V
V_{OH1}	High-level output voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	$I_{OH}=-100\mu A$	2.4			V
V_{OH2}	High-level output voltage (for other outputs)	$I_{OH}=-40\mu A$	2.4			V
I_I	Input leak current (T_1, $\overline{INT}$)	$V_{SS}\leqq V_{IN}\leqq V_{CC}$	−10		10	μA
I_{OZ}	Output leak current (BUS, T_0) high-impedance state	$V_{SS}+0.45\leqq V_{IN}\leqq V_{CC}$	−10		10	μA
I_{I1}	Input leak current (PORT)	$V_{SS}+0.45\leqq V_{IN}\leqq V_{CC}$		−0.2	−0.5	mA
I_{I2}	Input leak current ($\overline{RESET}$, $\overline{SS}$)	$V_{SS}+0.45\leqq V_{IN}\leqq V_{CC}$		−0.05		mA
I_{DD}	Supply current from V_{DD}			10	20	mA
$I_{DD}+I_{CC}$	Supply current from V_{DD} and V_{CC}			70	140	mA

TIMING REQUIREMENTS (T_a = 0 ~ 70℃, V_{CC} = V_{DD} = 5V ± 10%, V_{SS} = 0 V, unless otherwise noted)

Symbol	Parameter	Relationship to cycle time (t_C)	Alternative symbol	Limits			Unit
				Min	Typ	Max	
t	Clock cycle	$1/f_{XTAL}$	t	90.9		1000	ns
t_C	Cycle time	15t	t_{CY}	1.36		15	μs
$t_{h(PSEN-D)}$	Data hold time after $\overline{PSEN}$	1.5t—30	t_{DR}	0		110	ns
$t_{h(R-D)}$	Data hold time after $\overline{RD}$	1.5t—30	t_{DR}	0		110	ns
$t_{su(PSEN-D)}$	Data setup time after $\overline{PSEN}$	4.5t—170	t_{RD2}			240	ns
$t_{su(R-D)}$	Data setup time after $\overline{RD}$	6t—170	t_{RD1}			37.5	ns
$t_{su1(A-D)}$	Data setup time after address (external data memory read cycle)	10.5t—220	t_{AD1}			730	ns
$t_{su2(A-D)}$	Data setup time after address (external program memory read cycle)	7.5t—220	t_{AD2}			460	ns
$t_{su(PROG-D)}$	Data setup time after PROG	8.5t—120	t_{PR}			650	ns
$t_{h(PROG-D)}$	Data hold time after PROG	1.5t	t_{PF}	0		140	ns

Note 1 The input voltages are V_{IL} = 0.45V and V_{IH} = 2.4V.

2 f_{XTAL} is the oscillator frequency entered at the crystal input terminals (X_1, X_2).

SWITCHING CHARACTERISTICS (T_a 0 ~ 70℃, V_{CC} = V_{DD} = 5V ± 10%, V_{SS} = 0 V, unless otherwise noted)

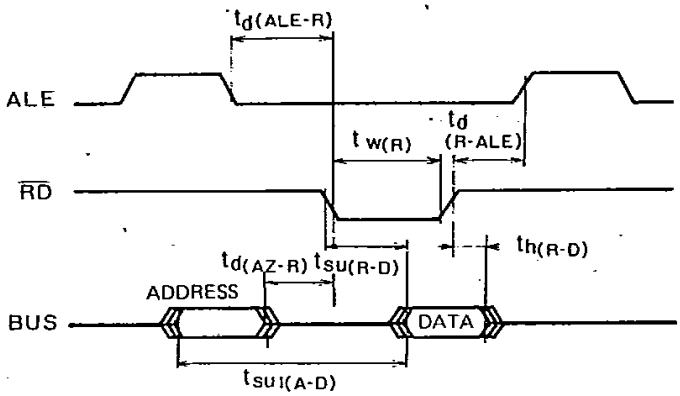
Symbol	Parameter	Relationship to cycle time (t_C)	Alternative symbol	Limits			Unit
				Min	Typ	Max	
$t_{w(ALE)}$	ALE pulse width	3.5t—170	t_{LL}	150			ns
$t_{d(A-ALE)}$	Delay time, address to ALE signal	2t—110	t_{AL}	70			ns
$t_{v(ALE-A)}$	Address valid time after ALE	t—40	t_{LA}	50			ns
$t_{w(PSEN)}$	$\overline{PSEN}$ pulse width	6t—200	t_{CC2}	350			ns
$t_{w(R)}$	$\overline{RD}$ pulse width	7.5t—200	t_{CC1}	480			ns
$t_{w(W)}$	$\overline{WR}$ pulse width	7.5t—200	t_{CC1}	480			ns
$t_{d(Q-W)}$	Delay time, data to $\overline{WR}$ signal	6.5t—200	t_{DW}	390			ns
$t_{v(W-Q)}$	Data valid time after $\overline{WR}$	t—50	t_{WD}	40			ns
$t_{d(A-W)}$	Delay time, address to $\overline{WR}$ signal	5t—150	t_{AW}	300			ns
$t_{d(AZ-R)}$	Delay time, address disable to $\overline{RD}$ signal	2t—40	t_{AFC1}	140			ns
$t_{d(AZ-W)}$	Delay time, address disable to $\overline{WR}$ signal	2t—40	t_{AFC1}	140			ns
$t_{d(AZ-PSEN)}$	Delay time, address disable to $\overline{PSEN}$ signal	0.5t—40	t_{AFC2}	10			ns
$t_{d(ALE-R)}$	Delay time, ALE to $\overline{RD}$ signal	3t—75	t_{LAFC1}	200			ns
$t_{d(ALE-W)}$	Delay time, ALE to $\overline{WR}$ signal	3t—75	t_{LAFC1}	200			ns
$t_{d(ALE-PSEN)}$	Delay time, ALE to $\overline{PSEN}$ signal	1.5t—75	t_{LAFC2}	60			ns
$t_{d(R-ALE)}$	Delay time, $\overline{RD}$ to ALE signal	t—65	t_{CA1}	25			ns
$t_{d(W-ALE)}$	Delay time, $\overline{WR}$ to ALE signal	t—65	t_{CA1}	25			ns
$t_{d(PROG-ALE)}$	Delay time, PROG to ALE signal	t—65	t_{CA1}	25			ns
$t_{d(PSEN-ALE)}$	Delay time, $\overline{PSEN}$ to ALE signal	4t—70	t_{CA2}	230			ns
$t_{d(PC-PROG)}$	Delay time, Port control to PROG signal	1.5t—80	t_{CP}	50			ns
$t_{v(PROG-PC)}$	Port control valid time after PROG	4t—260	t_{PC}	100			ns
$t_{d(Q-PROG)}$	Delay time, Data to PROG signal	6t—290	t_{DP}	250			ns
$t_{v(PROG-Q)}$	Data valid time after PROG	1.5t—90	t_{PD}	40			ns
$t_{w(PROGL)}$	PROG low pulse width	10.5t—250	t_{PP}	700			ns
$t_{d(Q-ALE)}$	Delay time, Data to ALE signal	4t—200	t_{PL}	160			ns
$t_{v(ALE-Q)}$	Data valid time after ALE	0.5t—30	t_{LP}	15			ns
$t_{d(ALE-Q)}$	Delay time, ALE to data	4.5t+100	t_{PV}			510	ns
$t_{w(T_0)}$	T_0 pulse period	3t	t_{OPRR}	270			ns

Note 3 Conditions of measurement control output C_L = 80pF data bus output, port output C_L = 150pF

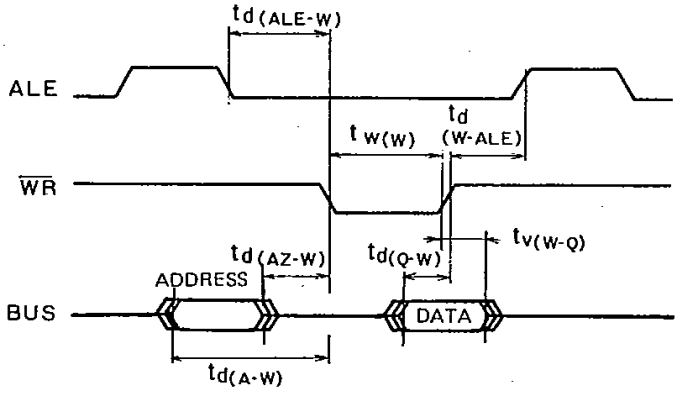
4 Reference levels for input/output voltages are low-level=0.8V and high-level=2V.

TIMING DIAGRAM

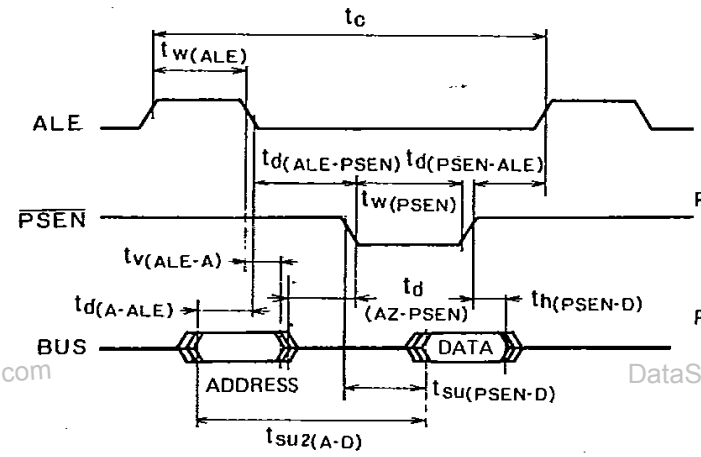
Read from External Data Memory



Write to External Data Memory



Instruction Fetch from External Program Memory



Port 2