

# High Performance 1024x8 Registered PROM

# 53/63RS881 53/63RS881A

63RS881

## Features/Benefits

- Edge triggered "D" registers
- Synchronous and asynchronous enables
- Versatile 1:16 initialization words
- 8-Bit-wide in 24-pin SKINNYDIP® package for high board density
- Simplifies system timing
- Faster cycle times
- 16 mA I<sub>OL</sub> output drive capability
- Reliable titanium-tungsten fuses (TIW), with programming yields typically greater than 98%

## Applications

- Microprogram control store
- State sequencers
- Next address generation
- Mapping PROM
- Programmable Logic Element (PLE™)  
10 Inputs, 8 Registered Outputs, 1024 product terms

## Description

The 53/63RS881 and 53/63RS881A are 1Kx8 PROMs with on-chip "D" type registers, versatile output enable control through synchronous and asynchronous enable inputs, and flexible start up sequencing through programmable initialization.

Data is transferred into the output registers on the rising edge of the clock. Provided that the asynchronous ( $\bar{E}$ ) and synchronous ( $\bar{ES}$ ) enables are low, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

Memory expansion and data control is made flexible with synchronous and asynchronous enable inputs. Outputs may be set to the high impedance state at any time by setting  $\bar{E}$  to a high or if  $\bar{ES}$  is high when the rising clock edge occurs. When  $V_{CC}$  power is first applied the synchronous enable flip-flop will be in the set condition causing the outputs to be in the high impedance state.

The flexible initialization feature allows start up and time out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE ( $\bar{IS}$ ) pin low, one of the 16 column words (A3-A0) will be set in the output registers independent of the row addresses (A9-A4). The unprogrammed state of  $\bar{IS}$  words are low, presenting a CLEAR with  $\bar{IS}$  pin low. With all  $\bar{IS}$  column words (A3-A0) programmed to the same pattern, the  $\bar{IS}$  function will be independent of both row and column addressing and may be used as a single pin control. With all  $\bar{IS}$  words programmed high a PRESET function is performed.

## Selection Guide

MEMORY		PACKAGE		PERFORMANCE	PART NUMBER	
SIZE	ORGANIZATION	PINS	TYPE		0°C to +75°C	-55°C to +125°C
8 K	1024x8	24 (28)	NS,JS, J,W, (NL),(L)	Enhanced	63RS881A	53RS881A
				Standard	63RS881	53RS881

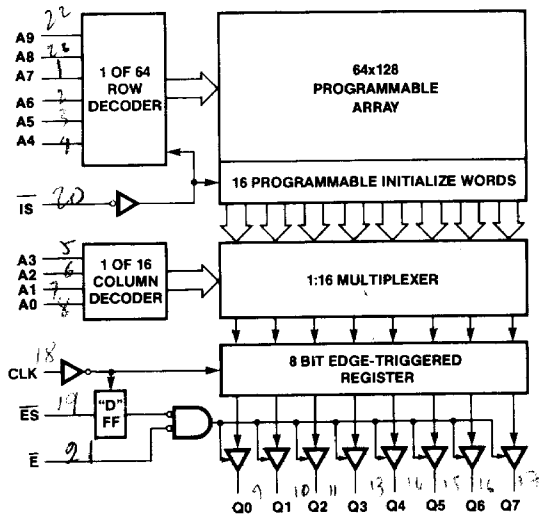
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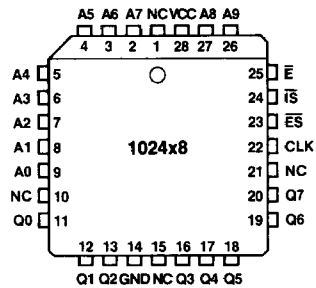
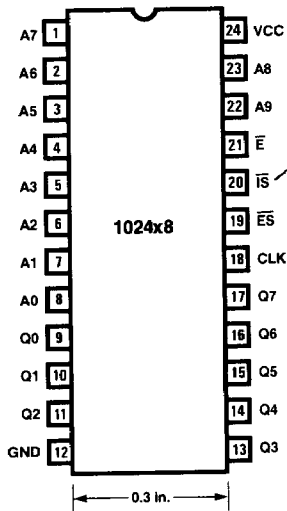
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374

Block Diagram



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Pin Configurations



Plastic Chip Carrier

### Absolute Maximum Ratings

	Operating	Programming
Supply voltage $V_{CC}$ .....	-0.5 V to 7 V	12 V
Input voltage .....	-1.5 V to 7 V	7 V
Input current .....	-30 mA to +5 mA	
Off-state output voltage .....	-0.5 V to 5.5 V	12 V
Storage temperature .....	-65°C to +150°C	

### Operating Conditions

SYMBOL	PARAMETER	TYP†	MILITARY		COMMERCIAL		UNIT				
			53RS881A	53RS881	63RS881A	63RS881					
			MIN	MAX	MIN	MAX					
$t_w$	Width of clock (high or low)	10	20	20	20	20	ns				
$t_s(A)$	Setup time from address to clock	25	40	45	30	35	ns				
$t_s(\overline{ES})$	Setup time from $\overline{ES}$ to clock	8	15	15	15	15	ns				
$t_s(\overline{IS})$	Setup time from $\overline{IS}$ to clock	20	30	35	25	30	ns				
$t_h(A)$	Hold time address to clock	-5	0	0	0	0	ns				
$t_h(\overline{ES})$	Hold time ( $\overline{ES}$ )	-3	5	5	5	5	ns				
$t_h(\overline{IS})$	Hold time ( $\overline{IS}$ )	-5	0	0	0	0	ns				
$V_{CC}$	Supply voltage	5	4.5	5.5	4.5	5.25	4.75	5.25	V		
$T_A$	Operating free-air temperature	25	-55	125	-55	125	0	75	0	75	°C

### Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IL}$	Low-level input voltage					0.8	V
$V_{IH}$	High-level input voltage			2.0			V
$V_{IC}$	Input clamp voltage	$V_{CC} = \text{MIN}$	$I_I = -18 \text{ mA}$			-1.2	V
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4 \text{ V}$			-0.25	mA
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}$	$V_I = V_{CC} \text{ MAX}$			40	$\mu\text{A}$
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$	$I_{OL} = 16 \text{ mA}$			0.5	V
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}$	Com $I_{OH} = -3.2 \text{ mA}$ Mil $I_{OH} = -2 \text{ mA}$	2.4			V
$I_{OZL}$	Off-state output current	$V_{CC} = \text{MAX}$	$V_O = 0.4 \text{ V}$			-40	$\mu\text{A}$
$I_{OZH}$			$V_O = 2.4 \text{ V}$			40	
$I_{OS}$	Output short-circuit current*	$V_{CC} = 5 \text{ V}$	$V_O = 0 \text{ V}$	-20		-90	mA
$I_{CC}$	Supply current	$V_{CC} = \text{MAX}$ . All inputs TTL. All outputs open.		130		180	mA

\* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

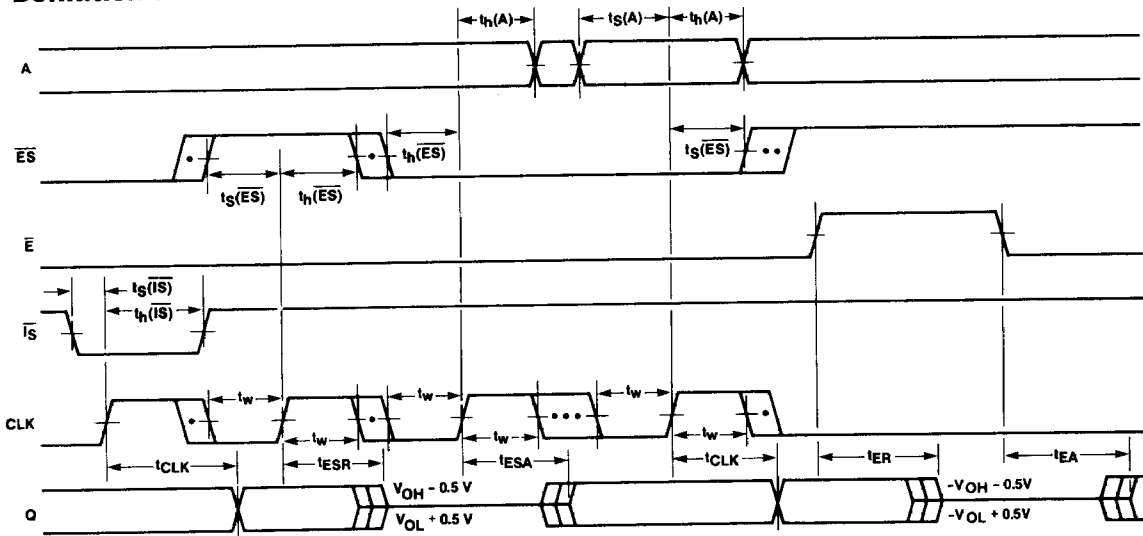
† Typical at 5.0 V  $V_{CC}$  and 25°C  $T_A$ .

**Switching Characteristics** Over Operating Conditions and using Standard Test Load

SYMBOL	PARAMETER	TYP	MILITARY				COMMERCIAL				UNIT
			53RS881A		53RS881		63RS881A		63RS881		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{CLK}$	Clock to output Delay	10	20	25	15	20	ns				
$t_{ESA}$	Clock to output access time ( $\overline{ES}$ )	18	30	35	25	30	ns				
$t_{ESR}$	Clock to output recovery time ( $\overline{ES}$ )	17	30	35	25	30	ns				
$t_{EA}$	Enable to output access time ( $\overline{E}$ )	18	30	35	25	30	ns				
$t_{ER}$	Disable to output recovery time ( $\overline{E}$ )	17	30	35	25	30	ns				

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**Definition of Waveforms**



- NOTES:
1. Input pulse amplitude 0 V to 3.0 V.
  2. Input rise and fall times 2-5 ns from 0.8 V to 2.0 V.
  3. Input access measured at the 1.5 V level.
  4.  $t_{AA}$  is tested with switch  $S_1$  closed.  $C_L = 30$  pF and measured at 1.5 V output level.
  5.  $t_{EA}$  and  $t_{ESA}$  are measured at the 1.5 V output level with  $C_L = 30$  pF.  $S_1$  is open for high impedance to "1" test and closed for high impedance to "0" test.
- $t_{ER}$  and  $t_{EA}$  are measured.  $C_L = 5$  pF.  $S_1$  is open for "1" to high impedance test, measured at  $V_{OH} - 0.5V$  output level;  $S_1$  is closed for "0" to high impedance test measured at  $V_{OL} + 0.5V$  output level.