Quad D Register With Standard And Three-State Outputs
29LS18

PRELIMINARY DATA

Features/Benefits
- **Low-power Schottky version of the popular 2918**
- **Four standard totem-pole outputs**
- **Four three-state outputs**
- **Four D-type flip-flops**
- **100% product assurance screening to MIL-STD-883 requirements**

PART NUMBER	PACKAGE	TEMPERATURE RANGE
29LS18NC ✓	N16	0°C to +70°C
29LS18JC ✓	J16	0°C to +70°C
29LS18JM ✓	J16	−55°C to +125°C
29LS18FM ✓	F16	+55°C to +125°C

Description
The 29LS18 consists of four D-type flip-flops with a buffered common clock. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

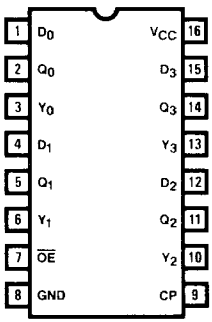
The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" (OE) input is LOW. When the OE input is HIGH, the Y outputs are in the high impedance state.

The 29LS18 is a 4-bit, high-speed register intended for use in real-time signal processing systems. The standard outputs are used in a recursive algorithm, and the three-state outputs provide access to a data bus to dump the results after a number of iterations.

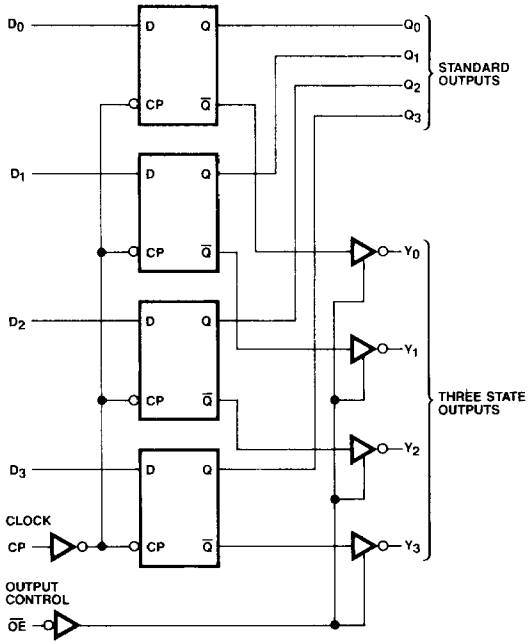
The device can also be used as an address register or status register in computers or computer peripherals.

Likewise, the 29LS18 is also useful in certain display applications where the standard outputs can be decoded to drive LED's (or equivalent) and the three-state outputs are bus organized for occasional interrogation of the data as displayed.

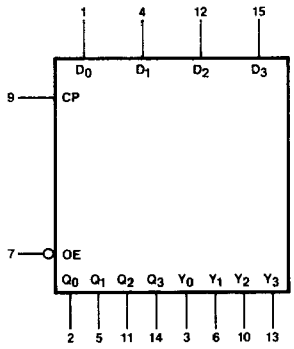
Pin Configuration



Logic Diagram



Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

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Absolute Maximum Ratings

Storage temperature ..... −65°C to +150°C
Temperature (ambient) under bias ..... −55°C to +125°C
Supply voltage to ground potential continuous ..... −0.5 V to +7.0 V
DC voltage applied to outputs for high output state ..... −0.5 V to + V_{CC} max.
DC input voltage ..... −0.5 V to +7.0 V
DC output current, into outputs 30mA
DC input current ..... −30mA to +5.0mA

Electrical Characteristics

Over Recommended Operating Range

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MILITARY T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%, MIN = 4.50V, MAX = 5.50V			COMMERCIAL T_A = 0°C to +70%, V_{CC} = 5.0V ± 5%, MIN = 4.75V, MAX = 5.25V			UNIT
				MIN	TYP[2]	MAX	MIN	TYP[2]	MAX	
V_{OH}	Output HIGH voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	Q, I_{OH} = −660μA	2.5	3.4		2.7	3.4		V
			Y, I_{OH} = −1.0mA	2.4	3.4					
			Y, I_{OH} = 2.6mA				2.4	3.4		
V_{OL}	Output LOW voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4			0.4	V
			I_{OL} = 8.0mA			0.45			0.45	
			I_{OL} = 12mA			0.5			0.5	
V_{IH}	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs		2.0			2.0			V
V_{IL}	Input LOW level	Guaranteed input logical LOW voltage for all inputs				0.7			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5			−1.5	V
I_{IL}	Input LOW current	V_{CC} = MAX, V_{IN} = 0.4V				−0.36			−0.36	mA
I_{IH}	Input HIGH current	V_{CC} = MAX, V_{IN} = 2.7V				20			20	μA
I_I	Input HIGH current	V_{CC} = MAX, V_{IN} = 7.0V				0.1			0.1	mA
I_{OZ}	Off-state (high impedance) output current	V_{CC} = MAX	V_O = 0.4V			−20			−20	μA
			V_O = 2.4V			20			20	
I_{SC}	Output short circuit current[3]	V_{CC} = MAX		−15		−85	−15		−85	mA
I_{CC}	Power supply current[4]	V_{CC} = MAX			17	28		17	28	mA

NOTES: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

4. I_{CC} is measured with all inputs at 4.5V and all outputs open.

Switching Characteristics

T_A = +25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Clock to Q_i		C_L = 15pF R_L = 2.0kΩ		18	27	ns
t_{PHL}					18	27	
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)				18	27	ns
t_{PHL}					18	27	
t_{pw}	Clock Pulse Width	LOW		18			ns
		HIGH		15			
t_s	Data			15			ns
t_h	Data			5.0			ns
t_{ZH}	$\overline{OE}$ to Y_i				7.0	11	ns
t_{ZL}					8	12	
t_{HZ}	$\overline{OE}$ to Y_i		C_L = 5.0pF R_L = 2.0kΩ		14	21	ns
t_{LZ}					12	18	
f_{max}	Maximum Clock Frequency[1]			35	50		MHz

Switching Characteristics

Over Operating Range[2]

SYMBOL	PARAMETER		TEST CONDITIONS	COMMERCIAL T_A = 0°C to +70°C V_{CC} = 5.0V ±5% MIN	COMMERCIAL MAX	MILITARY T_A = −55°C to +125°C V_{CC} = 5.0V ± 10% MIN	MILITARY MAX	UNIT
t_{PLH}	Clock to Q_i		C_L = 50pF R_L = 2.0kΩ		38		45	ns
t_{PHL}					38		45	
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)				35		40	ns
t_{PHL}					35		40	
t_{pw}	Clock Pulse Width	LOW		20		20		ns
		HIGH		20		20		
t_s	Data			15		15		ns
t_h	Data			5.0		5.0		ns
t_{ZH}	$\overline{OE}$ to Y_i				15		17	ns
t_{ZL}					16		17	
t_{HZ}	$\overline{OE}$ to Y_i		C_L = 5.0pF R_L = 2.0kΩ		27		30	ns
t_{LZ}					24		30	
f_{max}	Maximum Clock Frequency[1]			30				MHz

NOTES: 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.
2. AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Functional Table

INPUTS			OUTPUTS		NOTES
$\overline{OE}$	CLOCK CP	D	Q	Y	
H	L	X	NC	Z	—
H	H	X	NC	Z	—
H	↑	L	L	Z	—
H	↑	H	H	Z	—
L	↑	L	L	L	—
L	↑	H	H	H	—
L	—	—	L	L	1
L	—	—	H	H	1

L = LOW
H = HIGH
X = Don't care
NC = No change
↑ = LOW to HIGH transition
Z = High impedance

Note: 1. When $\overline{OE}$ is LOW, the Y output will be in the same logic state as the Q output.

Definition of Functional Terms

Data inputs, D_i
The four data inputs to the register.

Data outputs, Q_i
The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.

Three-state data outputs, Y_i
The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the Y_i outputs to the high-impedance state.

Clock, CP
The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.

Output Control, $\overline{OE}$
When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.