



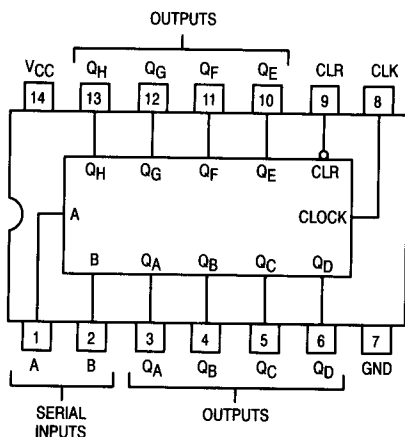
8-Bit Parallel-Out Shift Register

ELECTRICALLY TESTED PER:
MIL-M-38510/30605

The 'LS164 is a high-speed 8-Bit Serial-in Parallel-Out Shift Register. Serial data is entered through a 2-input AND gate synchronous with the LOW to HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register setting all outputs LOW independent of the clock. It utilizes the Schottky diode clamped process to achieve high speeds and is fully compatible with Motorola TTL products.

- Typical Shift Frequency of 35 MHz
- Asynchronous Master Reset
- Gated Serial Data Input
- Fully Synchronous Data Transfers
- Input Clamp Diodes Limit High-Speed Termination Effect

CONNECTION DIAGRAM



Pin Names		Loading (Note a)	
		HIGH	LOW
A, B	Data Inputs	0.5 U.L.	0.25 U.L.
CLK	Clock (active HIGH going Edge Input)	0.5 U.L.	0.25 U.L.
\overline{MR}	Master Reset (Active Low) Input	0.5 U.L.	0.25 U.L.
QA-QH	Outputs	10 U.L.	5(2.5) U.L.

Military 54LS164



AVAILABLE AS:

- 1) JAN: JM38510/30605BXA
- 2) SMD: N/A
- 3) 883: 54LS164/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 632-08	FLATS 717-04	LCC 756A-02	BURN-IN (COND. A)
A IN	1	1	2	VCC
B IN	2	2	3	VCC
QA	3	3	4	OPEN
QB	4	4	6	OPEN
QC	5	5	8	OPEN
QD	6	6	9	OPEN
GND	7	7	10	GND
CLK	8	8	12	VCC
CLR	9	9	13	GND
QE	10	10	14	OPEN
QF	11	11	16	OPEN
QG	12	12	18	OPEN
QH	13	13	19	OPEN
VCC	14	14	20	VCC

BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX

MODE SELECT TRUTH TABLE

Operating Mode	Inputs			Outputs		
	\overline{MR}	A	B	QA	QB	QH
Reset (Clear)	L	X	X	L	L	L
Shift	H	l	l	L	QA	QG
	H	l	h	L	QA	QG
	H	h	l	L	QA	QG
	H	h	h	H	QA	QG

H (h) = HIGH Voltage Levels

L (l) = LOW Voltage Levels

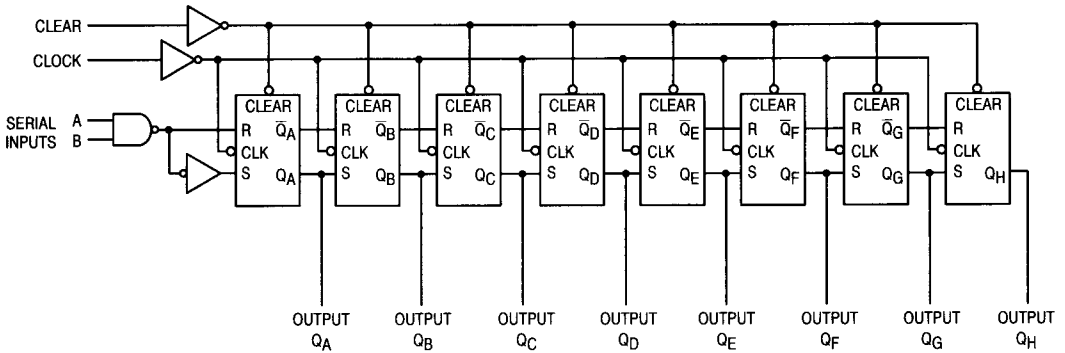
X = Don't Care

qn = Lower case letters indicate the state of the reference input or output one set-up time prior to the Low to High clock transition.

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LOGIC DIAGRAM

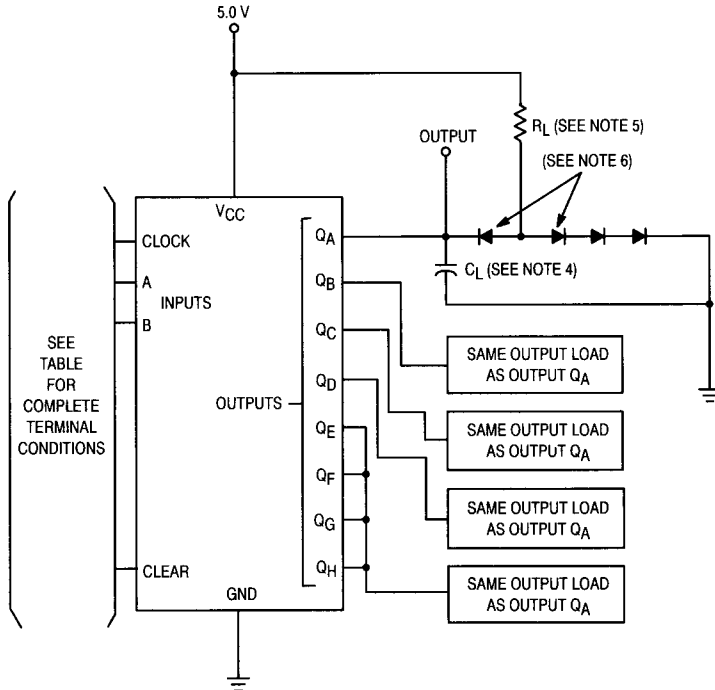


FUNCTIONAL DESCRIPTION

The 'LS164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active HIGH Enable for data entry through the other input. An unused input must be tied HIGH, or both inputs connected together.

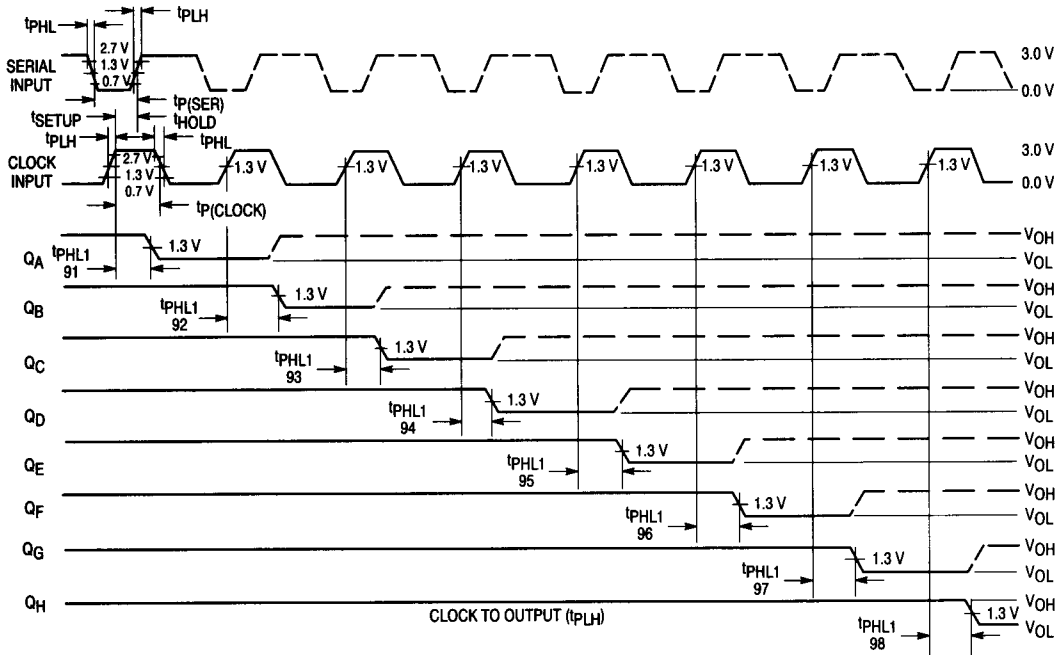
Each LOW-HIGH transition on the Clock (CLK) input shifts data one place to the right and enters into Q_A the Logical AND of the data inputs ($A \cdot B$) that existed before the rising clock edge. A LOW level on the Master Reset (\overline{MR}) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

TEST CIRCUIT

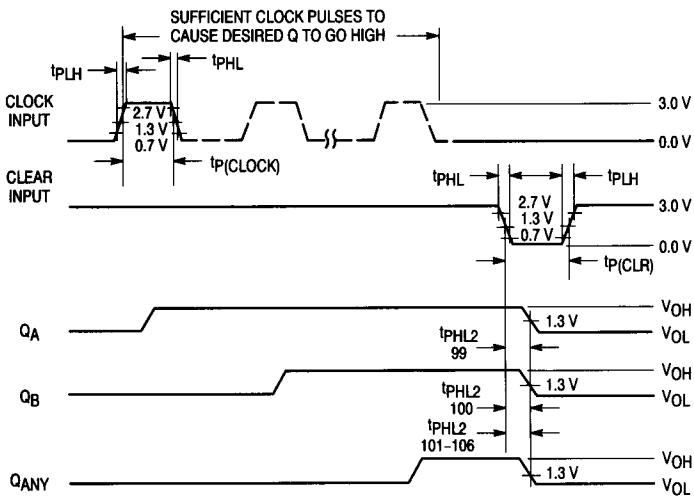


REFERENCE NOTES ON PAGE 5-202

CLOCK TO OUTPUT WAVEFORM

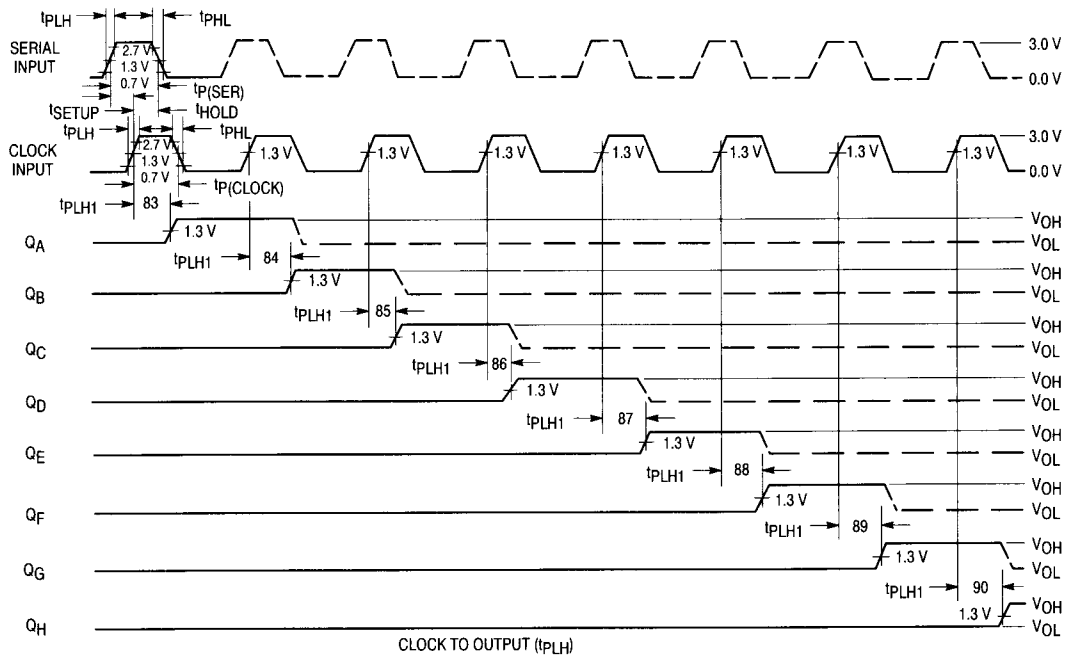


CLEAR TO OUTPUT WAVEFORM



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WAVEFORMS



NOTES:

1. Clock pulse characteristics:
 $PRR \leq 1.0 \text{ MHz}$, $t_{PLH} \leq 15 \text{ ns}$, $t_{p(\text{clock})} = 25 \text{ ns}$.
2. Clear pulse characteristics:
 $t_{PLH} \leq 15 \text{ ns}$, $t_{PHL} \leq 6.0 \text{ ns}$, $t_{p(\text{clear})} = 25 \text{ ns}$.
3. Serial pulse characteristics:
 $t_{PLH} \leq 15 \text{ ns}$, $t_{PHL} \leq 6.0 \text{ ns}$, $t_{p(\text{serial})} = 30 \text{ ns}$, $t_{\text{setup}} = 20 \text{ ns}$,
 $t_{\text{hold}} = 10 \text{ ns}$.
4. $C_L = 50 \text{ pF} \pm 10\%$ including scope probe, wiring and stray capacitance without package in test fixture.
5. $R_L = 2.0 \text{ k}\Omega \pm 5.0\%$.
6. All diodes are 1N3064, 1N916, or equivalent.
7. Prior to initiating tests, the output shall be placed in the proper state.

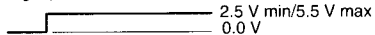
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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OH} = -0.4 mA, CLR = 2.0 V, CLK = (See Notes 1-7), V _{IH} = 2.0 V (both inputs).
V _{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 4.0 mA, other inputs are open, CLK = open, CLR = 0.7 V.
V _{IC}	Input Clamping Voltage		-1.5					V	V _{CC} = 4.5 V, I _{IN} = -18 mA, other inputs are open.
I _{IH}	Logical "1" Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V (other inputs = GND).
I _{IHH}	Logical "1" Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 5.5 V (other inputs = GND).
I _{OS}	Output Short Circuit Current	-15	-100	-15	-100	-15	-100	mA	V _{CC} = 5.5 V, V _{IN} = 4.5 V (both inputs), CLR = 4.5 V, V _{OUT} = GND, CLK = (See Notes 1-7), CR = 4.5 V.
I _{IL}	Logical "0" Output Voltage	-0.12	-0.36	-0.12	-0.36	-0.12	-0.36	mA	V _{CC} = 5.5 V, V _{IN} = 0.4 V, other inputs = 4.5 V.
I _{CC}	Power Supply Current Off		27		27		27	mA	V _{CC} = 5.5 V, V _{IN} = GND (both inputs), CLK = 5.5 V, CLR = (See Note 9).
V _{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 5.0 V, V _{INL} = 0.4 V, and V _{INH} = 2.5 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL1} t _{PHL1}	Propagation Delay /Data-Output Clock to Q _n	5.0	37	5.0	56	5.0	56	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF.
		—	32	—	51	—	51		
t _{PLH1} t _{PLH1}	Propagation Delay /Data-Output Clock to Q _n	5.0	32	5.0	48	5.0	48	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF.
		—	27	—	43	—	43		
t _{PHL2} t _{PHL2}	Propagation Delay /Data-Output Clear to Q _n	5.0	41	5.0	62	5.0	62	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF.
		—	36	—	57	—	57		
f _{MAX} f _{MAX}	Maximum Clock Frequency	22		20		20		MHz	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ. V _{CC} = 5.0 V, C _L = 15 pF.
		25							

NOTES:

1. One pulse minimum.
2. Two pulse minimum.
3. Three pulse minimum.
4. Four pulse minimum.
5. Five pulse minimum.
6. Six pulse minimum.
7. Seven pulse minimum.
8. Eight pulse minimum.
9.  2.5 V min/5.5 V max
0.0 V
10. The limits specified for C_L = 15 pF are guaranteed but not tested.