PRELIMINARY PRODUCT INFORMATION

NEC
ELECTRON DEVICE

BIPOLAR ANALOG INTEGRATED CIRCUIT
μPC1852

1 CHIP LSI WITH I²C BUS FOR PROCESSING U.S.TV MULTIPLEX AUDIO SIGNAL

THe μPC1852 is an IC for processing U.S.TV multiplex audio signal. In this IC, all the functions required for processing U.S. TV multiplex audio signal are incorporated in 1 chip.

This IC can perform mode switching, control such as adjustment of separations and filter etc. by I²C bus.

FEATURES

- Stereo demodulation, SAP demodulation and dbx NR circuits are composed on 1 chip.
- Mode switching and adjustment of separation etc. can be executed fully through I²C bus.
- Vcc = 8 to 10 V
- Input attenuator for easing the interface with IF is incorporated (I²C bus control).
- Output level is 1.4 V_{p-p} (L + R of 100 % modulation)

USE

- TV, VCR for North America

ORDER INFORMATION

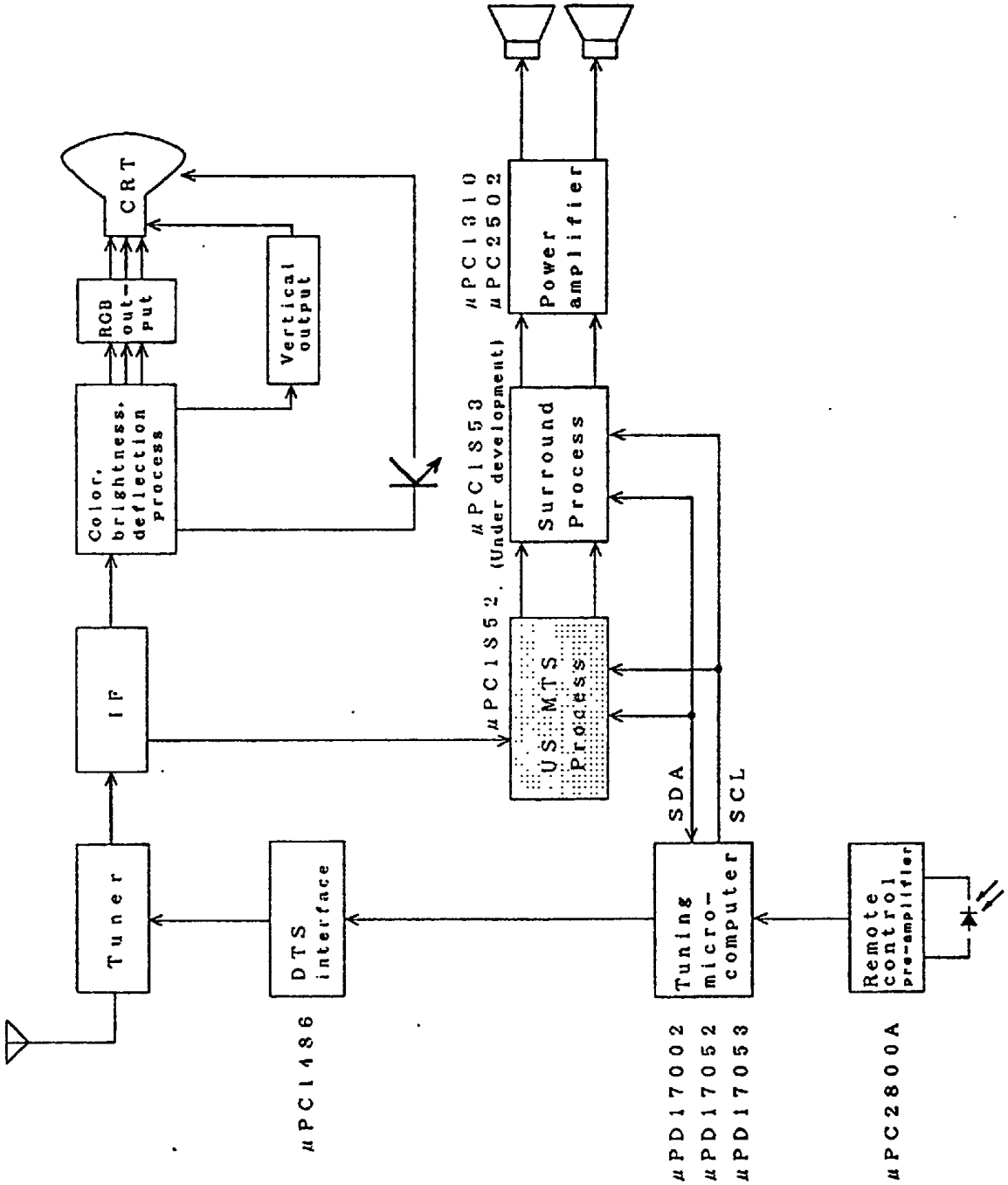
Order name	Package	Quality level
μPC1852CT	28 pin shrink DIP (400 mil)	Standard (for general electronic equipment)

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

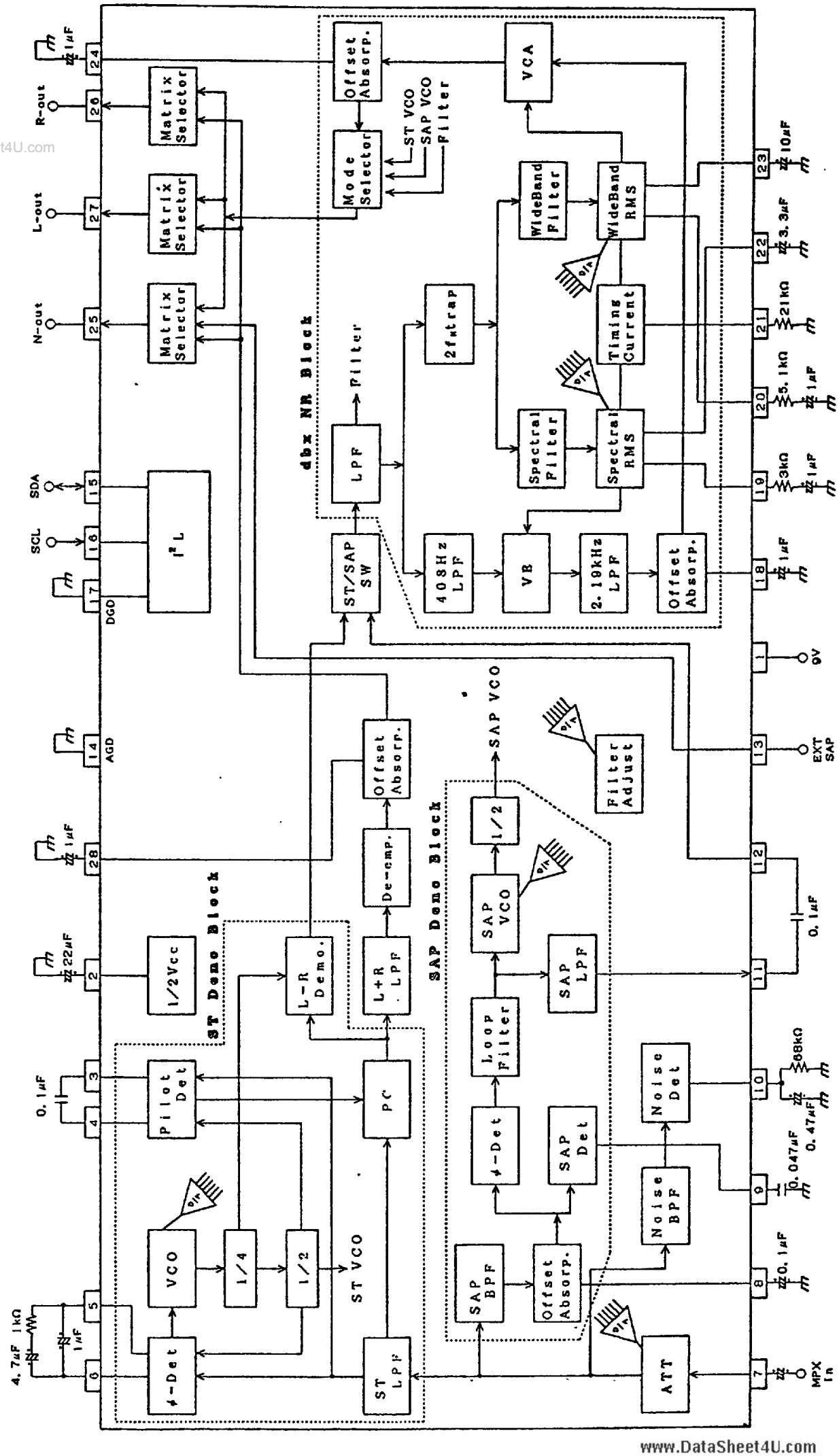
When using μPC1852, the contract with dbx Co. is needed. Proper attention should be paid. Address to be referred to : dbx Technology Licensing
Tel. (03)3378-0915(Tokyo) or (508)529-6003(USA)

The information contained in this document is being issued in advanced of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

SYSTEM BLOCK DIAGRAM (TV)



μPC1852 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Item	Symbol	Conditions	Ratings	Unit
Supply voltage	Vcc		11.0	V
Interface pin voltage	Vcont	SDA, SCL pin	Vcc + 0.2	V
Input signal voltage	Vin	COM pin	Vcc	V
Operating temperature	Topt	Vcc = 9 V	-20 ~ +75	℃
Storage temperature	Tstg		-40 ~ +125	℃

RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	Vcc		8.0	9.0	10.0	V
Interface pin voltage (H)	Vcont(H)		3.5		Vcc	V
Interface pin voltage (L)	Vcont(L)		0		1.5	V
Composit signal input voltage (COM pin)	Vin	L+R signal, at 100% modulation		0.424		V_{pp}
		L-R signal, at 100% modulation		0.848		V_{pp}
		Pilot signal		0.0848		V_{pp}
		SAP signal		0.254		V_{pp}

ABOUT I²C BUS INTERFACE

The μPC1852 has serial bus function. This serial bus is a double wired bus developed by PHILIPS Corporation. It is composed of 2 wires, serial clock line (SCL) and serial data line (SDA).

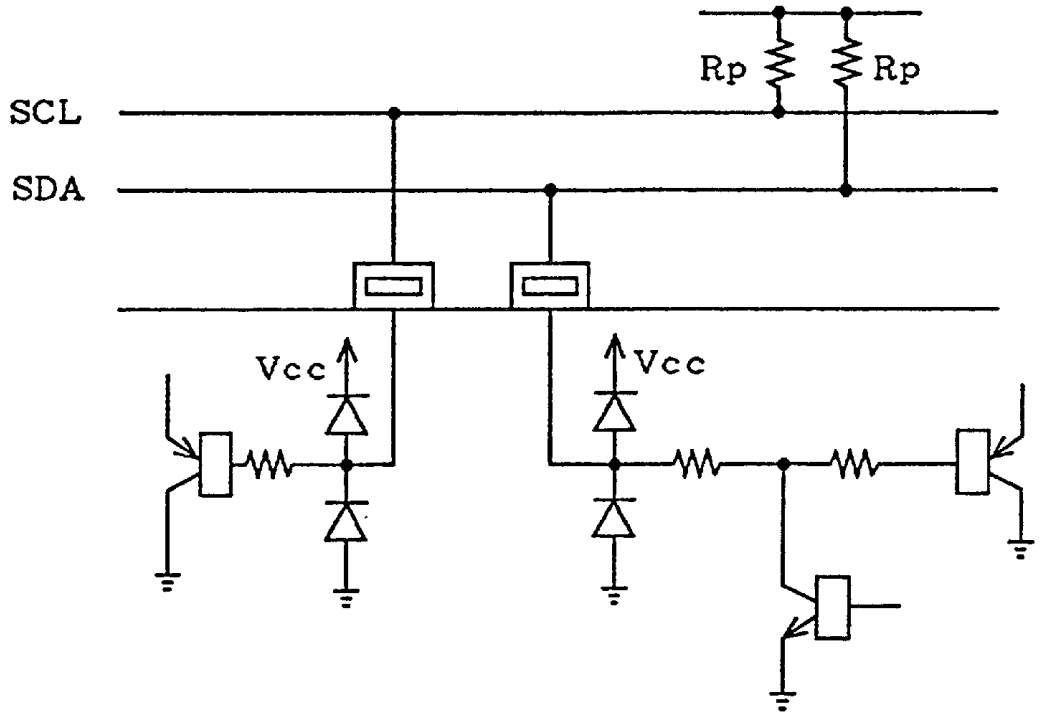
The μPC1852 has built-in I²C bus interface circuit, 7 rewritable registers (8 bits) and a readable register.

SCL (Serial Clock Line)

The master CPU outputs the serial clock to synchronize with the data. According to this clock, the μPC1852 takes in the serial data. Input level is compatible with CMOS.

SDA (Serial Data Line)

The master CPU outputs the data which is synchronized with the serial clock. The μPC1852 takes in this data according to the clock. Input level is compatible with CMOS.



DATA TRANSFER

(1) Start Condition

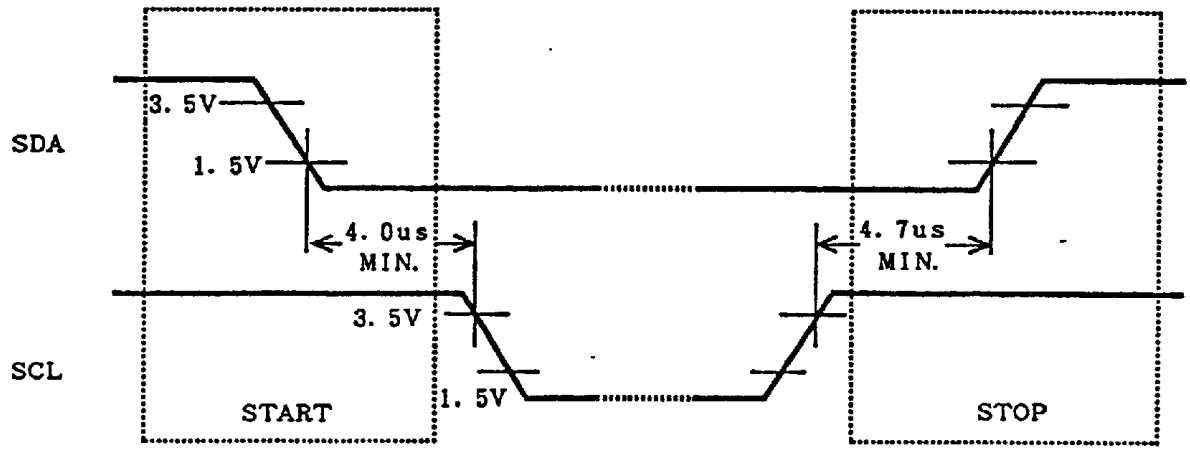
Start condition is made by falling of SDA from "H" to "L" during SCL is "H" as shown in the following figure.

When this condition is received, the μPC1852 takes in the data synchronized with the clock after that.

(2) Stop Condition

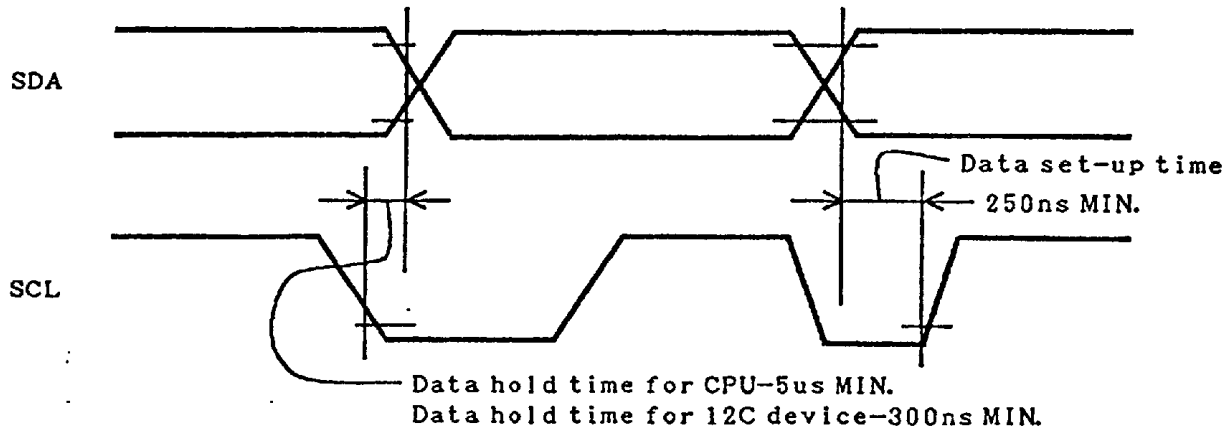
Stop condition is made by rising of SDA from "L" to "H" during SCL is "H" as shown in the following figure.

When this condition is received, the μPC1852 stops to take in or output the data.



(3) Data Transfer

In case of data transfer, data changing should be executed during SCL is "L". When SCL is "H", be sure not to change the data.



DATA TRANSFER FORMAT

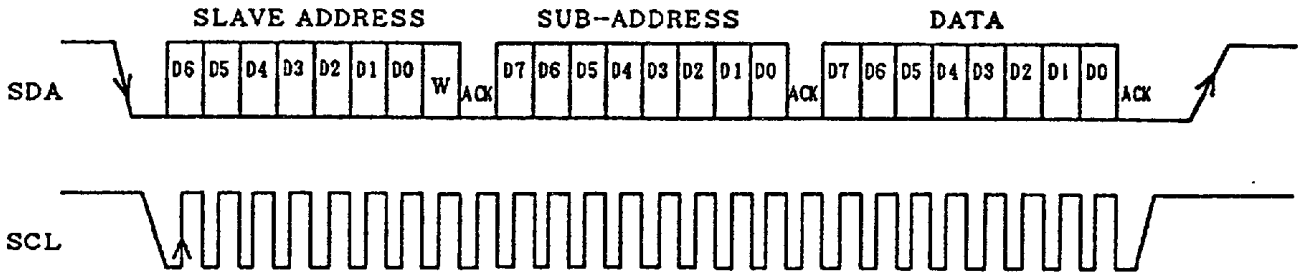
Data is composed of 8 bits unit, and 1 bit of acknowledge bit is always added after this 8 bits data. When the data is transferred, it should be MSB first which is transferred from MSB.

The 1 byte immediately after start condition specifies the chip address (slave address; note). This slave address is composed of 7 bits. The remaining 1 bit is read/write bit which specifies the direction of the data transferred after that.

Read means to transfer the data from the μPC1852 to master CPU. Write means to transfer the data from master CPU to the μPC1852. In case of read mode, write "1" to read/write bit and in case of write mode, write "0" to the bit.

In case of write mode, the byte following the slave address is subaddress byte of the μPC1852. The μPC1852 has 7 subaddresses from SA_0 to SA_6, and each of them is composed of 8 bits. The data which is set to subaddress follows next to this subaddress byte.

The following is an example of data transfer in write mode.



The μPC1852 has auto increment function which increments the subaddress automatically in write mode. (Bit D7 of Subaddress 06H is "1".)

By using this function, once the slave address and the subaddress are set, data can be transferred continuously to the subaddress after that. It is available for initializing, etc..

(1) 1 Byte Data Transfer

The following is the format in case of transferring 1 byte data.

S T A	SLAVE ADDRESS	W	A C K	SUB ADDRESS	A C K	DATA	A C K	S T P

STA : START
W : WRITE MODE
ACK : ACKNOWLEDGE
STP : STOP

(2) Serial Data Transfer (Bit D7 of Subaddress 06H is "1".)

The following is the format in case that 7 bytes data is transferred at once by using auto increment function.

S TA	SLAVE ADDRESS	W	A CK	SUB ADDRESS	A CK	DATA1	A CK	DATA2	A CK	- - -	DATA7	A CK	S TP

STA : START
W : WRITE MODE
ACK : ACKNOWLEDGE
STP : STOP

Transfer "00H" after the start and the slave address like above figure. Transfer the data of SA_0 after the subaddress, and then transfer the data of SA_1, SA_2,..., SA_8 continuously without transferring the stop condition. Finally, transfer the stop condition and terminate.

The increment of the subaddress stops automatically when the subaddress comes to "06H" inside.

If auto increment function is used and the first subaddress is set to "00H", the μPC1852 does not generate the acknowledge (NAK state) and requests stop condition to master CPU after the 7th byte data is transferred.

When the first subaddress set is "01H", it becomes NAK state at the 6th byte.

(3) Data Read

The μPC1852 has one register for reading. The contents of this register can be read by master CPU. The following is the format at data read.

S TA	SLAVE ADDRESS	R EA D	A CK	DATA	N A C K	S T P

STA : START
ACK : ACKNOWLEDGE
NACK : NON ACKNOWLEDGE
STP : STOP

(4) Acknowledge

On I^2C bus, acknowledge bit is added to the 9th bit after data in order to judge whether data transfer is successful or not.

The master CPU judges it with acknowledge condition, "H" and "L".

When this acknowledge period is "L", it means success.

And when the condition is "H", it means failure of transfer or forced release of bus as NAK condition.

The NAK condition is when wrong slave address is transferred to slave IC or data transfer from slave side is finished.

SLAVE ADDRESS

100010×0B····SLAVE RECEIVER
100010×1B····SLAVE TRANSMITTER

TYPE A:×=0
TYPE B:×=1

SUBADDRESS LIST

(1) Write mode

Sub-address	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
00H	0	Noise Detect 0 : SAP OFF 1 : SAP,ST OFF	Input level adjustment D5	D4	D3	D2	D1	D0
01H	0	fH monitor ON/OFF 0 : OFF 1 : ON	ST VCO adjustment D5	D4	D3	D2	D1	D0
02H	0	PC ON/OFF 0 : ON 1 : OFF	Filter adjustment D5	D4	D3	D2	D1	D0
03H	0	0	Low range separation adjustment D5	D4	D3	D2	D1	D0
04H	0	0	High range separation adjustment D5	D4	D3	D2	D1	D0
05H	0	5fH monitor ON/OFF 0 : OFF 1 : ON	SAP VCO adjustment D5	D4	D3	D2	D1	D0
06H	0	0	N output Select (2) 0 : In-SAP 1 : Ex-SAP	N output Select (1) 0 : SAP 1 : MONO	SAP1/2 Select 0 : SAP1 1 : SAP2	ST/SAP Select 0 : ST 1 : SAP	F-MONO ON/OFF 0 : OFF 1 : ON	MUTE ON/OFF 0 : ON 1 : OFF

(2) READ MODE

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
Power on reset 1:Detect	ST PILOT 0 : No 1 : Yes	SAP signal 0 : No 1 : Yes	Noise detection 0 : No 1 : Yes	ST Program 0 : No 1 : Yes	SAP Program 0 : No 1 : Yes	0	0

EXPLANATION OF EACH COMMAND

1. HOW TO ADJUST

1.1 INPUT LEVEL ADJUSTMENT (BIT D5 TO D0 OF SUBADDRESS 00H ARE USED)

1. 300 Hz, 150 mVrms sine wave is to be input into COM pin.
2. Then, the input level adjustment data D5 to D0 of subaddress 00H should be adjusted so that the output levels of ROT pin become 500 ± 10 mVrms.

1.2 ST VCO ADJUSTMENT (BIT D6 TO D0 OF SUBADDRESS 01H USED)

1. Write data "1" into fH monitor control bit D6 of subaddress 01H.
2. Connect the frequency counter to ROT pin, adjust ST VCO adjustment bit D5 to D0 of subaddress 01H so that the displays of the frequency counter become 15.73 kHz ± 0.1 kHz.
3. Write data "0" into fH monitor control bit D6 of subaddress 01H.
   Note : Mute data is to be OFF.

1.3 FILTER ADJUSTMENT (D6 TO D0 OF SUBADDRESS 02H USED)

1. Write data "1" into PC (Pilot Canceler) ON/OFF bit D6 of subaddress 02H.
2. Input the pilot signal (more than 15.73 kHz, 30 mVrms) from COM pin, and adjust the data of the filter adjustment bit (D5 to D0) of subaddress 02H, so that the AC output level of ROT pin becomes minimum.
3. Write data "0" into PC (Pilot Canceler) ON/OFF bit of subaddress 02H.

1.4 SEPARATION ADJUSTMENT (D5 TO D0 OF SUBADDRESS 03H, 04H USED)

1. Input the composite signals (modulation degree 30 %, f=300 Hz, L-only, NR yes) into COM pin, and adjust the low range separation adjustment bit (D5 to D0) of subaddress 03H, so that the output of ROT pin becomes minimum.
   AT this time, bit (D5 to D0) of subaddress 04H is to be set to "20H".
2. Adjust the high range separation adjustment bit (D5 to D0) of subaddress 04H, so that the output of ROT pin becomes minimum by changing the composite signal modulation frequency to 3 kHz.
3. Repeat step 1. with bit (D0 to D5) of subaddress 04H remaining the same status of step 2..

1.5 SAP VCO ADJUSTMENT (D6 TO D0 OF SUBADDRESS 05H USED)

1. Write data "1" into 5fH monitor control bit D6 of subaddress 05H.
2. Connect the frequency counter to ROT pin, adjust SAP VCO adjustment bit D5 to D0 of subaddress 05H so that the displays of the frequncy counter become 78.67 kHz ± 0.5 kHz.
3. Write data "0" into 5fH monitor control bit D6 of subaddress 05H.
   Note : Mute data is to be OFF.

2. METHOD OF THE USER CONTROL (WRITE MODE)

2.1 MUTE FUNCTION (BIT D0 OF SUBADDRESS 06H USED)

ON/OFF of the mute function can be controlled by controlling the data of bit D0 of subaddress 06H.

Data "0".....mute ON
Data "1".....mute OFF

2.2 FORCED MONAURAL CONTROL (BIT D1 OF SUBADDRESS 06H USED)

By controlling the data of bit D1 of subaddress 06H, it can be changed to the monaural mode compulsorily.

Data "0".....Stereo signal is output when choosing the stereo mode during the reception of stereo broadcasting. SAP signal is output when choosing the SAP mode during the reception of SAP broadcasting.

Data "1".....Even when choosing the stereo broadcasting or SAP broadcasting, the mode is compulsorily changed into the monaural mode.

2.3 ST/SAP SWITCHING (BIT D2 OF SUBADDRESS 06H USED)

By controlling bit D2 data of subaddress 06H, the reception of the stereo signal or SAP signal can be selected.

Data "0".....When the stereo signal is being sent out from the broadcasting station, the stereo signal is output.

Data "1".....When SAP signal is being sent out from the broadcasting station, SAP signal is output.

2.4 SAP 1/2 SWITCHING (BIT D3 OF SUBADDRESS 06H USED)

By controlling the bit D3 data of subaddress 06H, SAP1/SAP2 mode can be switched.

Data "0".....In both Lch and Rch, SAP signal can be output (SAP 1 mode).

Data "1".....SAP signal is output from Rch, and L + R (monaural) signal is output from Lch (SAP 2 mode).

2.5 NOISE DETECTION (BIT D6 OF SUBADDRESS 00H USED)

By controlling the bit D6 data of subaddress 00H, Noise detection mode can be switched.

Data "0".....In case of noise detection circuit operates, only SAP demodulation circuit stops.

Data "1".....In case of noise detection circuit operates, both stereo and SAP demodulation circuits stops.

2.6 NOT OUTPUT1 (BIT D4 OF SUBADDRESS 06H USED)

By controlling the bit D4 data of subaddress 06H, the reception of SAP signal or L+R signal can be selected.

Data "0".....SAP signal is output from Normal output terminal.

Data "1".....L+R (monaural) signal is output from Normal output terminal.

2.7 NOT OUTPUT2 (BIT D5 OF SUBADDRESS 06H USED)

By controlling the bit D5 data of subaddress 06H, the reception of Internal SAP signal or External SAP signal can be selected.

Data "0".....Internal SAP signal is output from Normal output terminal.

Data "1".....External SAP signal is output from Normal output terminal.

3. METHOD OF USER CONTROL (READ MODE)

3.1 DETECTION OF NOISE (D4 OF READ REGISTER USED)

By detecting the bit D4 data of the register for read data, the detection about whether the noise level (11.5 fH signal level) is more than 34 mVrms TYP. or not can be done.

When the noise level exceeds 34 mVrms TYP., the bit D4 data of the register for read data becomes "1".

And the operation of SAP, or SAP and stereo demodulation circuit is stopped.

3.2 DETECTION OF SAP BROADCASTING MODE (D5 OF READ REGISTER USED)

By detecting the bit D5 data of the register for read data, the detection about whether SAP signals are sent out or not from the broadcasting station can be done. When detecting SAP signals (5fH), the bit D5 data of the register for read data becomes "1".

3.3 DETECTION OF STEREO BROADCASTING MODE (D6 OF READ REGISTER USED)

By detecting the bit D6 data of the register for read data, the detection about whether stereo pilot signals are sent out or not from the broadcasting station can be done. When detecting stereo pilot signals the bit D6 data of the register for read data becomes "1".

3.4 DETECTION OF SAP RECEPTION MODE (D2 OF READ REGISTER USED)

By detecting the bit D2 data of the register for read data, the detection about whether SAP broadcasting are received or not. When only detecting SAP signal (5fH) in SAP mode, the data of bit D2 becomes "1".

3.5 DETECTION OF STEREO RECEPTION MODE (D3 OF READ REGISTER USED)

By detecting the bit D3 data of the register for read data, the detection about whether stereo broadcasting are received or not. When only detecting stereo pilot signal in stereo mode, the data of bit D3 becomes "1".

3.6 DETECTION OF POWER ON RESET MODE (D7 OF READ REGISTER USED)

When detecting power on reset the data of bit D7 becomes "1".

NOTE FOR USE

1. About External Parts

·As the resistor connected ITI pin, the metal film resistor of accuracy ±1 % should be used, and in the capacitor connected to WTI, STI pins, the tantalum capacitor should be used. (required by the license contract with dbx Co.)

2. About the Modification of Input Sensitivity

- By inserting a resistor between SDT pin and GND, SAP sensitivity can be reduced.
- By changing the resistance value between NDT pin and GND, the noise sensitivity can be modified.

AGD : ANALOG GROUND
DGD : DIGITAL GROUND
SCL : SERIAL CLOCK
SDA : SERIAL DETA
PD1 : PILOT DETECT 1
PD2 : PILOT DETECT 2
φD1 : PHASE DETECT 1
φD2 : PHASE DETECT 2
VRE : VOLTAGE REFERENCE
VCC : POWER SUPPLY
LOT : LEFT OUTPUT
ROT : RIGHT OUTPUT
NOT : NORMAL OUTPUT
VOF : VCA OFFSET ABSORPTION
SOA : SAP OFFSET ABSORPTION
MOA : MONAURAL OFFSET ABSORPTION
dOA : dbx OFFSET ABSORPTION
WT1 : WIDEBAND TIMING
WRB : WIDEBAND RMS BIAS
ITI : I(ELECTRIC CURRENT) TIMING
STI : SPECTRAL TIMING
SRB : SPECTRAL RMS BIAS
SI1 : SAP INPUT 1
SI2 : SAP INPUT 2
SOT : SAP OUTPUT
NDT : NOISE DETECT
SDT : SAP DETECT
COM : COMPOSITE INPUT