National Semiconductor

PRELIMINARY

DM74ALS996 TRI-STATE® Octal D-Type Edge-Triggered Readback Latches

General Description

These 8-bit registers are designed specifically for storing the contents of the input data bus plus providing the capability of reading-back the stored data onto that bus. The Q outputs are designed with bus driving capability.

The edge-triggered flip-flops enter the data on the low-to-high transition of the clock (CLK) when enable (WR) is low. Data can be read-back onto the data inputs by taking the read input (RD) low, in addition to having WR low. Whenever WR is high, both the read-back and write modes are disabled. Transitions on WR should only be made with CLK high in order to prevent false clocking.

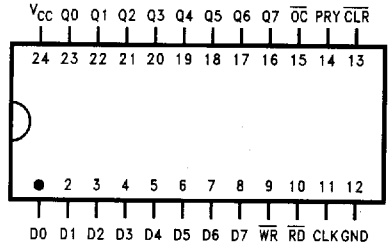
The polarity of the Q outputs can be controlled by the polarity input PRY. When PRY is high, Q will be the same as is stored in the flip-flops. When PRY is low, the output data will be inverted. The Q outputs can be placed into TRI-STATE by taking the output control (OC) high. The output control OC does not affect the internal operations of the register. Old data can be retained or new data can be entered while the outputs are off.

A low level at the clear input (CLR) resets the internal registers low. The clear function is asynchronous and overrides all other register functions.

Features

- TRI-STATE I/O-type read-back inputs
- TRI-STATE bus-driving outputs
- Bus-structured pinout
- True or complementary data at Q outputs

Connection Diagram



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Order Number DM74ALS996WM or DM74ALS996NT
See NS Package Number M24B or N24C

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage (Control Pins)	7V
Input Voltage (D Inputs and Disabled TRI-STATE Outputs)	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Parameter	Min	Nom	Max	Unit
Supply Voltage (V_{CC})	4.5	5.5	5.5	V
High-Level Input Voltage (V_{IH})	2			V
Low-Level Input Voltage (V_{IL})			0.8	V
High-Level Output Current (I_{OH})				
Q			−2.6	mA
D			−0.4	mA
Low-Level Output Current (I_{OL})				
Q			24	mA
D			8	mA
Clock Frequency (f_{CLOCK})	0		35	MHz
Pulse Duration				
CLR Low	10			
CLK Low	14.5			ns
CLK High	14.5			
Setup Time (t_{SU})				
Data before CLK	15			
CLK High before WR	15			ns
CLR High (Inactive) before CLK	10			
Hold Time (t_H)				
Data after CLK	0			ns
RD High after CLK	5			

Electrical Characteristics

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage		V_{CC} = 4.5V	I_I = −18 mA			−1.2	V
V_{OH}	High-Level Output Voltage	All Outputs	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC}−2			V
		Q	V_{CC} = 4.5V	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}	Low-Level Output Voltage	D Outputs	V_{CC} = 4.5V	I_{OL} = 4 mA		0.25	0.4	V
			V_{CC} = 4.5V	I_{OL} = 8 mA		0.35	0.5	
V_{OL}	Low-Level Output Voltage	Q Outputs	V_{CC} = 4.5V	I_{OL} = 12 mA		0.25	0.4	V
			V_{CC} = 4.5V	I_{OL} = 24 mA		0.35	0.5	
I_{OZH}		Q Outputs	V_{CC} = 5.5V	V_I = 2.7V			20	μA
I_{OZL}		Q Outputs	V_{CC} = 5.5V	V_I = 0.4V			−20	μA
I_I		D Inputs	V_{CC} = 5.5V	V_I = 5.5V			0.1	mA
		All Other	V_{CC} = 5.5V	V_I = 5.5V			0.1	
I_{IH}		D Inputs	V_{CC} = 5.5V	V_I = 2.7V			20	μA
		All Other					20	
I_{IL}		D Inputs	V_{CC} = 5.5V	V_I = 0.4V			−0.1	mA
		All Other					−0.1	
I_O			V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}			V_{CC} = 5.5V	Q Outputs High		35	55	mA
			WR, RD Low	Q Outputs Low		55	85	
				Q Outputs in TRI-STATE		42	85	

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: For I/O ports, the parameter I_{IH} and I_{IL} include the TRI-STATE output current.

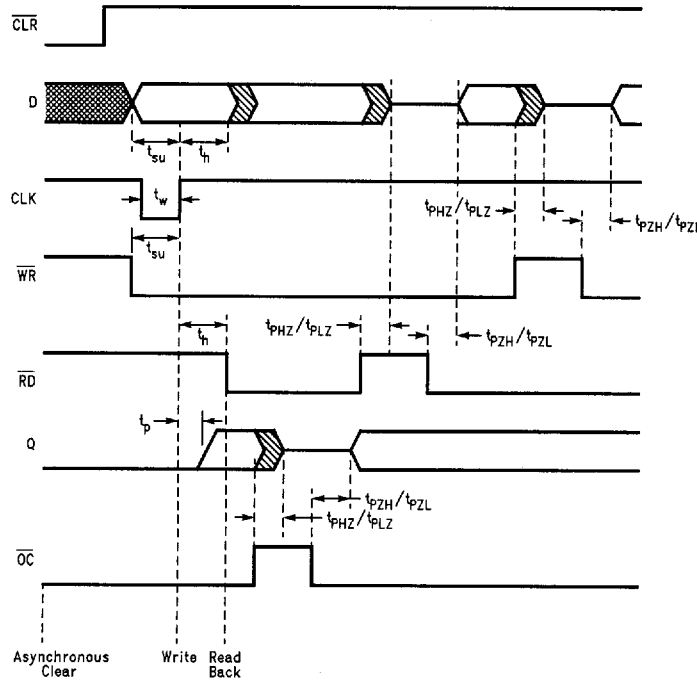
Note 3: The output conditions have been chosen to produce current that closely approximates one-half of the true I_{OS} current.

Switching Characteristics (Note 1)

Parameter	From (Input)	To (Output)	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C			V_{CC} = 4.5V to 5.5V, C_L = 50 pF, T_A = 0°C to +70°C		Units
			Min	Typ	Max	Min	Max	
f_{MAX}				40		35		MHz
t_{PLH}	CLK	Q		15	24	5	28	ns
t_{PHL}	(PRY = H or L)			16	24	5	28	
t_{PLH}	CLR (PRY = L)	Q		15	23	7	27	ns
t_{PHL}	CLR (PRY = H)			13	19	7	23	ns
t_{PLH}	PRY	Q		13	20	5	23	ns
t_{PHL}				13	20	5	23	ns
t_{PHL}	CLR	D		19	25	8	30	ns
$t_{PZL/ZH}$	RD	D		9	15	3	16	ns
$t_{PHZ/LZ}$				10	16	3	19	ns
$t_{PZL/ZH}$	WR	D		9	14	3	16	ns
$t_{PHZ/LZ}$				10	16	3	19	ns
$t_{PZL/ZH}$	OC	Q		8	13	4	15	ns
$t_{PHZ/LZ}$				4	8	1	10	ns

Note 1: See Section 5 for test waveforms and output load.

Timing Diagram



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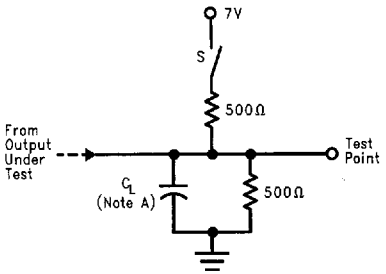
Parameter Measurement Information

Test Circuit for Q Outputs



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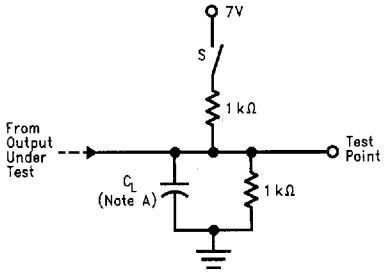
Test Circuit for D Outputs



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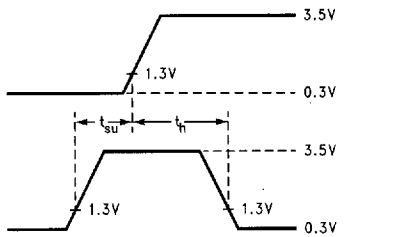
Voltage Waveforms—Setup and Hold Times



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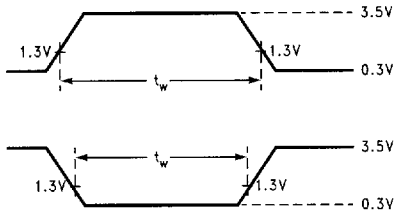
Voltage Waveforms—Setup and Hold Times



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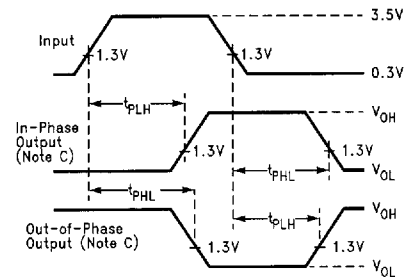
Voltage Waveforms—Propagation Delay Times



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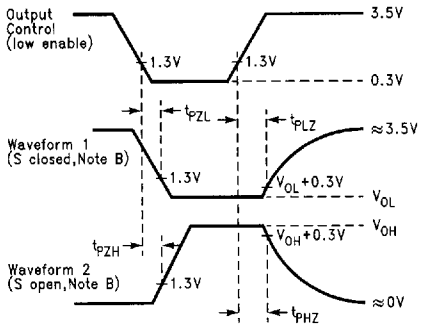
Voltage Waveforms—TRI-STATE Output Times



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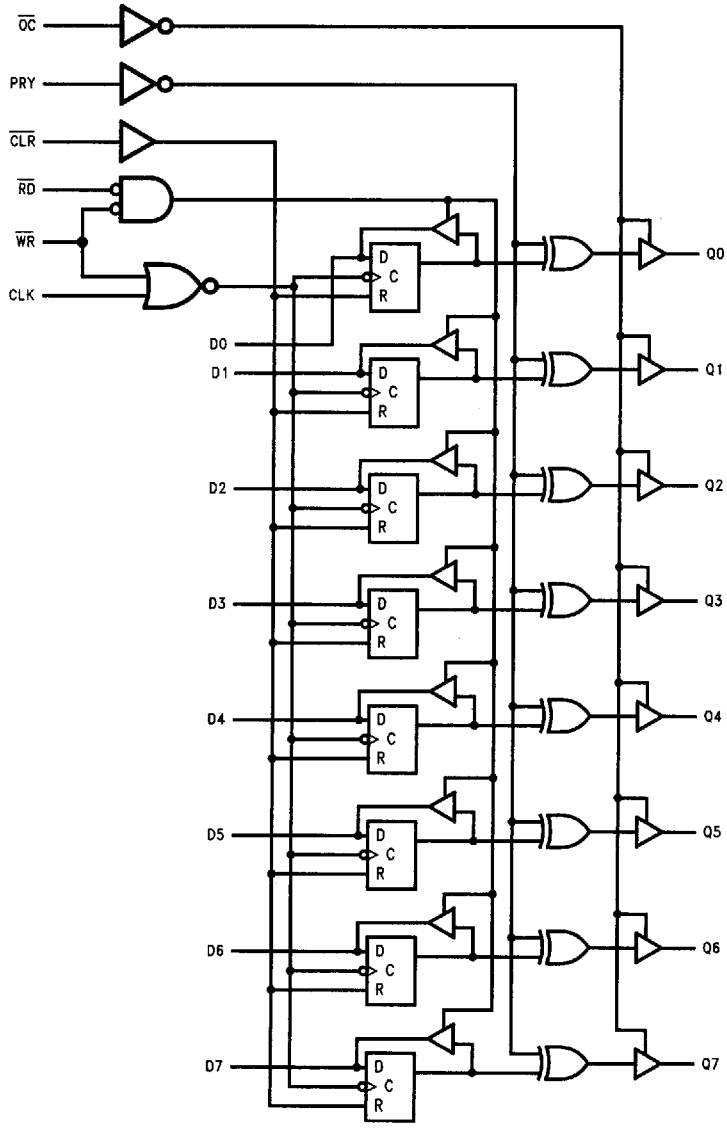
Note A: C_L includes probe and jig capacitance

Note B: Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Note C: When measuring propagation delay times of TRI-STATE outputs, switch S is open.

Note D: All input pulses have the following characteristics: frequency = 1 MHz, $t_r = t_f = 2$ ns, $Z_O = 50\Omega$.

Logic Diagram



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