National Semiconductor

February 1996

NM29A040/080
4-Mbit/8-Mbit CMOS Serial FLASH E²PROM

General Description

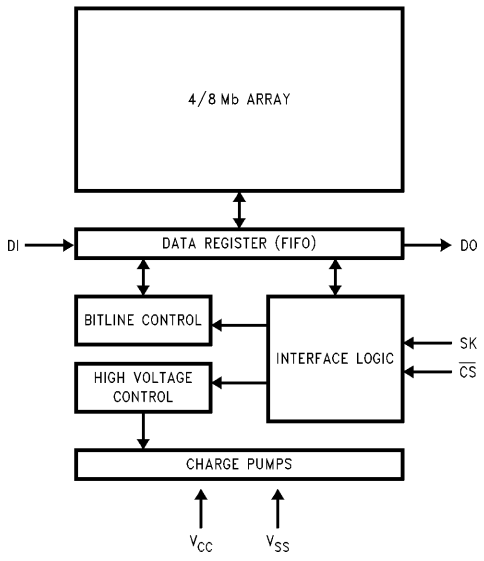
The NM29A040/080 are 4-Mbit and 8-Mbit Flash memories designed with a MICROWIRE™ serial interface. All of the features of the device are designed to provide the most cost effective solution for applications requiring low bandwidth file storage. Examples of these applications include digital answering machines and personal digital recorders (digital audio) or FAX and digital scanners (digital imaging). The Serial Flash requires only a single 5V power supply, has a small erase block size (4 kbytes) and a low EMI serial interface.

The NM29A040/080 have been designed to work seamlessly with National's CompactRISC™ family (e.g. NSAM266) of processors. In this manner National is able to provide the complete system solution to digital audio recording (processor, CODEC, Flash memory, software) or digital imaging.

Features

- Single 5V ±10% power supply
- 4 kbyte erase block
- Organized as 128 (256) Blocks per 4-Mbit (8-Mbit) Device
  - — 128 pages per block
  - — 32 bytes per page (256 bits)
- MICROWIRE™ compatible interface
- Low operating current (typical)
  - — 5 mA read current
  - — 15 mA write current
  - — 10 mA erase current
  - — 5 μA standby current
- 100k write/erase cycle endurance
- Offered in PLCC and SOIC packages

Block Diagram



TL/D/12475–1

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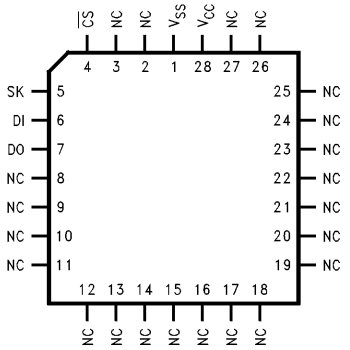
NM29A040/080 4-Mbit/8-Mbit CMOS Serial FLASH E²PROM

Connection Diagrams

Plastic Chip Carrier (V)



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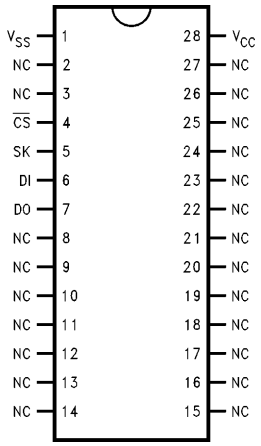
NM29A040V
NS Package Number V28A

Small Outline Package (M)



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NM29A040M
NM29A080M
NS Package Number MA28A

Pin Assignments

DO	Serial Data Output
DI	Serial Data Input
SK	Serial Data Clock
$\overline{CS}$	Chip Select
NC	No Connection

Ordering Information

Commercial Temperature Range (0°C to +70°C)

Order Number
NM29A040V
NM29A040M
NM29A080V
NM29A080M

Extended Temp. Range (−40°C to +85°C)

Order Number
NM29A040EV
NM29A040EM
NM29A080EV
NM29A080EM

Pin Functions

SERIAL DATA INPUT: DI

The DI pin is used for transferring in commands and data. Data is latched on the rising edge of SK.

SERIAL DATA OUT: DO

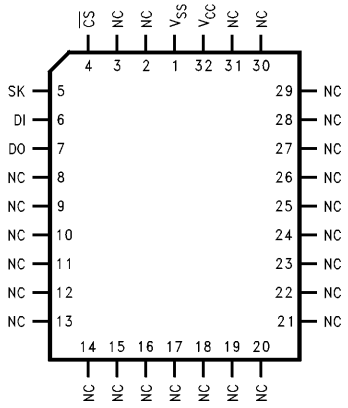
The DO pin is used for transferring out status and data. Data output will change following the falling edge of SK.

CHIP SELECT: $\overline{CS}$

This signal indicates which device is selected. When this signal is inactive the device ignores SK. This signal can be tied to ground when there is only one Serial Flash device. The $\overline{CS}$ pin may be pulled high to reset command input.

SERIAL DATA CLOCK: SK

This is the standard synchronous MICROWIRE clock which determines the rate of data transfer. On each toggle, one data bit is shifted into or out of the Serial Flash.



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NM29A080V
NS Package Number VA32A

System Concepts

The NM29A040/080 are 4-Mbit and 8-Mbit NAND Flash designed to provide the most cost effective solution for file storage applications. These applications include digital audio recording, digital image storage and data logging applications.

For digital audio storage, the NM29A040/080 have been matched with National's NSAM266 voice processor. Applications that can benefit from this combination include digital answering machines, personal digital recorders, pagers and voicemail systems. When combined with National Semiconductor's CompactSPEECH™ embedded software and the NSAM266 processor, customers can quickly bring to market systems capable of recording up to 15 minutes of audio on a single 4 Mb device. Multiple NM29A040/080's can be used to extend the record time up to 2 hours.

Digital imaging applications include FAX machines, handheld scanners and digital cameras. Combining the NM29A040/080 with the CompactRISC family of embedded processors can enable complete solutions for image storage.

Data logging applications can take advantage of the NM29A040/080's simple interface and nonvolatility to allow simple 8-bit microcontroller based systems to have access to over 4 Mb of storage. The nonvolatility ensures data integrity in remote, battery powered applications.

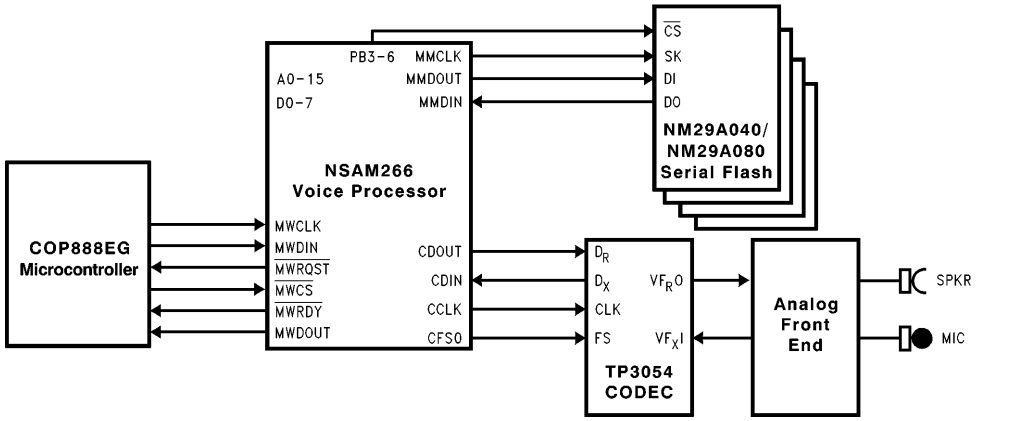

FIGURE 1. Digital Audio Recording Solution

TABLE I. Data Transfer Rates

	Transfer Rates		Total Time	
	Page	Block	Page	Block
Read	1.02 Mbits/s (127.5 kbytes/s)	2.61 Mbits/s (325.8 kbytes/s)	251 μs	12.6 ms
Write	406.3 kbits/s (50.8 kbytes/s)	536.4 kbits/s (67.1 kbytes/s)	630 μs	61.1 ms
Erase	—	—	—	6 ms

Device Operation

The basic functions required for storing messages or images on the NM29A040/080 are Page Read, Page Write, and Block Erase. These functions can be implemented by combining the different instructions for the NM29A040/080 in the following sequences.

PAGE READ

Page Read will read out the 32 bytes of a page for the specified address. To continue reading the page at the next address, an Increment command (90H) can be issued. In this way the system can avoid repeatedly using the three byte Set-Address command. The Increment command is then followed by the Read command and proceeds in the same manner as shown in *Figure 2*.

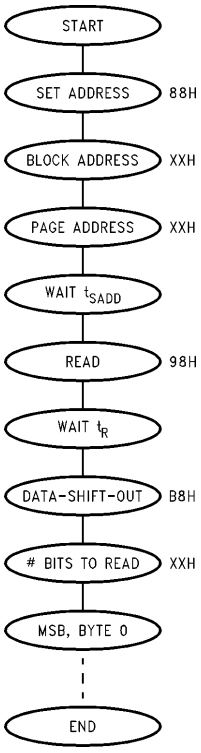

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FIGURE 2. Page Read Sequence

PAGE WRITE

Page Write sequence will write up to 32 bytes into a specified page. Like the Page Read sequence, the Increment command can be used to quickly set the address to the next page for writing data sequentially into a block.

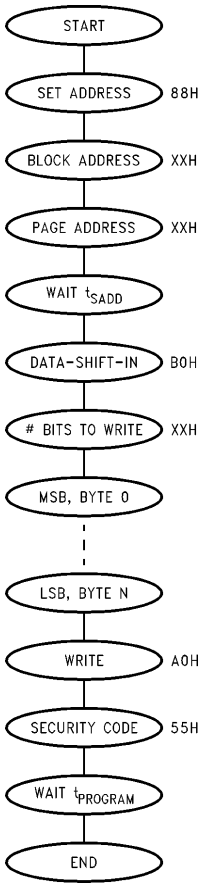

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FIGURE 3. Page Write Sequence

Device Operation (Continued)

BLOCK ERASE

The Block Erase sequence erases a specified block (4 kB) of data. Flash memory devices require that a block be in an erased state prior to writing to a memory cell. In this manner, a block must be erased prior to the recording of any messages or storage of any images.

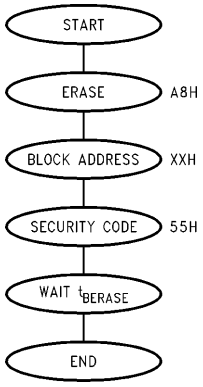

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FIGURE 4. Block Erase Sequence

Functional Description

ORGANIZATION

The NM29A040/080 are 4-Mbit and 8-Mbit devices respectively organized as 128/256 blocks of 128 pages. A block is the smallest unit that can be erased and is 4 kbytes in size. Within a block are 16 rows of 8 pages, each row 256 bytes long. Each page is 32 bytes long. Read and write operations always operate on a page at a time.

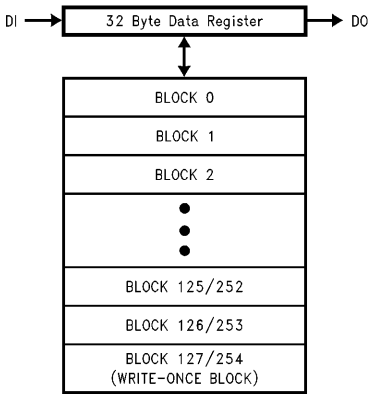

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FIGURE 5. Device Organization

Reading or writing data to the Serial Flash involves clocking data into or out of the data register. The data register is a 32-byte wide shift register, equivalent in size to one page. When shifting in a full page, writing to the array and then reading out the same page, the first bit shifted in will be the first bit shifted out. If for example only 5 bytes are shifted in, written to the array and then the same page is read out, 27 bytes should be shifted out before the original 5 bytes will be shifted out. See Note 4 in the notifications section for an explanation of multiple page writes and masking.

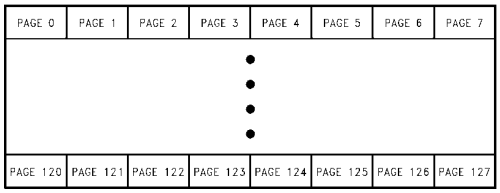

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FIGURE 6. Block Organization

WRITE ONCE BLOCK

The NM29A040 contains 127 blocks (blocks 0 thru block 126) which are fully accessible to the user for reading, writing and erasing. The final block, number 127, has been set aslde as a write once block. The pages in this block may only be written to once. Once the data is written, it may not be erased. In this manner, block 127 may be used for storing system configuration information that cannot be lost.

The NM29A080 operates in a similar manner but has 253 blocks that are fully accessible. Block 254 contains the unusable block information although this block has 256 pages as opposed to the standard 128 pages.

The last block is not accessible through the normal Read and Write commands. Special commands for Read (D0H) and Write (F0H) are used to perform the last block operations. An erase operation is not available or usable on the last block.

DATA REGISTER

The data register is a 32-byte FIFO that is used to shift data into or out of the device. When a write operation is performed, all 32 bytes are written to the currently addressed page. Refer to Note 4 for how to write less than 32 bytes to a page.

The data register may be used as an on-chip holding area for partial page data. For example, if data is acquired externally in 8-byte multiples, the data register can be used to hold each 8-byte segment. After the 4th such data segment, an entire page of data will have been accumulated, at which point the write command mat be issued. No data may be shifted into or out of the data register while the device is busy.

READY/$\overline{\text{BUSY}}$ OUTPUT

When the Serial Flash device is selected with $\overline{\text{CS}}$ held low, then the DO pin reflects the Ready/$\overline{\text{Busy}}$ state of the device. This is true at all times except when reading data out of the device, as in the Get-Status command or the Data-Shift-Out command. When the device is unselected, the DO output is in a high impedance state.

Instruction Set

The NM29A040/080 have 12 instructions which are described in Table II. The command byte (Byte 1) has the following format:

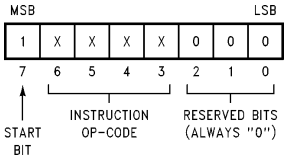

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FIGURE 7. Command Byte

The MSB is always a ''1'' and is considered the start bit; all leading ''0's'' are ignored. The first ''1'' detected on the rising edge of SK indicates the initiation of a command. The next 4 bits are the instruction opcode. The final 3 bits are reserved and must always be ''0''. Data input of a command other than those listed in Table II is prohibited. Data may be corrupted if unspecified commands are used.

TABLE II. Instruction Set

Command	Byte 1	Byte 2	Byte 3
Get-Status	80H		
Set-Address	88H	Block Address	Page Address
Increment	90H		
Read	98H		
Write	A0H	55H	
Erase	A8H	Block Address	55H
Data-Shift-In	B0H	# Bits to Shift-In	
Data-Shift-Out	B8H	# Bits to Shift-Out	
Read Last Block	D0H		
Write Enable	E0H		
Write Disable	E8H		
Write Last Block	F0H	55H	

GET-STATUS

The Get-Status command allows the user to determine the status of the NM29A040/080. It may be issued whether the device is busy or not. The output is a status byte which indicates the internal state of the Serial Flash. The output byte is defined as:

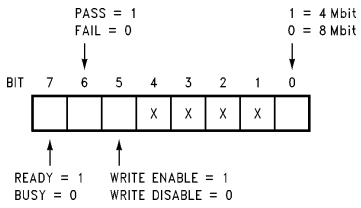

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FIGURE 8. Get-Status Byte

Bit 7 of the status byte tells whether the device is busy performing an operation (write, erase, etc.) or is ready for a new command. Bit 6 tells if a previous write or erase cycle completed successfully. Bit 5 tells if the device is in a write enabled or disabled mode. Bit 0 distinguishes between a 4-Mbit device and an 8-Mbit device. The remaining bits are reserved for future use and may appear as any value (''1'' or ''0'').

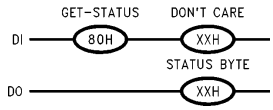

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FIGURE 9. Get-Status Sequence

SET-ADDRESS

The Set-Address command defines which page and block of the memory is affected by an operation. The Set-Address command is followed by two bytes, the first indicating the block number and the second indicating the page number. The block number chooses one of the 127/254 blocks while the page number chooses one of the 128 pages within the given block. The Set-Address command is usually followed by a Read, Write, or Data-Shift-In command. Between the page address byte and the next command there is a delay of t_{SADD}. The address that is selected remains the active address until a new Set-Address or Increment command is given.

INCREMENT

The Increment command automatically increments the selected page address. When the Increment command is given after the last page in a block has been read, the address will roll over to the first page in the following block. When the last page in the last addressable block is read out followed by an Increment command, the new address is indeterminate.

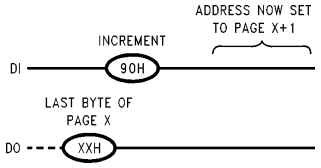

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FIGURE 10. Increment Sequence

READ

The Read command transfers data from the selected page of the memory array into the data register. To read the data out through DO, the Read command is followed by the two byte Data-Shift-Out command. There is a delay of t_R between the Read command and the Data-Shift-Out command as the data is transferred from the array to the on-chip buffer. During t_R the status byte will indicate that the part is busy.

WRITE

The Write command programs data from the 32-byte shift register into a page in the memory array for the currently selected address. A security code 55H follows the Write command to ensure against accidental Writes. Get-Status may be used to ensure that the operation was successful. The Write command will be ignored if Write-Enable has not been set.

Instruction Set (Continued)

ERASE

The Erase command erases a single block. The Erase command is followed by a single byte telling which block to erase. In this manner, no Set-Address sequence is required to erase a block. Following the block address byte is a single byte security code, 55H, that is used to prevent inadvertent erasure. Get-Status may be used to check if the operation was completed successfully. At the completion of the Erase command, the selected address is undetermined. A Set-Address command is required before any subsequent Read or Write.

DATA-SHIFT-IN

The Data-Shift-In command is used to send data into the on-chip buffer. The number of bits sent into the buffer is determined by an 8-bit argument following the command. The argument is always 1 less than the actual number of bits to shift in. For example, to shift in all 32 bytes (256 bits), the argument would be FFH (255). To shift in just 4 bytes (32 bits), the argument would be 1FH (31). Following the argument, the data is shifted in through DI. Data-Shift-In may come before or after the Set-Address sequence when performing a page write operation.

DATA-SHIFT-OUT

The Data-Shift-Out command is used to shift data out of the on-chip buffer through DO. The number of bits sent out is determined by an 8-bit argument following the command. The argument is always 1 less than the actual number of bits to shift out. For example, to shift out all 32 bytes (256 bits), the argument would be FFH (255). To shift out 2 bytes (16 bits), the argument would be 0FH (15). Following the argument, the data is shifted out through DO. Data shifted out during this command is also internally shifted back into the data register. Thus after shifting all 256 bits, the contents of the data register remain unchanged.

WRITE ENABLE

The Write Enable command is used as a security check against inadvertent writes or erases to the device. When this command is issued, any subsequent Write or Erase commands proceed in the normal fashion. If the Write Enable command is not given or the device is in the Write Disable mode then a write to any page or erase to any block will not be allowed. Use the Get-Status command to determine whether the device currently is in the Write Enabled or Disabled mode. The NM29A040/080 will always power up in the Write Disable mode. This command may be issued while the device is busy. Any change in the Write Enable status will affect the next write or erase operation that is issued.

WRITE DISABLE

The Write Disable command is used to prevent inadvertant writes or erases. Once this command is executed, all subsequent Write or Erase commands will not be accepted. This command may be issued while the device is busy. Any change in the Write Enable status will affect the next write or erase operation that is issued.

READ LAST BLOCK

The Read Last Block command is used to read the contents of Block 127 (4-Mbit) or Block 254 (8-Mbit). The Read Last Block operation proceeds like a normal read operation except that the block number is ignored in the Set-Address sequence. The block address is automatically set to Block 127 or 254. The Set-Address command is still necessary to set the page to be read. In the case of the 8M, the page address can range from 0−255 for purposes of reading or writing the last block.

WRITE LAST BLOCK

The Write Last Block command writes a page of data to the currently selected page of Block 127 or 254. The Write Last Block command operates like a normal write command except the block number is ignored in the Set-Address sequence. The block address is automatically set to Block 127 or 254. The Set-Address command is still necessary to set the page to be written. In the case of the 8M, the page address can range from 0−255 for purposes of reading or writing the last block. The Write Last Block command is followed by a security code (55H). Once the information has been written into the memory array, it may not be erased.

Notifications

(1) Interruption by $\overline{CS}$ Going High

When the NM29A040/080 begins reading a page from the array (t_R), writing a page to the array (t_{PROG}), or erasing a block (t_{BERASE}), the operation will complete regardless of the state of $\overline{CS}$. The $\overline{CS}$ pin may go high during these operations. If $\overline{CS}$ is held low during these operations the DO pin will reflect the state of the operation with a low state (busy) while the operation is being executed. When the operation is completed, DO will pull high to reflect the ready state.

(2) Command Reset

The NM29A040/080 command register is reset whenever $\overline{CS}$ changes from low to high. As long as the device is powered, the data register will continue to hold its data. The state of $\overline{CS}$ does not affect on-going operations as described in Notification (1).

(3) Power-Up

On power-up, the NM29A040/080 is set in the write disable mode. This prevents any spurious writes to the device. To enable writes or erases, the Write Enable (E0H) command must be given. At power-up, the 32-byte shift register will contain unknown data.

(4) Multiple Programs to a Page

It is possible to program a page more than one time between block erases. However, each bit (cell) may only be programmed once. (Once data has been changed fro a ''1'' to a ''0'', a block erase operation is required to change the data back to a ''1''.) After a block is erased, all bytes will read as ''FFH''. When less than 32 bytes need to be programmed into a page, the remaining bytes may be masked by writing ''FFH'' to those locations. In this way the cells are not changed from their erased states. Later, these bytes can be programmed with the desired data. It is suggested that the number of writes to a page between block erases be held to as few as possible.

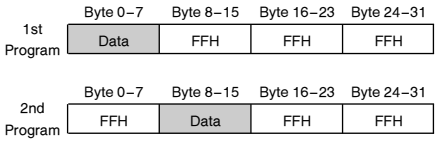


FIGURE 11. Multiple Page Program

(5) Identification of Unusable Blocks

The NM29A040/080 may contain unusable blocks. These unusable blocks are due to bit errors in the block. An unusable block will not affect adjacent blocks. The location of these blocks may be found pre-programmed in Block 127 (4 Mb) or 254 (8 Mb). Each page in Block 127 or 254 corresponds to a block in the array at a similar address. For example, Page 3 in Block 127 corresponds to Block 3. If Block 3 is a usable block, then all bytes in Page 3 of Block 127 will read out ''FFH''. If Block 3 is an unusable block, then some of the bytes in Page 3 of Block 127 will read out data other than ''FFH''. For customers using the NM29A040/080 with the NSAM266 speech processor, the CompactSPEECH embedded software automatically locates the unusable blocks and works around these locations when performing Read, Write and Erase operations.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply (V_{CC})	−0.6V to 7.0V
Input Voltage (V_{IN})	−0.6V to 7.0V
Input/Output Voltage ($V_{I/O}$)	−0.6V to V_{CC} ±0.5V (≤7V)
Power Dissipation (P_D)	300 mW
Soldering Temperature (T_{solder}, 10 sec.)	260°C
Storage Temperature (T_{stg})	−55°C to +150°C
Operating Temperature (T_{opr})	−40°C to +85°C

Recommended Operating Conditions

	Min	Typ	Max	Units
Power Supply (V_{CC})	4.50	5.0	5.50	V

DC Operating Characteristics (T_A = 0°C to +70°C, V_{CC} = 5V ±10%)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Leakage Current	V_{IN} = 0V − V_{CC}			±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.4V − V_{CC}			±10	μA
I_{CC01}	Operating Current Data Input/Output	t_{CYCLE} = 500 ns		5	20	mA
I_{CC02}	Programming Current			15	60	mA
I_{CC03}	Erasing Current			10	40	mA
I_{CCS1}	Standby Current	$\overline{CS}$ = V_{IH}		120	500	μA
I_{CCS2}	Standby Current	$\overline{CS}$ = V_{CC} − 0.2V		5	50	μA
V_{OH}	High Level Output Voltage	I_{OH} = −400 μA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2.1 mA			0.4	V
V_{IH}	High Level Input Voltage		2.0		V_{CC} + 0.5	V
V_{IL}	Low Level Input Voltage		−0.3*		0.8	V

* −2V (Pulse width ≤20 ns)

AC Electrical Characteristics (T_A = 0°C to +70°C, V_{CC} = 5V ±10%)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{SK}	SK Clock Frequency		0		4	MHz
t_{SKH}	SK High Time		125			ns
t_{SKL}	SK Low Time		125			ns
t_{SKS}	SK Setup Time	Relative to $\overline{CS}$ Falling Edge	50			ns
t_{CS}	Minimum $\overline{CS}$ High Time		250			ns
t_{CSS}	$\overline{CS}$ Setup Time	Relative to SK Rising Edge	100			ns
t_{DIS}	DI Setup Time	Relative to SK Rising Edge	50			ns
t_{CSH}	$\overline{CS}$ Hold Time	Relative to SK Falling Edge	50			ns
t_{DIH}	DI Hold Time	Relative to SK Rising Edge	20			ns
t_{DF}	$\overline{CS}$ to DO in TRI-STATE®	AC Test			100	ns
t_{DH}	DO Hold Time	Relative to SK Falling Edge	0			ns
t_{PD}	Output Delay	Relative to SK Falling Edge			100	ns
t_{SADD}	Set Address Time	AC Test			200*/400**	μs
t_{PROG}	Page Program Time			400	5000	μs
t_{BERASE}	Block Erase Time			6	100	ms
t_R	Page Read Transfer Time			9	25	μs

*NM29A040

**NM29A080

Number of Valid Blocks

The NM29A040/080 may contain unusable blocks. These unusable blocks should not be used to store data. Notification (5) describes how to identify unusable blocks.

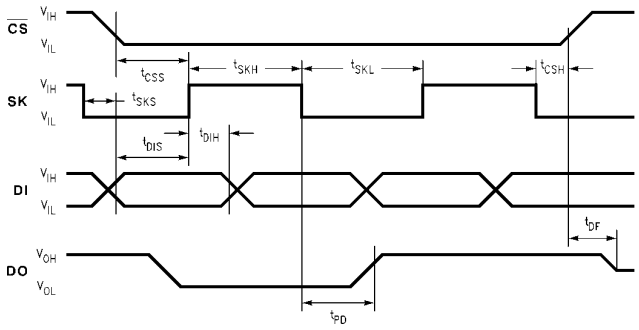
Symbol	Parameter	Min	Typ	Max	Units
N_{VB4}	4-Mbit Number of Valid Blocks(1)	117	TBD	127(2)	Block
N_{VB8}	8-Mbit Number of Valid Blocks(1)	234	TBD	254(2)	Block

Note 1: A valid block is a block having all 4096 bytes usable. An unusable block is a block in which a minimum of one bit is unusable.

Note 2: Not including Block 127 (4-Mbit) or 254 (8-Mbit).

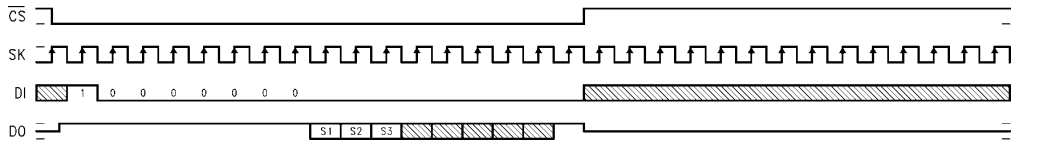
Timing Diagrams

Synchronous Data Timing



TL/D/12475–16

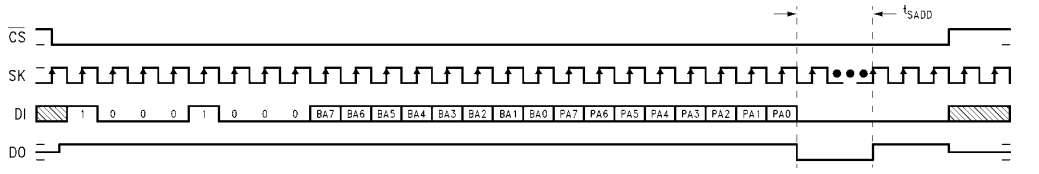
Get Status Timing



TL/D/12475–17

Note: To avoid putting the device in an unknown state, DI should be held low when not clocking in data/commands.

Set Address Timing

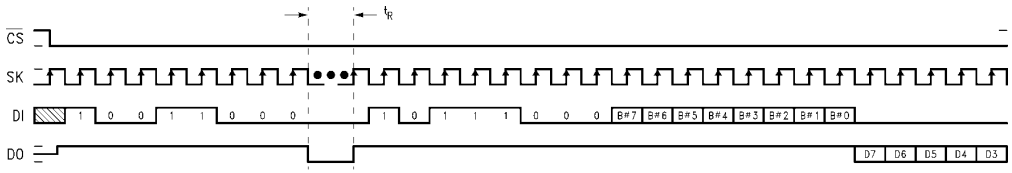


TL/D/12475–18

Note: $\overline{CS}$ can be pulled high during t_{SADD}, t_R, t_{PROG}, and t_{BERASE}. However, DO will only reflect the status (ready/busy) while $\overline{CS}$ is low.

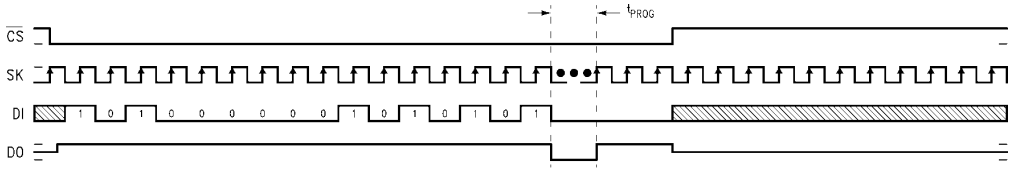
Timing Diagrams (Continued)

Read and Data-Shift-Out Timing



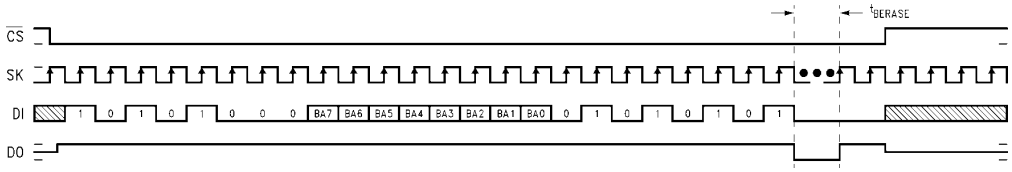
TL/D/12475–19

Write Timing



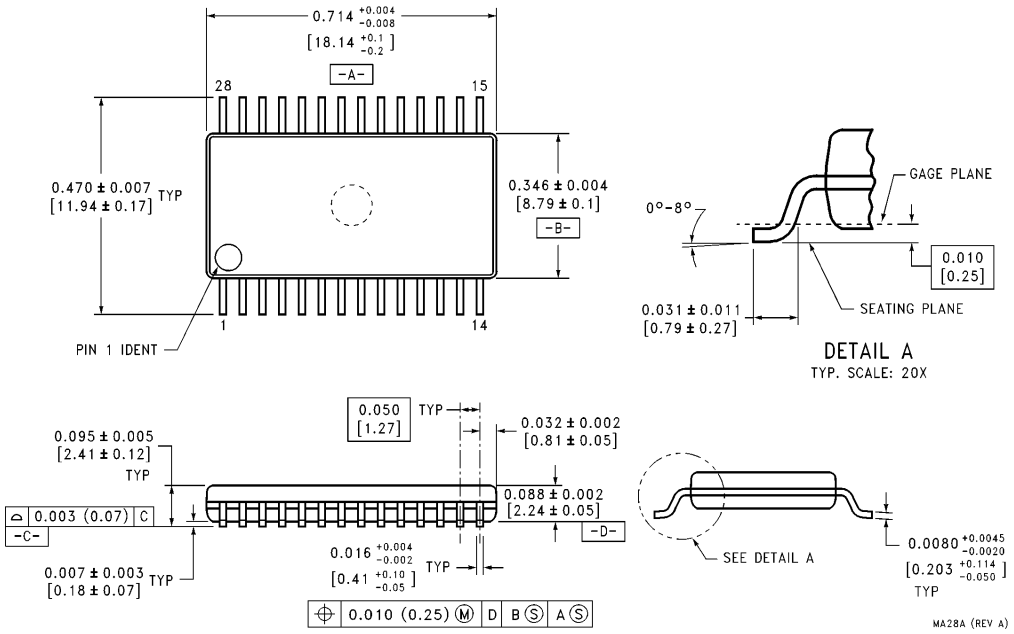
TL/D/12475–20

Erase Timing



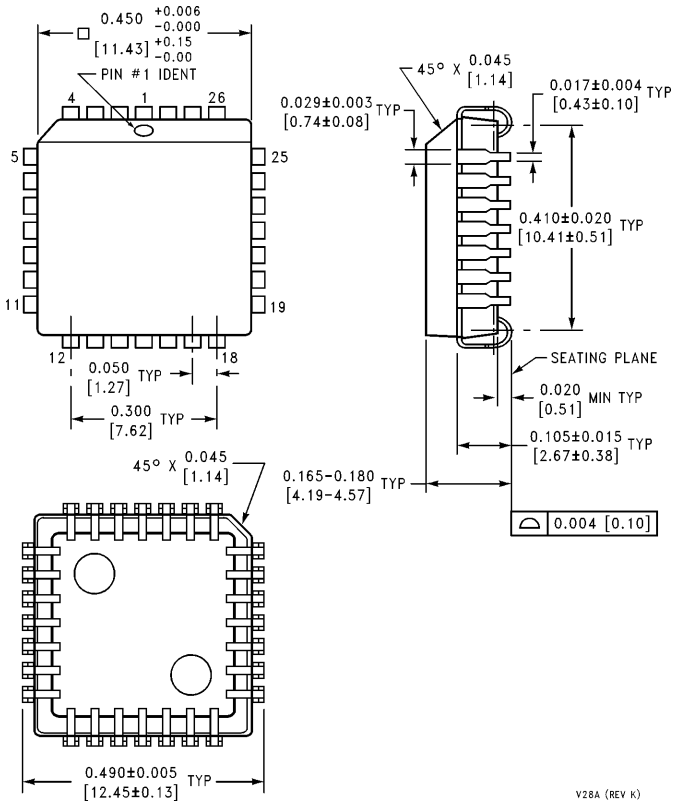
TL/D/12475–21

Physical Dimensions inches (millimeters)



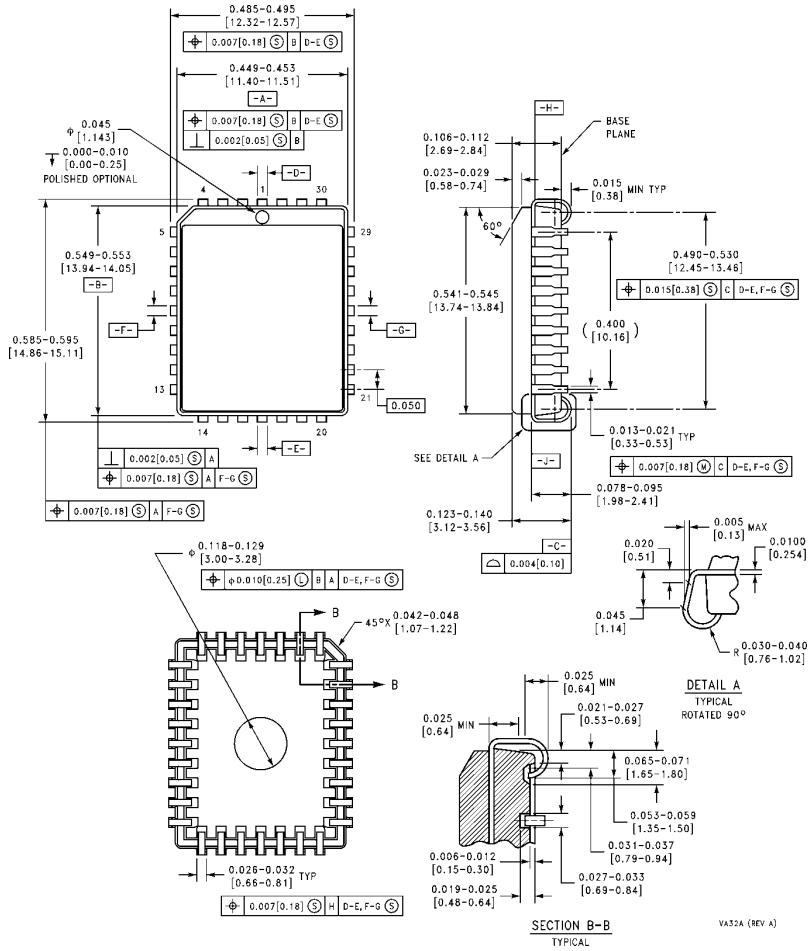
Molded Small Outline Package
Order Number NM29A040M/NM29A080M
NS Package Number MA28A

Physical Dimensions inches (millimeters) (Continued)



Molded Plastic Leaded Chip Carrier
Order Number NM29A040V
NS Package Number V28A

Physical Dimensions inches (millimeters) (Continued)



Molded Plastic Leaded Chip Carrier
Order Number NM29A080V
NS Package Number VA32A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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