



TRI-STATE® 8-Bit Latches

General Description

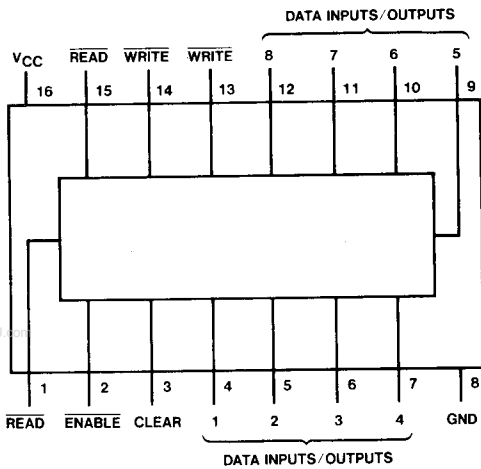
By utilizing TRI-STATE circuitry on the outputs, the inputs and outputs can be accessed on the same pins, and these circuits provide eight separate R-S latches in the popular 16-pin package. While in the high-impedance state, the inputs and outputs are disabled and no information can be entered. When both WRITE inputs are brought to a low logic level, the outputs are disabled and new information may be entered at the inputs. When a low logic level is applied to both READ inputs, and a high logic level to both WRITE in-

puts, the inputs are rendered inactive and data may be read from the outputs.

Features

- TRI-STATE I/O pins
- 8 latches in popular 16-pin package
- Typical propagation delay—22 ns

Connection Diagram



7553 (J,W); 8553 (N)

Truth Table

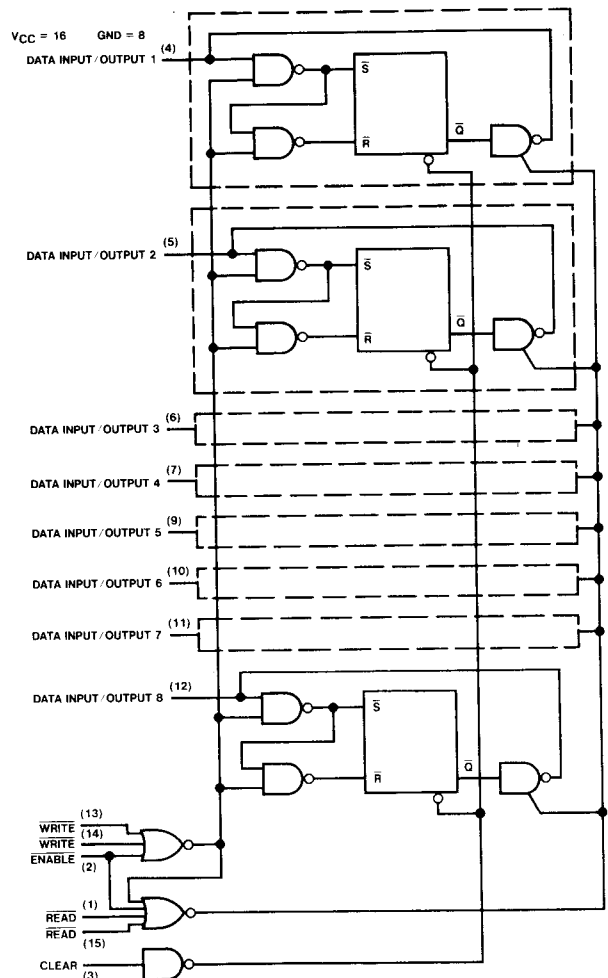
Clear	Enable	Read'	Write**	Operation	State of Bus
H	L	L	H	Enter L	L
H	L	L	L	Enter L	Hi-Z
L	X	H	H	Do Nothing	Hi-Z
L	H	X	X	Do Nothing	Hi-Z
L	L	X	L	Write	H or L ***
L	L	L	H	Read	H or L ***

*Both Read Inputs

**Both Write Inputs

***Depends on State of Latch

Logic Diagram





Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Conditions	DM75			DM85			Units
			53			53			
			Min	Typ (1)	Max	Min	Typ (1)	Max	
V _{IH}	High Level Input Voltage		2			2		V	
V _{IL}	Low Level Input Voltage				0.8		0.8	V	
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -12 mA			-1.5		-1.5	V	
I _{OH}	High Level Output Current				-2.0		-5.2	mA	
V _{OH}	High Level Output Voltage	V _{CC} = Min, V _{IH} = 2 V V _{IL} = 0.8 V, I _{OH} = Max	2.4			2.4		V	
I _{OL}	Low Level Output Current				16		16	mA	
V _{OL}	Low Level Output Voltage	V _{CC} = Min, V _{IH} = 2 V V _{IL} = 0.8 V, I _{OL} = 16 mA			0.4		0.4	V	
I _{O(OFF)}	Off State (High Impedance State) Output Current	V _{CC} = Max, V _{IH} = 2 V V _{IL} = 0.8 V		V _O = 0.4 V V _O = 2.4 V	-40 40		-40 40	μA	
I _I	Input Current at Maximum Input Voltage	V _{CC} = Max, V _I = 5.5 V			1		1	mA	
I _{IH}	High Level Input Current	V _{CC} = Max, V _I = 2.4 V			40		40	μA	
I _{IL}	Low Level Input Current	V _{CC} = Max, V _I = 0.4 V			-1.6		-1.6	mA	
I _{OS}	Short Circuit Output Current	V _{CC} = Max (2)	-28		-70	-28	-70	mA	
I _{CC}	Supply Current	V _{CC} = Max		66	93		66	93	mA

Note 1: All typical values are at V_{CC} = 5 V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

Parameter		From (Input)	To (Output)	Conditions	DM75/85			Units
					53			
					Min	Typ	Max	
t _{PHL}	Propagation Delay Time, High-to-Low-Level Output	Clear	Output	C _L = 50 pF, R _L = 400 Ω		21	32	ns
t _{ZH}	Output Enable Time to High Level	Enable	Output			22	33	ns
t _{ZL}	Output Enable Time to Low Level	Enable	Output			25	38	ns
t _{HZ}	Output Disable Time from High Level	Enable	Output	C _L = 5 pF, R _L = 400 Ω		7	12	ns
t _{LZ}	Output Disable Time from Low Level	Enable	Output			20	30	ns
t _w	Minimum Pulse Width	Clear			15	10		ns
		Write			40	28		
t _{SETUP}	Minimum Data Setup Time	High Level			20	14		ns
		Low Level			36	26		
t _{HOLD}	Minimum Data Hold Time	High Level			-15	-26		ns
		Low Level			-8	-14		