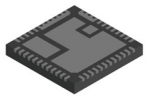
Single-Phase Voltage Regulator with SVID Interface for Computing Applications

NCP81568



QFN48
CASE 483BT

The NCP81568 is a high−performance, low−bias current, single−phase single rail regulator with integrated power MOSFETs intended to support a wide range of computing applications. The device is able to deliver up to 20.25A TDC, 40A ICCMAX output current on an adjustable output with SVID interface. Operating in high switching frequency allows employing small size inductor and capacitors. The controller makes use of **onsemi**'s patented high performance RPM operation. RPM control maximizes transient response while allowing for smooth transitions between discontinuous−frequency−scaling operation and continuous−mode full−power operation. The NCP81568 has an ultra−low offset current monitor amplifier with programmable offset compensation for high−accuracy current monitoring.

Features

- High Performance RPM Control System
- Intel IMVP9.2 Protocol
- Ultra Low Offset IOUT Monitor with DCR Sense
- Differential Remote Output Voltage Sensing
- Soft Transient Control Reduces Inrush Current and Audio Noise
- Dynamic VID Feed−Forward
- Externally Programmable Droop Gain
- Input Supply Voltage Feed−Forward Control
- Built−in Over−voltage, Under−voltage and Pin Programmable Over−Current Protection
- Zero Droop Capable
- Ultrasonic Operation
- Programmable Operating Frequency
- QFN48, 6 mm × 6 mm, 0.4 mm Pitch Package
- This is a Pb−Free Device

Applications

- Desktop, Notebook and Ultra−book Computers

MARKING DIAGRAM

NCP81568	= Specific Device Code
A	= Assembly Location
WL	= Lot ID
YY	= Year
WW	= Work Week
G	= Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCP81568MNTXG	QFN48 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NCP81568 BLOCK DIAGRAM

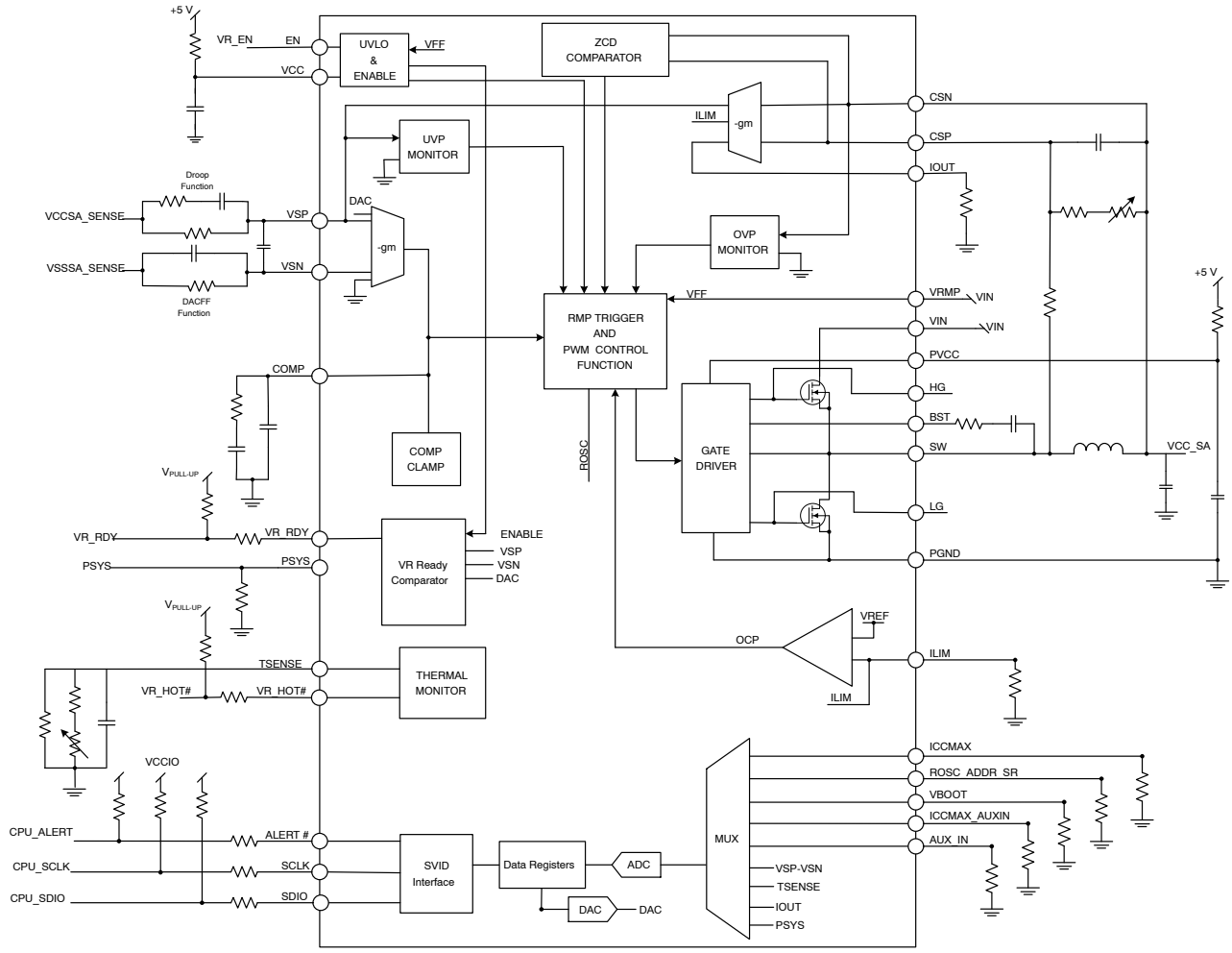


Figure 1. Block Diagram

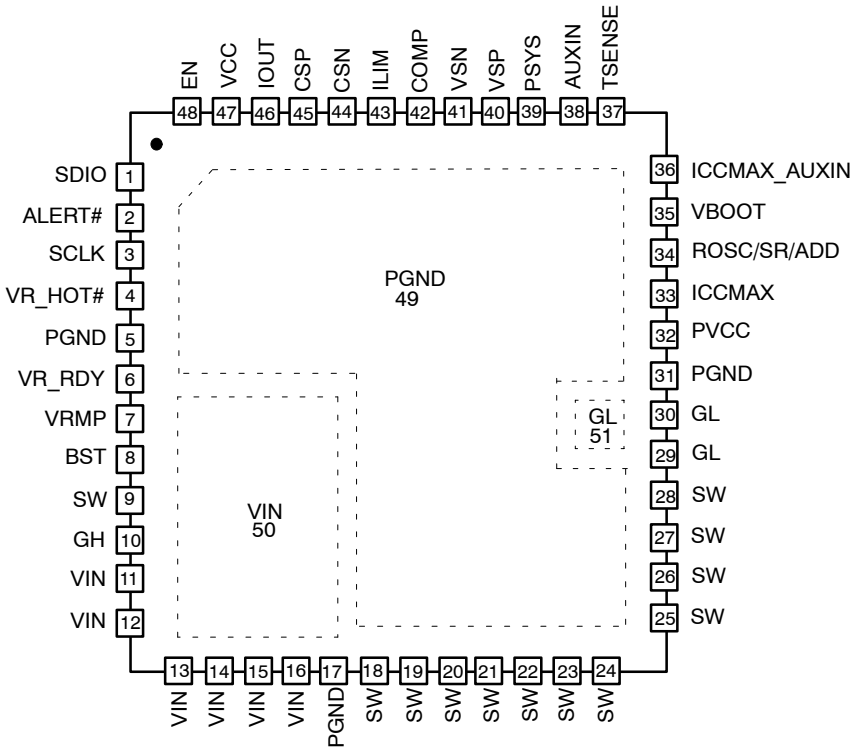


Figure 2. Pin−out (Top View)

Table 1. PIN FUNCTION DESCRIPTIONS

Pin No.	Symbol	Description
1	SDIO	Serial VID Data Interface
2	ALERT#	Serial VID ALERT#
3	SCLK	Serial VID Clock
4	VR_HOT#	Thermal Logic Output for Over−Temperature Condition on TSENSE
5	PGND	Power Ground. Power Supply Ground Pins, Connected to Source of Internal LS FET and Internal Control Circuits.
6	VR_RDY	VR_RDY Indicates the Controller is Ready to Accept SVID Commands
7	VRMP	Feed−forward input of Vin for the ramp−slope compensation. The voltage fed into this pin is used to control the ramp of the PWM slopes.
8	BST	Provides Bootstrap Voltage for the HS Gate Driver. A Cap is Required from this Pin to SW
9	SW	Switching Node. Provides a Return Path for the Integrated HS Driver
10	GH	Gate of HS FET
11	VIN	Input Voltage for HS FET Drain. 22 μF or More Ceramic Caps must Bypass this Input to Power Ground. Place Close to Pins
12	VIN	Input Voltage for HS FET Drain. 22 μF or More Ceramic Caps must Bypass this Input to Power Ground. Place Close to Pins
13	VIN	Input Voltage for HS FET Drain. 22 μF or More Ceramic Caps must Bypass this Input to Power Ground. Place Close to Pins
14	VIN	Input Voltage for HS FET Drain. 22 μF or More Ceramic Caps must Bypass this Input to Power Ground. Place Close to Pins
15	VIN	Input Voltage for HS FET Drain. 22 μF or More Ceramic Caps must Bypass this Input to Power Ground. Place Close to Pins
16	VIN	Input Voltage for HS FET Drain. 22 μF or More Ceramic Caps must Bypass this Input to Power Ground. Place Close to Pins
17	PGND	Power Ground. Power Supply Ground Pins, Connected to Source of Internal LS FET and Internal Control Circuits.

Table 1. PIN FUNCTION DESCRIPTIONS (continued)

Pin No.	Symbol	Description
18	SW	Switch Node. Pins to be Connected to an External Inductor. These Pins are Interconnection between Internal HS and LS FETs
19	SW	Switch Node. Pins to be Connected to an External Inductor. These Pins are Interconnection between Internal HS and LS FETs
20	SW	Switch Node. Pins to be Connected to an External Inductor. These Pins are Interconnection between Internal HS and LS FETs
21	SW	Switch Node. Pins to be Connected to an External Inductor. These Pins are Interconnection between Internal HS and LS FETs
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26	SW	Switch Node. Pins to be Connected to an External Inductor. These Pins are Interconnection between Internal HS and LS FETs
27	SW	Switch Node. Pins to be Connected to an External Inductor. These Pins are Interconnection between Internal HS and LS FETs
28	SW	Switch Node. Pins to be Connected to an External Inductor. These Pins are Interconnection between Internal HS and LS FETs
29	GL	Gate of LS FET
30	GL	Gate of LS FET
31	PGND	Power Ground. Power Supply Ground Pins, Connected to Source of Internal LS FET and Internal Control Circuits.
32	PVCC	Power Supply input pin of internal gate driver. A 4.7 μF or large ceramic capacitor bypasses this input to ground. This capacitor should be placed as close as possible to the pin.
33	ICCMAX	ICCMAX Register Program
34	ROSC/SR/ADD	Programming for F_{SW}, Slew Rate, and SVID Address. A Resistor to GND Programs these Values during Start−up, per Look−up Table
35	VBOOT	Programming for V_{BOOT}. A Resistor to GND Programs this value during Start−up, per Look−up Table
36	ICCMAX_AUXIN	ICCMAX_AUXIN Register Program
37	TSENSE	External Temperature Sense Network is Connected to this Pin
38	AUXIN	AUX IMON Input
39	PSYS	System Power Signal Input. A Resistor to Ground Scales this Signal
40	VSP	Differential Output Voltage Sense Positive
41	VSN	Differential Output Voltage Sense Negative
42	COMP	Compensation
43	ILIM	Current−Limit Program
44	CSN	Differential Current Sense Negative
45	CSP	Differential Current Sense Positive
46	IOUT	IOUT Gain Program
47	VCC	Power Supply Input Pin of Control Circuits. A 1 μF or Larger Ceramic Capacitor Bypasses this Input to Ground, Placed Close to the Controller
48	EN	Enable
49	PGND	Flag. Power Ground. Power Supply Ground Pins, Connected to Source of Internal LS FET and Internal Control Circuits.
50	VIN	Flag. Input Voltage for HS FET Drain. 22 μF or More Ceramic Caps must Bypass this Input to Power Ground. Place Close to Pins
51	GL	Flag. Gate of LS FET

Table 2. ABSOLUTE MAXIMUM RATINGS (Note 1)

Rating	Symbol	Min	Max	Unit
Power Supply	V_{VIN}	–	30	V
Analog Supply Voltage	V_{CC}, PV_{CC}	−0.3	6.0	V
Switch Node (Pin 9)	V_{SW}	−0.5	30	V
		−7 V (<5 ns)	33 V (<40 ns)	
Switch Node (Pins 18−28)	V_{SW}	−0.5	30	V
		−7 V (<5 ns)	33 V (<40 ns)	
BST	BST_PGND	−0.3	33	V
		−2 V (<200 ns)		
BST to SW (Pin 9)	BST_SW	−0.3	6.5	V
			7 V (<100 ns)	
GH to SW (Pin 9)	GH	−0.3	BST + 0.3	V
		−2 (< 200 ns)		
GL	GL	−0.3	PV_{CC} + 0.3	V
		−2 (< 200 ns)		
PGND	PGND	−0.3	0.3	V
VSN	VSN	−0.3	0.3	V
SVID	SCLK, SDIO	−0.3	3.6	V
All Other Pins		−0.3	V_{CC} + 0.3	V
Latch Up Current: All Pins, Except Digital Pins Digital Pins	I_{LU}	 −200 −10	 200 10	mA
Peak Output Current (F_{SW} = 600 kHz, V_{IN} = 20 V, V_{OUT} = 1.0 V, Duration = 10 ms, Period = 1s, T_A = 25°C)	I_O	–	50	A
Unclamped Inductive Switching Single−Pulse Avalanche Energy, Highside FET (T_J = 25°C, V_{CC}/V_{GS} = 5 V, L = 3 μH, I_L = 95 APK)	UIS	–	16.24	mJ

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All signals referenced to PGND unless noted otherwise.

Table 3. ESD CAPABILITY

Description	Symbol	Typ	Unit
ESD Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Charged Device Model (Note 2)	ESD_{CDM}	1000	V

2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per JS−001−2017
   ESD Charged Device Model tested per JS−002−2018
   Latch Up Current tested per JESD78.

Table 4. RECOMMENDED OPERATING RANGES

Parameter	Symbol	Min	Max	Unit
VCC Voltage Range	VCC	4.75	5.25	V
Operating Junction Temperature Range (Note 3)	T_J	−40	125	°C
Operating Ambient Temperature Range	T_A	−40	100	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. JEDEC JESD 51−7 with 0 LFM

Table 5. THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Storage Temperature Range	T_{STG}	−40 to +150	°C
Thermal Resistance Junction to Board (Note 4)	$R_{\theta JB}$	5.01	°C/W
Thermal Resistance Junction to Ambient (Note 4)	$R_{\theta JA}$	20.55	°C/W
Power Dissipation at T_A = 25°C (Note 5)	P_D	5.3	W
Moisture Sensitivity Level (Note 6)	MSL	1	–

4. The thermal resistance values are dependent on the internal losses split between devices and the PCB heat dissipation. This data is based on a typical operation condition with a 4−layer FR−4 PCB board, which as two, 1−ounce copper internal power and ground planes and 2−ounce copper traces on top and bottom layers with approximately 80% copper coverage. No airflow and no heat sink applied (reference EIA/JEDEC 51−7). It also does not account for other heat sources that may be present on the PCB next to the device in question (such as inductors, resistors, etc.)
5. The maximum power dissipation (PD) is dependent on input voltage, output voltage, output current, external components selected, and PCB layout. The reference data is obtained based on T_{JMAX} = 125°C and $R_{\theta JA}$ = 20.55°C/W.
6. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC Standard: J−STD−020D.1.

Table 6. ELECTRICAL CHARACTERISTICS (Unless otherwise stated: −40°C < T_A < 100°C; 4.75 V < VCC < 5.25 V; C_{VCC} = 0.1 μF)

Parameter	Test Conditions	Min	Typ	Max	Unit
BIAS SUPPLY					
VCC Quiescent Current	PS0 / PS1	–	–	12.5	mA
	PS2 / PS3	–	–	12	mA
	PS4	–	45	–	μA
	EN = High (No Switching)	–	9.7	–	mA
	EN = Low	–	–	43	μA
VCC UVLO Threshold	VCC Rising	–	–	4.6	V
	VCC Falling	4.1	–	–	V
VCC UVLO Hysteresis		–	100	–	mV
VIN UVLO Threshold	VIN Rising	–	–	4.25	V
	VIN Falling	3	–	–	V
VIN UVLO Hysteresis		–	830	–	mV
ENABLE INPUT					
Upper Threshold	V_{UPPER}	0.8	–	–	V
Lower Threshold	V_{LOWER}	–	–	0.3	V
Enable Hysteresis		200	300	–	mV
Enable Delay Time	Measure Time from Enable Transitioning HI to VR_RDY High	–	–	2.5	ms
DAC SLEW RATE					
Soft Start Slew Rate		–	1/2 SR Fast	–	mV/μs
Slew Rate Slow		–	1/2 SR Fast	–	mV/μs
Slew Rate Fast	Resistor Selectable (Table 7)	>10	–	–	mV/μs
ADC					
Voltage Range		0	–	2.5	V
Total Unadjusted Error (TUE)		−1	–	+1	%
Differential Non-Linearity (DNL)	8-Bit	–	–	1	LSB
Power Supply Sensitivity		−1	–	+1	%
Conversion Time		–	7.4	10	μs
Round Robin		100	–	–	μs

Table 6. ELECTRICAL CHARACTERISTICS (Unless otherwise stated: −40°C < T_A < 100°C; 4.75 V < VCC < 5.25 V; C_{VCC} = 0.1 μF)

Parameter	Test Conditions	Min	Typ	Max	Unit
IMVP9.2 DAC					
System Voltage Accuracy	0.75 V ≤ DAC < 1.52 V (at 25°C only)	−0.5	–	0.5	%
	0.5 V< DAC < 0.745 V (at 25°C only)	−8	–	8	mV
	0.25 V < DAC < 0.495 V (at 25°C only)	−10	–	10	mV
PSYS					
Full Scale Input Voltage		–	2.5	–	V
Disable Threshold		–	VCC −0.2	–	V
TSENSE					
Alert# Assert Threshold		–	556	–	mV
Alert# De-Assert Threshold		–	595	–	mV
VRHOT Assert Threshold		–	517	–	mV
VRHOT Rising Threshold		–	556	–	mV
TSENSE Bias Current		115.5	120	125.5	μA
VR_RDY_OUTPUT					
Output Low Saturation Voltage	I_{VR_RDY} = 4 mA	–	0.1	0.3	V
Rise Time	External Pull-Up of 1 kΩ to 3.3 V, C_{TOT} = 45 pF, ΔVo = 10% to 90%	–	110	–	ns
Fall Time	External Pull-Up of 1 kΩ to 3.3 V, C_{TOT} = 45 pF, ΔVo = 90% to 10%	–	20	–	ns
Output Voltage High		0.8	–	3.3	V
DIFFERENTIAL VOLTAGE SENSE AMPLIFIER					
Input Bias Current		−1	–	1	μA
VSP Input Voltage Range		–	–	3.04	V
VSN Input Voltage Range		0	–	0.3	V
gm	VSP = 1.2 V	1.33	1.6	2	mS
Open loop Gain	Load = 1 nF in Series with 1 kΩ in Parallel with 10 pF to Ground	–	73	–	dB
−3dB Bandwidth	Load = 1 nF in Series with 1 kΩ in Parallel with 10 pF to Ground	–	15	–	MHz
Sink and Source Current	Input Differential −200 mV & +200 mV	–	280		μA
IOUT					
Analog Gain Accuracy	0 V < CSP − CSN < 20 mV	−4	–	4	%
gm		7.68	8.0	8.32	mS
IOUT Output Accuracy		−1.12	–	1.12	μA
OUTPUT OVER VOLTAGE & UNDER VOLTAGE PROTECTION (OVP & UVP)					
Relative Over Voltage Threshold	CSN−VID Setting	360	400	440	mV
Absolute Over Voltage Threshold (10 mV DAC Step)	CSN−GND	3.3	3.44	3.6	V
Absolute Over Voltage Threshold (5 mV DAC Step)	CSN−GND	2.4	2.5	2.6	V
Over Voltage Delay	CSN Rising to GL High	–	300	–	ns
Under Voltage Threshold	VSP−VSN Falling	180	260	400	mV
Under-Voltage Hysteresis	VSP−VSN Falling/Rising	–	25	–	mV
Under-Voltage Blanking Delay	VSP−VSN Falling to VR_RDY Falling	–	5	–	μs
DROOP					
gm		0.96	1.0	1.04	mS
Offset Accuracy		−1	–	1	μA

Table 6. ELECTRICAL CHARACTERISTICS (Unless otherwise stated: −40°C < T_A < 100°C; 4.75 V < VCC < 5.25 V; C_{VCC} = 0.1 μF)

Parameter	Test Conditions	Min	Typ	Max	Unit
DROOP					
Common Mode Rejection	CSP Input at 1.1 V, 1.65 V to 1.8 V	60	80	–	dB
OVERCURRENT PROTECTION					
ILIMIT Threshold		1.275	1.3	1.325	V
ILIMIT Delay		–	280	–	ns
ILIMIT Gain	I_{ILIMIT}/(CSP−CSN), CSP−CSN = 20 mV	–	1.0	–	mS
SWN ZCD COMPARATOR					
Offset Accuracy		−1.5	–	1.5	mV
HIGH-SIDE MOSFET					
Drain-to-Source On Resistance	V_{GS} = 5 V, I_D = 30 A, R_{ON_H}	–	8	–	mΩ
LOW-SIDE MOSFET					
Drain-to-Source On Resistance	V_{GS} = 5 V, I_D = 30 A, R_{ON_L}	–	2	–	mΩ
HIGH-SIDE GATE DRIVE					
Pull-High Drive On Resistance	$V_{BST} - V_{SW}$ = 5 V, R_{DRV_HH}	–	1.2	2.5	Ω
Pull-Low Drive On Resistance	$V_{BST} - V_{SW}$ = 5 V, R_{DRV_HL}	–	0.8	2.0	Ω
GH Propagation Delay Time	From GL Falling to GH Rising, T_{GH_d}	–	23	35	ns
GH Rise Time	TGH_R	–	9	20	ns
GH Fall Time	TGH_F	–	9	20	ns
GH Pull-Down Resistance	$V_{BST} - V_{SW}$ = 0 V	–	292	–	kΩ
LOW-SIDE GATE DRIVE					
Pull-High Drive On Resistance	$V_{CCP} - V_{PGND}$ = 5 V, R_{DRV_LH}	–	0.9	2.5	Ω
Pull-Low Drive On Resistance	$V_{CCP} - V_{PGND}$ = 5 V, R_{DRV_LL}	–	0.4	1.4	Ω
GL Propagation Delay Time	From GH Falling to GL Rising, T_{GL_d}	–	11	35	ns
GL Rise Time	TGL_R	–	9	20	ns
GL Fall Time	TGL_F	–	11	20	ns
SW					
SW Minimum Pulse Width (Note 7)		–	60	–	ns
SW TO PGND RESISTANCE					
SW to PGND Pull−Down Resistance	R_{SW}	–	2	–	kΩ
BOOTSTRAP RECTIFIER SWITCH					
Output Low Resistance	EN = L or EN = H and DRVL = H, R_{on_BST}	5	13	21	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Guaranteed by design, not tested in production.

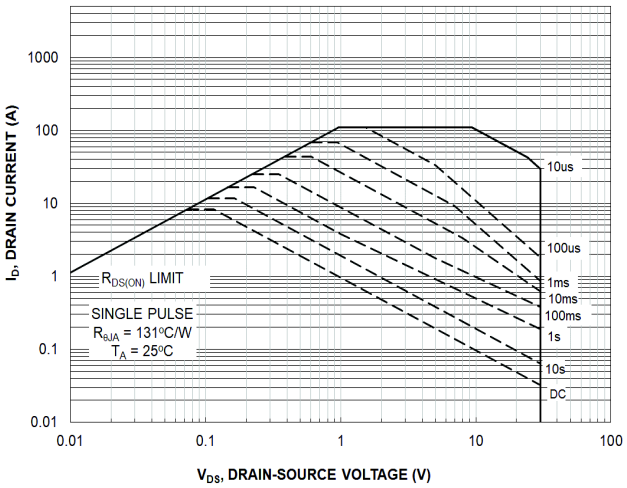


Figure 3. Highside FET Forward Biased Safe Operating Area

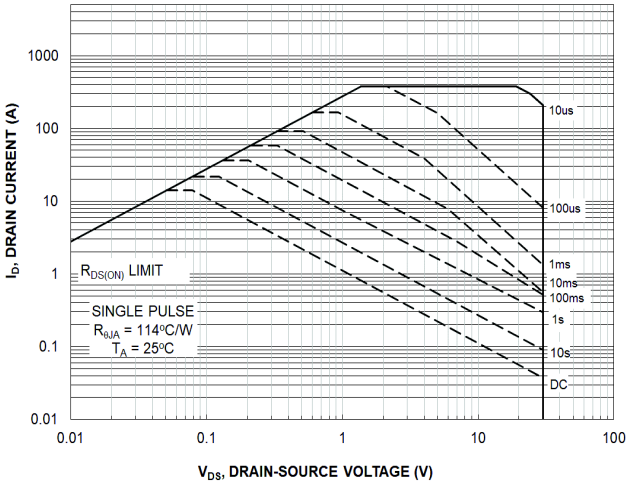
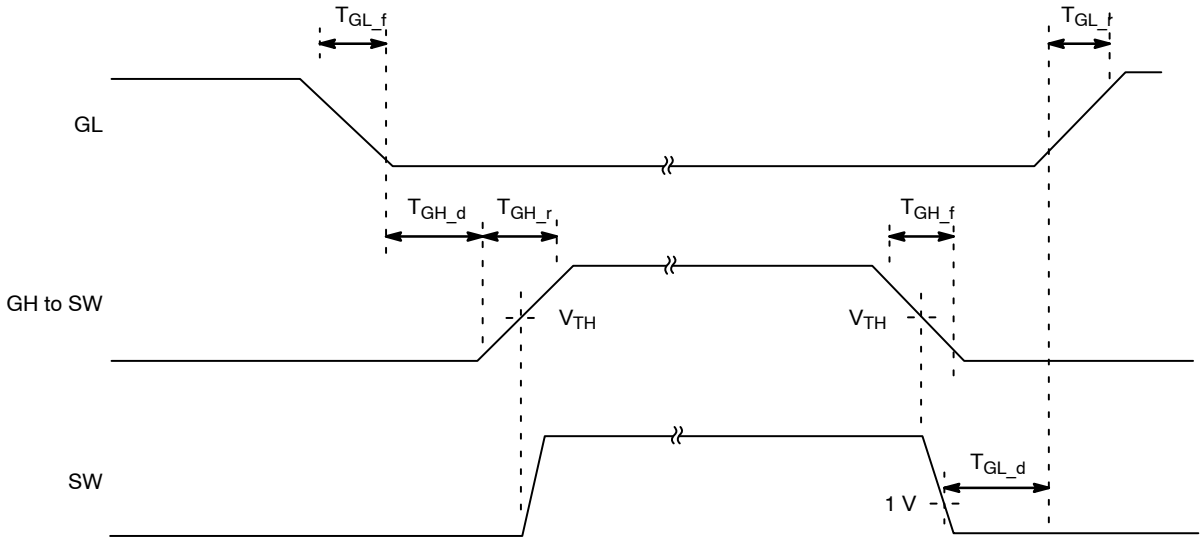


Figure 4. Lowside FET Forward Biased Safe Operating Area



NOTE: Timing is referenced to the 10% and the 90% points, unless otherwise stated.

Figure 5. Driver Timing Diagram

DEVICE CONFIGURATION

The NCP81568 is a single phase IMVP9.2 SVID controller with a built−in gate driver and integrated power MOSFETs. The controller makes use of a digitally enhanced high−performance current mode RPM control method that provides excellent transient response while minimizing transient aliasing. The average operating frequency is digitally stabilized to remove frequency drift under all continuous mode operating conditions.

Basic Configuration

The controller has five basic configuration features. On power up, a 10 μA current is sourced from these pins through a resistor connected to this pin and the resulting voltage is measured. These values are programmed on power up and cannot be changed after the initial power up sequence is complete. The following features will be programmed.

- Switching Frequency
- SVID Address
- Slew Rate
- VBOOT
- Output Voltage Step

Table 7. SWITCHING FREQUENCY, SLEW RATE AND SVID ADDRESS

Resistor (kΩ)	Switching Frequency (kΩ)	Slew Rate (mV/μs)	SVID Address
10	500	10	1
14	600		
18.2	700		
22.6	500	30	
27.4	600		
33.2	700		
40.2	500	48	
48.7	600		
57.6	700		
68.1	500	10	2
80.6	600		
95.3	700		
113	500	30	
133	600		
158	700		
187	500	48	
221	600		
280	700		

Table 8. VBOOT, OUTPUT VOLTAGE STEP AND INTEL PROPRIETARY CURRENT PROTECTION FEATURE

Resistor (kΩ)	V_{BOOT} (V)	Output Voltage Step	Intel Proprietary Current Protection Feature
10	0	5 mV/step	ON
14	1.05		
18.2	0	10 mV/step	
22.6	1.8		
27.4	0	5 mV/step	OFF
33.2	1.05		
40.2	0	10 mV/step	
48.7	1.8		
57.6	0.5	5 mV/step	OFF
68.1	0.5	10 mV/step	

Ultrasonic Mode

The switching frequency of a rail in DCM will decrease at very light loads. Ultrasonic Mode forces the switching frequency to stay above the audible range.

Remote Sense Error Amplifier

A high performance, high input impedance, true differential transconductance amplifier is provided to accurately sense the regulator output voltage and provide high bandwidth transient performance. The VSP and VSN inputs should be connected to the regulator's output voltage sense points through filter networks describe in the Droop Compensation and DAC Feed−Forward Compensation sections. The remote sense error amplifier outputs a current proportional to the difference between the output voltage and the DAC voltage:

$$I_{COMP} = gm \cdot \left(V_{DAC} - \left(V_{VSP} - V_{VSN}\right)\right) \quad \text{(eq. 1)}$$

This current is applied to a standard Type II compensation network.

Single−Phase Rail Voltage Compensation

The Remote Sense Amplifier outputs a current that is applied to a Type II compensation network formed by external tuning components CLF, RZ and CHF.

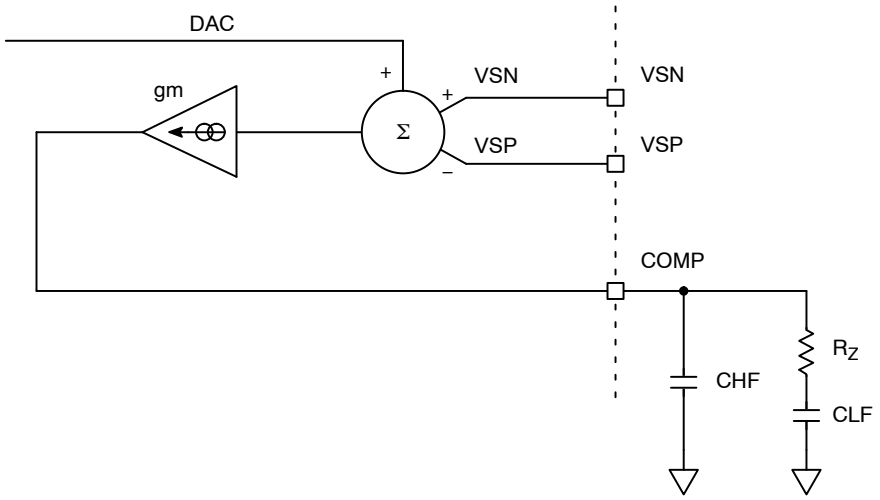


Figure 6. Rail Voltage Compensation

Differential Current Feedback Amplifier

The NCP81568 controller has a low offset, differential amplifier to sense output inductor current. An external low−pass filter can be used to superimpose a reconstruction of the AC inductor current onto the DC current signal sensed across the inductor. The low−pass filter time constant should match the inductor L/DCR time constant by setting the filter pole frequency equal to the zero of the output inductor. This makes the filter AC output mimic the product of AC inductor current and DCR, with the same gain as the filter DC output. It is best to perform fine tuning of the filter pole during transient testing.

$$F_Z = \frac{DCR\ @\ 25°C}{2 \cdot \pi \cdot L} \quad \text{(eq. 2)}$$

$$F_P = \frac{1}{2 \cdot \pi \cdot \left(\frac{R_{PHSP} \cdot (R_{TH} + R_{CSSP})}{R_{PHSP} + R_{TH} + R_{CSSP}}\right) \cdot C_{CSSP}} \quad \text{(eq. 3)}$$

Forming the low−pass filter with an NTC thermistor (R_{TH}) placed near the output inductor, compensates both the DC gain and the filter time constant for the inductor DCR change with temperature. The values of R_{PHSP} and R_{CSSP} are set based on the effect of temperature on both the thermistor and inductor. The CSP and CSN pins are high impedance inputs, but it is recommended that the low−pass filter resistance not exceed 10 k in order to avoid offset due to leakage current. It is also recommended that the voltage sense element (inductor DCR) be no less than 0.5 m for sufficient current accuracy. Recommended values for the external filter components are:

R_{PHSP} = 7.68 kΩ, R_{CSSP} = 14.3 kΩ

R_{TH} = 100 kΩ, Beta = 4300

$$C_{CSSP} = \frac{L_{PHASE}}{\frac{R_{PHSP} \cdot (R_{TH} + R_{CSSP})}{R_{PHSP} + R_{TH} + R_{CSSP}} \cdot DCR} \quad \text{(eq. 4)}$$

Using 2 parallel capacitors in the low−pass filter allows fine tuning of the pole frequency using commonly available capacitor values.

The DC gain equation for the current sense amplifier output is:

$$V_{CURR} = \frac{R_{TH} + R_{CSSP}}{R_{PHSP} + R_{TH} + R_{CSSP}} \cdot I_{OUT} \cdot DCR \quad \text{(eq. 5)}$$

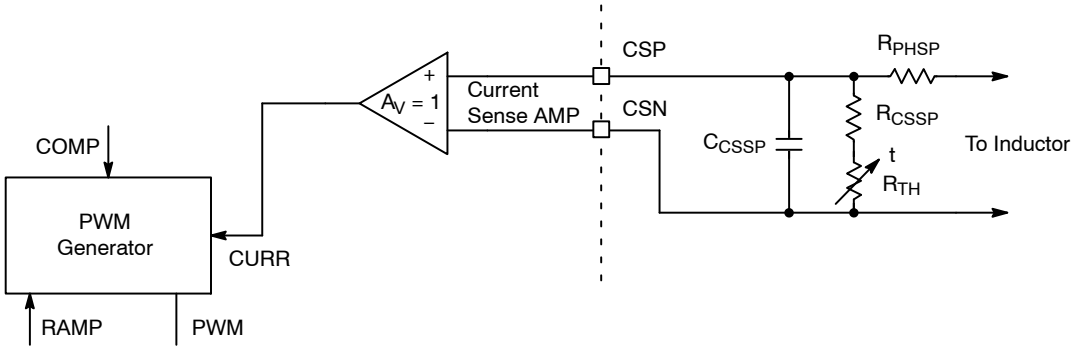


Figure 7. Differential Current Feedback Amplifier

The amplifier output signal is combined with the COMP and RAMP signals at the PWM comparator inputs to produce the Ramp Pulse Modulation (RPM) PWM signal.

Load−Line Programming (DROOP)

An output load−line is a power supply characteristic wherein the regulated (DC) output voltage decreases by a voltage V_{DROOP}, proportional to load current. This characteristic can reduce the output capacitance required to maintain output voltage within limits during load transients faster than those to which the regulation loop can respond.

In the NCP81568, a load−line is produced by adding a signal proportional to output load current (V_{DROOP}) to the output voltage feedback signal – thereby satisfying the voltage regulator at an output voltage reduced proportional to load current. V_{DROOP} is developed across a resistance between the VSP pin and the output voltage sense point.

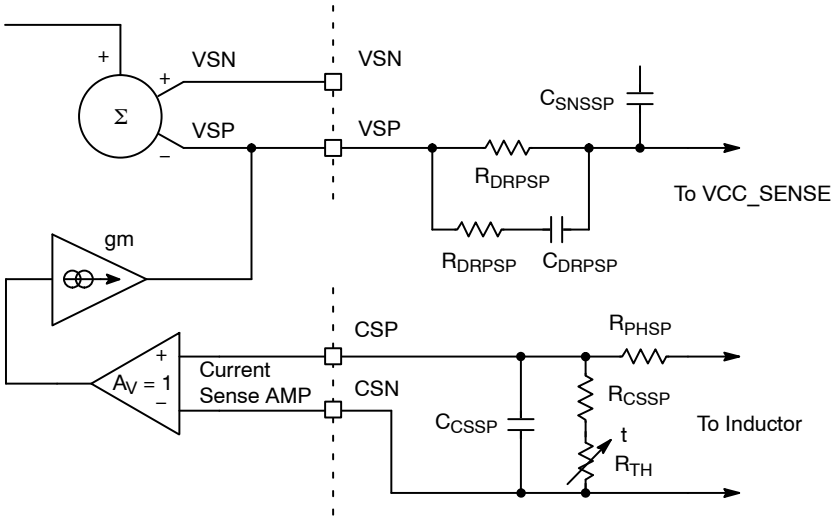


Figure 8. Load−Line Programming

$$V_{DROOP} = R_{DRPSP} \cdot gm \cdot \frac{R_{TH} + R_{CSSP}}{R_{PHSP} + R_{TH} + R_{CSSP}} \cdot I_{OUT} \cdot DCR \quad \text{(eq. 6)}$$

The load−line is programmed by choosing R_{DRPSP} such that the ratio of voltage produced across R_{DRPSP} to output current is equal to the desired load−line.

$$R_{DRPSP} = \frac{Loadline}{gm \cdot DCR} \cdot \frac{R_{PHSP} + R_{TH} + R_{CSSP}}{R_{TH} + R_{CSSP}} \quad \text{(eq. 7)}$$

Programming the DAC Feed−Forward Filter

The NCP81568 outputs a pulse of current from the VSN pin upon each increment of the internal DAC following a DVID UP command. A parallel RC network inserted into the path from VSN to the output voltage return sense point, VSS_SENSE, causes these current pulses to temporarily decrease the voltage between VSP and VSN. This causes the output voltage during DVID to be regulated slightly higher, in order to compensate for the response of the Droop function to the inductor current flowing into the charging output capacitors. RFFSP sets the gain of the DAC feed−forward and CFFSP provides the time constant to cancel the time constant of the system per the following equations. C_{OUT} is the total output capacitance of the system.

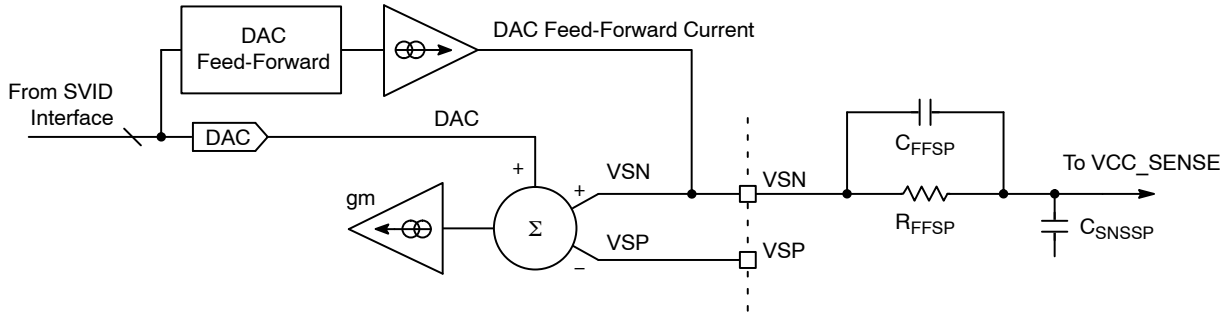


Figure 9. DAC Feed−Forward Filter Programming

$$R_{FFSP} = \frac{\text{Loadline} \cdot C_{OUT}}{1.35 \cdot 10^{-9}} \ (\Omega) \qquad C_{FFSP} = \frac{200}{R_{FFSP}} \ (\text{nF}) \qquad \text{(eq. 8)}$$

Programming ICCMAX

The SVID interface provides the platform ICC_MAX value at register 21 h. A resistor to ground on the ICCMAX pin programs this register at the time the part is enabled. 10 μA is sourced from these pins to generate a voltage on the program resistor. The value of the register is 1 A per LSB and is set by the equation below. The resistor value should be no less than 10 kΩ. This needs to be programmed both for the SA and the AUXIN rails.

$$ICC\_MAX_{21h} = \frac{R \cdot 10\ \mu A \cdot 255\ A}{2.5\ V} \qquad \text{(eq. 9)}$$

Programming IOUT

The IOUT pin sources a current in proportion to the ILIMIT sink current. The voltage on the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to ICCMAX generates a 2.5 V signal on IOUT. The gm of the IOUT amplifier is 8.

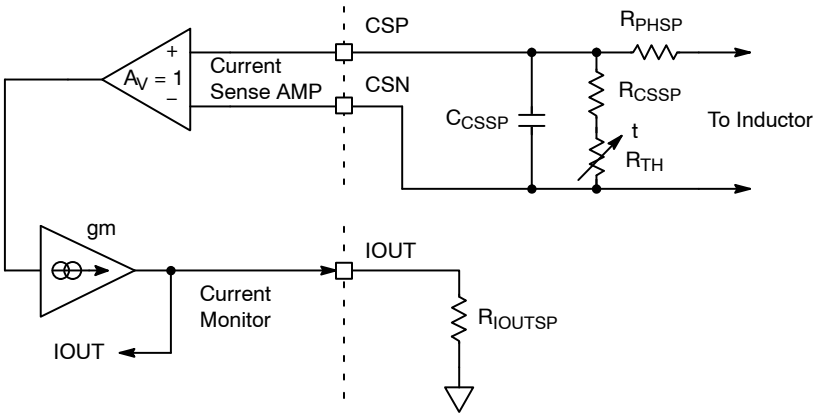


Figure 10. IOUT Programming

$$R_{IOUTSP} = \frac{2.5\ V}{gm \cdot \frac{R_{th} + R_{CSSP}}{R_{PHSP} + R_{th} + R_{CSSP}} \cdot ICCMAX \cdot DCR} \qquad \text{(eq. 10)}$$

Programming the Current Limit

The current limit threshold is programmed with a resistor (R_{ILIMSP}) from the ILIM pin to ground. The current limit latches the single−phase rail off immediately if the ILIM pin voltage exceeds the ILIM Threshold. Set the value of the current limit resistor based on the equation shown below. A capacitor can be placed in parallel with the programming resistor to slightly delay activation of the latch if some tolerance of short over−current events is desired.

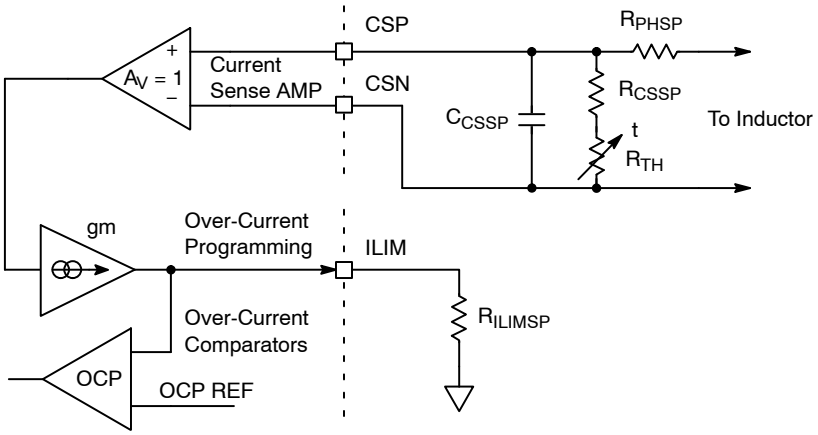


Figure 11. Current Limit Programming

$$R_{ILIMSP} = \frac{1.3\ V}{gm \cdot \frac{R_{TH} + R_{CSSP}}{R_{PHSP} + R_{TH} + R_{CSSP}} \cdot I_{OUT_{LIMIT}} \cdot DCR} \quad \text{(eq. 11)}$$

PSYS

The PSYS pin is an analog input to the VR controller. PSYS is a system input power monitor that facilitates the monitoring of the total platform system power. A 20 kΩ pull down resistor must be used for scaling of the PSYS information.

To disable the PSYS function, the pin should be pulled to 5 V through a resistor.

TSENSE Network

A temperature sense input is provided. A precision current is sourced out the TSENSE pin to generate voltage on the temperature sense network. The voltage on the temperature sense input is sampled by the internal A/D converter. A 100k NTC similar to the Murata NCP15WF104E03RC should be used. RCOMP1 in the following Figure 12 is optional and can be used to slightly change the hysteresis. See the specification table for the thermal sensing voltage thresholds and source current.

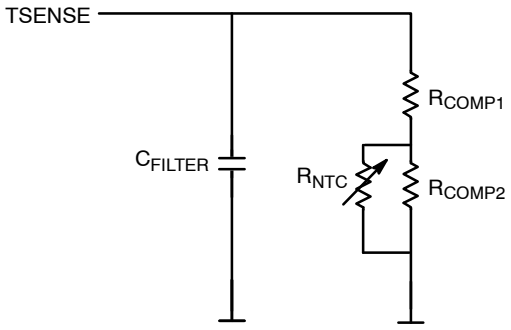


Figure 12. Tsense Network

Over−Current Protection (OCP)

The current limit is set with a resistor between the ILIM pin and ground. The voltage on this pin is compared to the ILIM threshold voltage (V_{CL}). If the ILIM pin voltage exceeds the lower Threshold Voltage, an internal latch−off timer starts. When the timer expires, the controller shuts down if the fault is not removed. If the voltage at the ILIM pin exceeds the higher Threshold Voltage, the controller shuts down immediately. To recover from an OCP fault, the EN pin or V_{CC} voltage must be cycled low.

Under−Voltage Protection

Under−voltage protection will shut off the output similar to OCP to protect against short circuits. The threshold is specified in the parametric spec tables and is not adjustable.

Input Under−Voltage Protection

The controller is protected against under−voltage on the VCC, PVCC, and VRMP pins.

Over−Voltage Protection (OVP)

When operating in CCM mode, the NCP81568 has a relative OVP feature on VCC, PVCC and VRMP pins that generates an OVP fault when the voltage on the CSN pin (VCSN) rises 400 mV above the programmed output voltage. The NCP81568 has an absolute OVP feature which generates an OVP fault when the voltage on the CSN pin (VCSN) exceeds 2.5 V.

When an OVP fault occurs, the HG driver is turned off and the LG driver is turned on to discharge the output. The internal output voltage control DAC also begins to ramp down at a rate of 1.6 mv/s. The LG driver turns off when VCSN drops below the dac voltage and continues to pulse on so that VOUT tracks the internal DAC voltage down to 0 V. To exit an OVP fault condition, the EN pin must be toggled low or the controller must be power cycled. OVP is disabled during VID changes and when VOUT = 0 V.

Serial VID Interface (SVID)

For Intel proprietary interface communication details please contact Intel, inc.

Layout Notes

The NCP81568 has differential voltage and current monitoring. This improves signal integrity and reduces noise issues related to layout for easy design use. To ensure proper function, there are some general rules to follow. Always place the inductor current sense RC filters as close to the CSN and CSP pins on the controller as possible. Place the VCC/PVCC decoupling caps as close as possible to the controller VCC/PVCC pins.

Electrical Layout Considerations

Good electrical layout is key to ensure proper operation, high efficiency, and noise reduction. Electrical layout guidelines are:

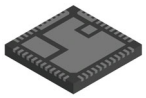
- *Power Paths:* Use wide and short traces for power paths (such as VIN, SW, and PGND) to reduce parasitic inductance and high−frequency loop area. It is also good for efficiency improvement.
- *Power Supply Decoupling:* The device should be well decoupled by input capacitors and input loop area should be a small as possible to reduce parasitic inductance, input voltage spike, and noise emission. Usually, a small low−ESL MLCC is placed very close to VIN and PGND pins.
- *VCC Decoupling:* Place decoupling caps as close as possible to the controller VCC and PVCC pins. The filter resistor at VCC pin should be not higher than 2.2 Ω to prevent large voltage drop.
- *Switching Node:* SW node should be a copper pour, but compact because it is also a noise source. SW Pin 9 should have a short inductance path to SW pins 18−28.
- *Bootstrap:* The bootstrap cap and optional resistor need to be very close and directly connected between BST and SW pins.
- *Voltage Sense:* Use Kelvin sense pair and arrange a “quiet” path for the differential output voltage sense.
- *Current sense:* Careful layout for current sensing is critical for jitter minimization, accurate current limiting, and IOUT reporting. The temperature compensating thermistor should be placed as close as possible to the inductor. The wiring path should be kept as short as possible and well away from the switch node.

Thermal Layout Considerations

Good thermal layout helps high power dissipation from a small package with reduced temperature rise. Thermal layout guidelines are:

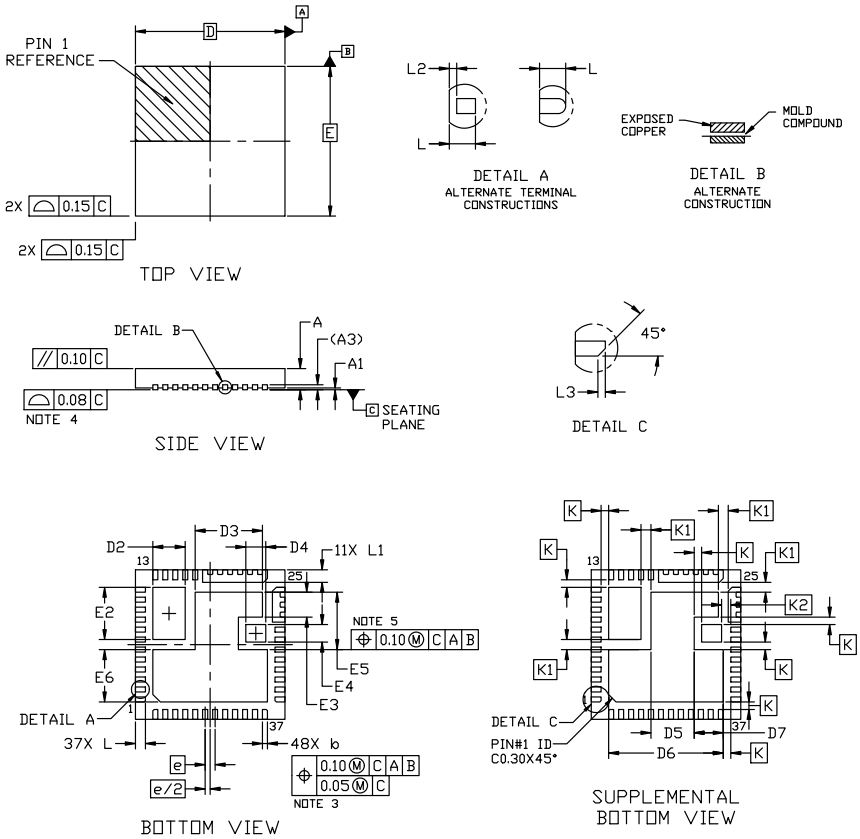
- The exposed pads must be well soldered on the board.
- A four or more layers PCB board with solid ground planes is preferred for better heat dissipation.
- More free vias are welcome to be around IC and underneath the exposed pads to connect the inner ground layers to reduce thermal impedance.
- Use large area copper pour to help thermal conduction and radiation.
- Do not put the inductor to be too close to the IC, thus the heat sources are distributed.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



PQFN48 6.00x6.00x0.75, 0.40P
CASE 483BT
ISSUE F

DATE 28 JUL 2023



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO ALL THREE EXPOSED PADS IN BOTH X AND Y AXIS.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	---	---	0.05
A3		0.20 REF.	
b	0.15	0.20	0.25
D	5.90	6.00	6.10
D2	1.20	1.30	1.40
D3	2.60	2.70	2.80
D4	0.70	0.80	0.90
D5	1.63	1.73	1.83
D6	4.50	4.60	4.70
D7	1.07	1.17	1.27
E	5.90	6.00	6.10
E2	2.00	2.10	2.20
E3	0.90	1.00	1.10
E4	0.60	0.70	0.80
E5	2.20	2.30	2.40
E6	2.00	2.10	2.20
e		0.40 BSC	
K		0.30 REF	
K1		0.40 REF	
K2		0.37 REF	
L	0.30	0.40	0.50
L1	040	0.50	0.60
L2	---	---	0.15
L3		0.15 REF	

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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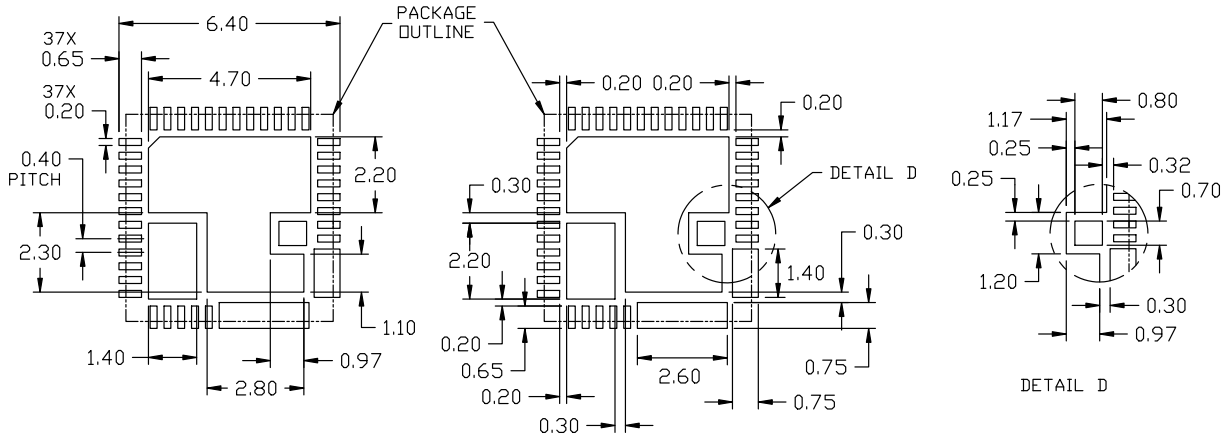
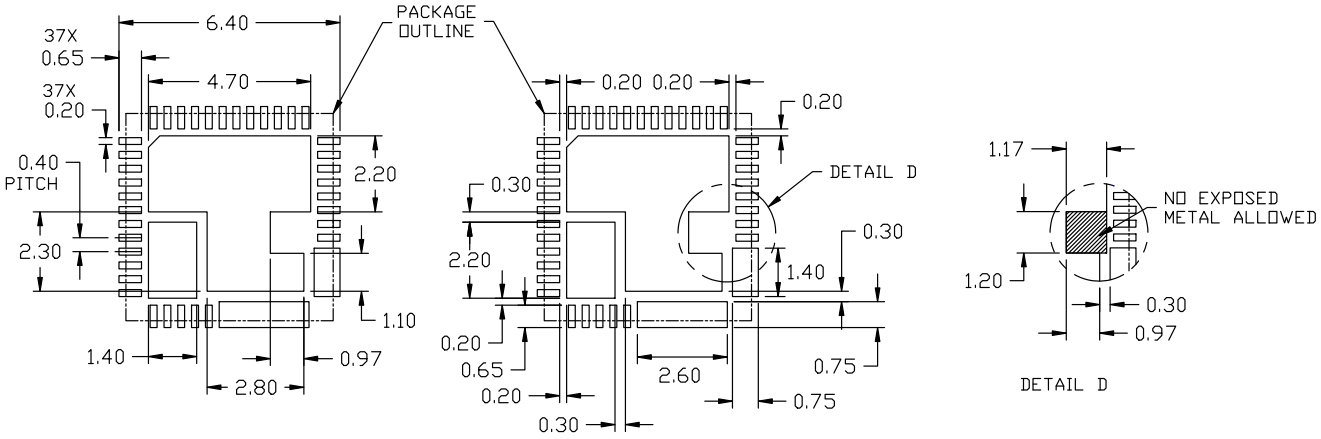


RECOMMENDED MOUNTING FOOTPRINT*
(1.5X SCALE)



RECOMMENDED MOUNTING FOOTPRINT - ALTERNATE*
(1.5X SCALE)

* For additional information on our Pb-Free strategy and soldering details, please download the ONSEMI Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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