Clock and synchronization signals of SAA7187 and SAA7188 Application note for digital video encoder

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1.0 INTRODUCTION

The devices of the SAA7187/88 family of video encoders can be used in a variety of applications differing regarding the signal flow of timing information. Video timing is defined by clock signals, synchronization signals and blanking signals. The video encoder ICs can generate these signals by itself (master mode), or can accept them as input (slave mode). The master/slave characteristic can be chosen independently for clock and sync-signals.

This application note describes the various clock and synchronization signals, their functions, and how to select and program them. The timing relation of some of these signals is programmable. An application example shows a possible configuration.

2.0 CLOCK LLC AND CREF SIGNAL

The SAA7187/88 has two clock signals: LLC and CREF, functionally compatible with other Philips digital video processing circuits. LLC on pin 38 is the Line-Locked-Clock in double pixel clock frequency. CREF on pin 39 is the clock qualifier signal, accompanying LLC, to indicate on which LLC edges the 16 bit wide YUV data stream transports valid data. CREF is continuously toggling in pixel rate frequency, but is not meant as pixel clock. The transitions of CREF have to maintain certain setup and hold times relative to clock LLC (see data sheet). The digital encoder ICs can generate and provide (drive) the clock signals by its own by means of the built-in crystal oscillator, or receive the clock signals from external. In remote genlock mode, LLC and CREF can be fed from one of the Philips digital decoder (DMSD), but must then be accompanied by RTC signal (real time control information).

2.1 Built-in clock signal generator

SAA7187/88 has built-in an optional crystal oscillator for LLC frequency. A crystal with double pixel clock frequency as base frequency, or as third harmonic frequency, with appropriate auxiliary circuitry, can be connected between the pins XTALi (input, pin 41) and XTALo (output, pin 40). The swing at the XTAL-pins is about 1Vpp, and is DC-compensated via an internal resistor between the two pins. Alternatively an external crystal oscillator could directly drive into XTALi.

An internal switch, hardware controlled by CDIR at pin 36, selects whether the IC provides or receives clock signals LLC and CREF (see Table 1). If CDIR is low, clock is taken from the internal crystal oscillator and the IC outputs LLC at pin 38 and CREF at pin 39. If CDIR is high, LLC pin and CREF pin are both switched to be input. The IC then requires a double pixel clock LLC from external circuitry at pin 38. Under certain conditions, CREF input at pin 39 has data-phase (timing) relevance, but it does not have directly clock and data qualifying function.

2.2 External Clock

In the “clock slave mode” case, i.e., if clock is provided from external into LLC pin 38, a CREF-like signal can optionally be applied to pin 39, but this is not required. If the IC sees a toggling signal, i.e., edges, at pin 39, CREF will contribute to re-synchronization of the internal horizontal counter (once per line) and – by that – defines the active data phases in the 16 bit wide YUV input data stream. If horizontal synchronization from external via RCV1 or RCV2 is selected, i.e., the encoder IC is in slave mode regarding horizontal timing, CREF defines together with the selected horizontal reference input signal, when the horizontal trigger counter has to start. From there the programming parameter HTRIG (11 bits in subaddress 6E and 6F) defines the start of the horizontal pixel counter, and the LSB of the parameter HTRIG determines one of the two possible phases of the internally effective CREF relative to the external provided CREF. The horizontal reference edge is defined regarding source and polarity by the various bits in subaddress 6Chec (see also later in this application note: re-trigger).

If no CREF is provided to the IC, a horizontal reference signal input is sampled direct with LLC resolution. The phase of the internal CREF, and expected valid data phases, are defined by the selected horizontal reference edge, and by the LSB of HTRIG. The horizontal reference edge is defined regarding source and polarity by the various bits in subaddress 6Chec (see also later in this application note: re-trigger).

Table 1. Selection of Clock Modes

CDIR	LLC	CREF	XTALo	XTALi	RTCI	RTCE
Pin 36	Pin 38	Pin 39	Pin 40	Pin 41	Pin 43	subaddress 61hex
low	output	output	local crystal		don’t care	don’t care
low	output	output	don’t care	external oscillator	don’t care	don’t care
high	input	don’t care but constant	don’t care		don’t care	0
high	input	input	don’t care		don’t care	0
high	input from DMSD/CGC	don’t care but constant	don’t care		RTCO from DMSD	1
high	input from DMSD/CGC	input from DMSD/CGC	don’t care		RTCO from DMSD	1

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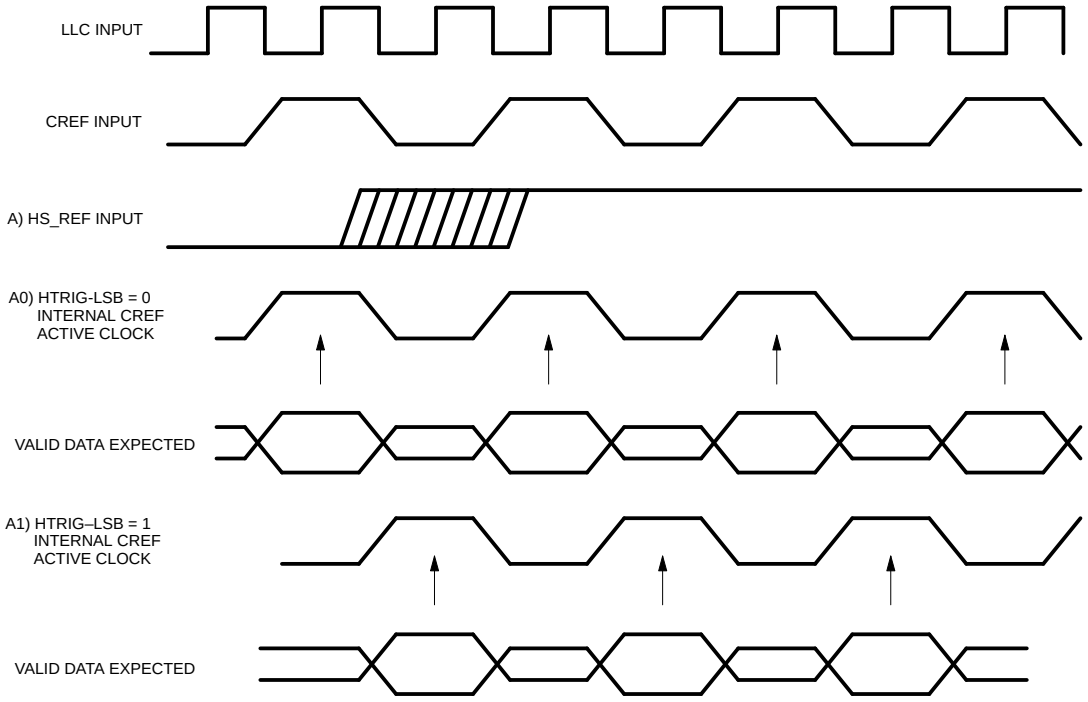

Figure 1. Timing of internal CREF and expected valid data input, if CREF and horizontal reference is provided from external into the encoder IC

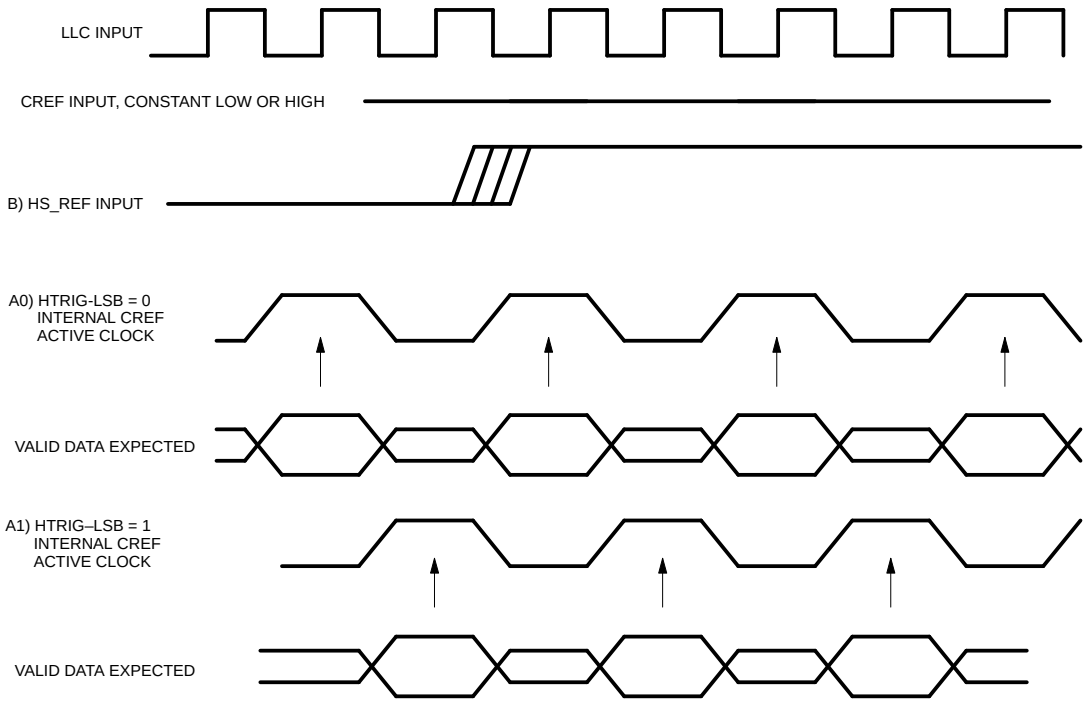

Figure 2. Timing of internal CREF based on horizontal reference signal input only

2.3 Clock accuracy

The digital encoder SAA7187 and SAA7188A synthesize all horizontal and vertical timing as well as the color subcarrier oscillation from the provided clock LLC, respectively crystal. If the clock frequency deviates from its nominal value, line and field frequency will change accordingly. Consumer type receiver equipment is rather tolerant regarding these raster frequencies, and can normally accept and follow several % deviations from the standard raster frequencies.

But the subcarrier frequency has much higher requirements regarding accuracy and stability to ensure proper color decoding. Broadcast quality class specification asks for less than 2ppm deviation of subcarrier frequency. Consumer type equipment may accept up to 50ppm static deviation, but dynamic deviation should be kept much smaller and very slow.

In case the crystal or the provided LLC at the digital encoder does not have the correct frequency, the synthesized color subcarrier frequency can still be adjusted to the required frequency value, by programming the 32 bit of “FSC” under subaddress 63hex to 66hex appropriate. Subcarrier phase reset PHRES in subaddress 70hex has then to be switched off, i.e., set to 00. In general, such an adjustment of “FSC” would produce a non-standard video output signal regarding subcarrier to line phase coupling, comparable to a regular VCR signal. The resulting video signal shows correct subcarrier frequency and (slightly) incorrect raster frequencies. It can be decoded and displayed correctly by any equipment that could handle VCR signals, e.g. by a consumer type television set.

2.4 Remote Genlock

In remote genlock mode the digital encoder runs with the line locked clock LLC, generated by a digital multi standard decoder (DMSD) respectively clock generator (CGC), like SAA7110, SAA7196, SAA7197 or SAA7157. In the decoding process the line locked clock LLC is derived from an analog video input signal as reference. If this input video signal is not stable or non standard, e.g., a camcorder play back signal, the DMSD will control LLC to stay line locked, which may result into a non-nominal clock frequency. The Philips digital decoder provides an RTC-signal (real time control information) to enable the digital encoder (DENC) to compensate such non-nominal clock, if decoder and encoder are running the same system, i.e., same sampling scheme (CCIR or SQP) and same video norm (field frequency, subcarrier frequency). Decoder LLC and RTCO output signal from DMSD must be connected to LLC and RTCI input signal of DENC. Horizontal and vertical sync signal of both systems can run with phase offset. The data path can have any processing delay, or may be not closed at all.

SAA7187 can be paired for remote genlock operation with the SAA7110, or SAA7191B plus SAA7197, or with SAA7196.

SAA7188A can be paired for remote genlock operation with SAA7151B plus SAA7157.

3.0 RASTER CONTROL OUTPUT SIGNALS

The NTSC / PAL video encoder has an internal synchronization circuitry. For the purpose of this application note it is referred to as horizontal counter – counting in clocks along a horizontal line – and as vertical counter – counting in half lines through a video field. A third counter for color field sequence identification is implemented to support the interlace characteristic of the video signal as well as to distinguish the NTSC four color field sequence, and PAL eight color field sequence. The IC has four Raster Control pins (RCxx), which reflect the timing and status of the internal synchronization circuitry. Two of them carry vertical / field synchronization signals, and two carry horizontal / line synchronization information. One of each pair is output only, the other one can be defined as output or as input, to re-trigger the internal synchronization circuitry. (The nomenclature of these four pins is related to data flow in a particular application, but should not be understood as restriction.) All four signals are defined on one and the same internal synchronization circuitry.

3.1 Vertical – Field – Reference Output Signals

The digital encoder SAA7187 and SAA7188A have two pins to output field reference Raster Control signals. RCM1 on pin 29 has output only functionality, and a fixed (nominal) signal polarity. RCV1 on pin 6 has selectable signal polarity and can be used as output or as input to re-trigger internal timing (see later in this application note).

3.1.1 Field Reference Signal Types

For both field reference outputs, one signal out of a set of the following three signal types can be selected independently.

VS Vertical Sync signal is nominal active (nominal high) for 3 lines if 60Hz timing is selected, or for 2.5 lines if 50Hz timing is selected, i.e., during those half lines, in which the analog CVBS output contains the main vertical sync pulses..

FS Frame Sync signal is an odd_/even signal, that is active (nominal low) during every first i.e. odd field, and inactive (nominal high) during every second, i.e., even field in the 2:1 interlace scheme of two fields in one frame. The first field is that field, in which the first main vertical sync pulse (serration pulse) starts in coincidence with the begin of a line.

FSEQ The color Field SEQuence signal indicates the start of the color field sequence (see CCIR report 624, e.g.). FSEQ is active (nominal high) during the first field of the 4-(NTSC) or 8-(PAL) color field sequence for standard encoding. FSEQ is inactive (nominal low) through all the other fields.

The position of the output signals VS, FS and FSEQ as RCM1 at pin 29, as well as RCV1 at pin 6, has a fix timing relationship to the internal horizontal and vertical counters and is not directly effected by programming of HTRIG or VTRIG. The leading (nominal rising) edge of VS, and all edges of FS and FSEQ occur at nominal field start (according to CCIR nomenclature), and on half line boundaries. For standard interlaced mode and nominal field length, FS is low for 262.5 (312.5) lines and high for 262.5 (312.5) lines, for example. The leading (nominal falling) edge of FS or the leading (nominal rising) edge of FSEQ indicates the begin of a frame, the begin of a field, and also the begin of a line, and can be used to reset/trigger external vertical as well as horizontal synchronization counter.

If the encoder is forced into non-interlaced mode through external re-trigger, the FS function is meaningless. If non-standard encoding regarding subcarrier-to-line coupling is applied, selection of FSEQ function is meaningless.

Selecting any of these signal for output as RCM1 on pin 29 or as RCV1 on pin 6 has no direct effect on internal blanking or other processing in the encoder IC itself. RCM1 and RCV1 as output are just auxiliary timing signals for use by the application environment, to support the video signal source (e.g., MPEG decompression circuitry, or video memory controller, or graphics generator) to time its data stream output.

3.1.2 Pin 29 : RCM1

Pin 29 RCM1 has output only function and carries field synchronizing raster control information. Via two SRCM bits in subaddress 6Dhex one of three types of field sync signals can be selected.

Table 2. Selection of RCM1 signal function on Pin 29

F = relevant function, x = other function/signal definition, – = don't care

BITS UNDER SUBADDRESS 6Dh								BITS UNDER SUBADDRESS 61h								SHORT NAME	FUNCTION RESULTING SIGNAL
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0		
								–	x	x	x	x	x	x	F	FISE	select field frequency (V–pulse sequence) select number of clocks/line (selects FSEQ as 4 or 8 field sequence)
–	–	–	–	F	F	x	x									SRCM	select RCM1 signal function
				0	0										0	VS 50Hz	active **high** for **2.5** lines at begin of every field
				0	0										1	VS 60Hz	active **high** for **3** lines at begin of every field
				0	1										0	FS 50Hz	**low** in **first** (odd) field, **312.5** lines high in second (even) field, 312.5 lines
				0	1										1	FS 60Hz	**low** in **first** (odd) field, **262.5** lines high in second (even) field, 262.5 lines
				1	0										0	FSEQ 50Hz	**high** in the **first** field **of 8** field sequence
				1	0										1	FSEQ 60Hz	**high** in the **first** field **of 4** field sequence
				1	1										x	n.a.	reserved, do not use

3.1.3 Pin 6 as Output: RCV1

Pin 6 RCV1 can assume output as well as input function and carries field synchronizing raster control information. Via two SRCV1x bits, PRCV1 bit and ORCV1 bit in subaddress 6Chex one of three types of field sync signals can be determined for RCV1 output.

Table 3. Selection of RCV1 output signal function on pin 6

F = relevant function, x = other function/signal definition, – = don't care

BITS UNDER SUBADDRESS 6Ch								BITS UNDER SUBADDRESS 61h								SHORT NAME	FUNCTION RESULTING SIGNAL
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0		
								–	x	x	x	x	x	x	F	FISE	select field frequency (V-pulse sequence) select number of clocks/line (defines FSEQ as 4 or 8 field sequence)
x	x	x	x	F	x	x	x									PRCV1	Select RCV1 signal polarity
x	x	x	F	x	x	x	x									ORCV1	Input or Output of RCV1 signal
F	F	x	x	x	x	x	x									SRCV1	Select RCV1 signal function
x	x		0	x											–	input	RCV1 is input, see Table 6
0	0		1	0											0	VS 50Hz	Active **high** for **2.5** lines at begin of every field
0	0		1	1											0	VS 50Hz	Active **low** for **2.5** lines at begin of every field
0	0		1	0											1	VS 60Hz	Active **high** for **3** lines at begin of every field
0	0		1	1											1	VS 60Hz	Active **low** for **3** lines at begin of every field
0	1		1	0											0	FS 50Hz	**Low** in first (**odd**) field, **312.5** lines High in second (even) field, 312.5 lines
0	1		1	1											0	FS 50Hz	**High** in first (**odd**) field, **312.5** lines Low in second (even) field, 312.5 lines
0	1		1	0											1	FS 60Hz	**Low** in first (**odd**) field, **262.5** lines High in second (even) field, 262.5 lines
0	1		1	1											1	FS 60Hz	**High** in first (**odd**) field, **262.5** lines Low in second (even) field, 262.5 lines
1	0		1	0											0	FSEQ 50Hz	**High** in the **first** field of **8** field sequence
1	0		1	1											0	FSEQ 50Hz	**Low** in the **first** field of **8** field sequence
1	0		1	0											1	FSEQ 60Hz	**High** in the **first** field of **4** field sequence
1	0		1	1											1	FSEQ 60Hz	**Low** in the **first** field of **4** field sequence
1	1		–	–											x	n.a.	reserved, do not use

3.2 Horizontal – Line – Reference Output Signals

The digital encoder SAA7187 and SAA7188A have two pins to output line reference Raster Control signals. RCM2 on pin 30 has output only functionality, and a fixed (nominal) signal polarity. RCV2 on pin 7 has selectable signal polarity and can be used as output, or as trigger input to re–synchronize internal timing, or as 'blanking' input to gate input data stream (see later in this application note).

Both horizontal raster control output signals can be freely defined along the line, and are active (nominal high) between "begin" and "end" (see Table 4). Begin and end can be chosen independently for RCM2 and RCV2. Both pairs are relative to the same internal horizontal counter, and are defined in LLC clocks. The internal horizontal counter manifests its timing in the analog output, and can depend on re–trigger via RCV1 or RCV2 input signals and programming of HTRIG under subaddress 6Ehex and 6Fhex (see later in this application note).

RCM2 and RCV2 as output are auxiliary timing signals for use by the application environment, e.g., to help the data source (MPEG decompression circuitry, video memory controller or graphics overlay generator) to time its data stream, or disable it. The programming of RCM2 and RCV2 as output does not effect internal blanking, data enabling, or any timing or processing in the encoder IC itself.

3.2.1 Pin 30: RCM2

Pin 30 RCM2 has output only function. RCM2 is active high between 'Begin = BMRQ' and 'End = EMRQ' in every line, i.e., also during vertical blanking interval VBI. Programming of FAL and LAL has no effect on RCM2. If End is programmed before (i.e., with a lower number than) Begin, RCM2 may be seen/understood as an active low signal between End and Begin.

3.2.2 Pin 7 as Output : RCV2

Pin 7 RCV2 can assume output as well as input function (see Tables 3, 4, and 5).

Program bit ORCV2 = 1 defines pin 7 for RCV2 output signal. RCV2 output is active (nominal high) from programmed 'Begin = BRCV' to 'End = ERCV'. The polarity is defined by program bit PRCV2.

Program bit CBLF defines whether RCV2 output is active in every line (CBLF = 0), regardless of vertical position, or whether RCV2 output is only active during selected vertical active range (CBLF = 1). Vertical active range is defined between 'first active line' FAL and 'last active line' LAL under subaddress 7Bhex to 7Dhex. By that, RCV2 as output signal could be used as horizontal line timing reference signal ("HREF") or as composite blanking signal ("CBN"), to enable data output at the video signal source. But if pin 7 is programmed as RCV2 output signal, its signal and related programming has no effect for any timing, blanking, data enabling or processing in the encoder IC itself. FAL and LAL defines internal vertical blanking, independently of whether CBLF is selecting it for gating of RCV2 output or not.

Table 4. Definition of output timing of RCM2 (pin 30) and RCV2 (pin 7)

PROGRAM WORD	11 BIT ADDRESS IN HORIZONTAL DIRECTION LLC RESOLUTION	RCM2 PIN30 OUTPUT ONLY	RCV2 PIN7 ONLY IF OUTPUT
BRMQ	subaddress 71hex, 73hex	L-to-H transition, rising edge	
ERMQ	subaddress 72hex, 73hex	H-to-L transition, falling edge	
BRMQ	subaddress 77hex, 79hex		begin of 'active' phase
ERMQ	subaddress 78hex, 79hex		end of 'active' phase

Table 5. Selection of RCV2 output signal function on pin 7

F = relevant function, x = other function/signal definition, – = don't care

BITS IN SUBADDRESS 6Chex								SHORT NAME	FUNCTION DESCRIPTION
7	6	5	4	3	2	1	0		
x	x	x	x	x	x	x	F	PRCV2	Polarity of RCV2
x	x	x	x	x	x	F	x	ORCV2	I/O of RCV2
x	x	x	x	x	F	x	x	CBLF	RCV2 in VBI (see FAL and LAL)
					x	0	x	input	RVC2 is input, see Table 7
					0	1	0	"HREF"	RCV2 **output** is active **high** between BRCV till ERCV in every line of the entire field, i.e., **including** VBI
					0	1	1	"HREF_"	RCV2 **output** is active **low** between BRCV till ERCV in every line of the entire field, i.e., **including** VBI
					1	1	0	"CBN"	RCV2 **output** is active **high** between BRCV till ERCV in active lines only from FAL to LAL, i.e., **excluding** VBI
					1	1	1	"CB"	RCV2 **output** is active **low** between BRCV till ERCV in active lines only from FAL to LAL, i.e., **excluding** VBI

4.0 RASTER CONTROL INPUT SIGNALS, SYNC-SLAVE-MODE

The internal synchronization circuitry of the digital encoder SAA7187 and SAA7188A are always defined by FISE (number of clocks per line, subaddress 61hex), FLEN (number of lines per field, subaddress 7Ahex and 7Dhex), and PAL (defining color field sequence length, subaddress 61hex). In sync slave mode, those horizontal and vertical counters can be re-triggered by an external trigger event at pin 6 as RCV1 input and/or at pin 7 as RCV2 input. The rising or falling edge can be selected as timing reference (trigger event) to re-synchronize the internal synchronization circuitry, regarding horizontal or vertical counter, or odd-even flip-flop, or color field sequence counter. As long as no trigger event occurs the internal counters are free running in the defined loops. Any single occurance of the selected edge in RCV1 or RCV2 input will hard re-trigger — i.e., it is not a smoothed PLL procedure. Due to processing pipeline delay, the resulting re-synchronization does not take effect before the next following corresponding period. A programmable vertical and horizontal trigger offset can be applied via VTRIG and HTRIG.

RCV2 as input can also optionally be used as “composite blanking” signal to gate the input data stream, but only for data coming through V-port (and D-port).

VTRIG represents a negative delay between external trigger event and internal vertical counter start, i.e., start of main vertical sync (serration) pulses. The external re-synchronization event at RCV1 over–writes the vertical counter state with VTRIG value, which then synchronizes the next vertical period to the external trigger signal. VTRIG is defined with 5 bits under subaddress 70 hex. The programmed VTRIG number corresponds with the position of the external trigger event along the field, counted in half lines. Programming 00 will synchronize the internal vertical counter to generate vertical sync at the begin of that same half line, in which the external trigger event occurs. Programming of 1F hex results in vertical sync output 31 half lines ahead of the external trigger input, for example.

HTRIG represents a negative delay between external trigger event and internal horizontal counter start, i.e., leading edge of horizontal sync pulse. The external re-synchronization event at RCV1 or RCV2 over-writes the horizontal counter state with HTRIG value, which then synchronizes the next horizontal period to the external trigger signal. HTRIG is defined with 11 bits under subaddresses 6E hex and 6F hex in LLC clock resolution, and covers the whole line period. The programmed HTRIG number corresponds with its position (in LLC clocks) along the scan line.

4.1 Pin 6 as Input: RCV1

If pin 6 is selected as input, RCV1 signal could carry field synchronization information in a form like vertical sync VS, or frame sync FS, or field sequence identification FSEQ. The actual re-trigger function of RCV1 input is defined via the two SRCV1 bits, TRCV2 bit, ORCV1 bit and PRCV1 bit, all in subaddress 6Chex, and the PAL bit in subaddress 61hex. Table 6 describes signal meaning and effect of RCV1 as input at pin 6.

Table 6. Selection of RCV1 input signal function on pin 6

F = relevant function, x = other function/signal definition, – = don't care

BITS UNDER SUBADDRESS 6Ch								BITS UNDER SUBADDRESS 61h								SHORT NAME	RCV1 INPUT PIN 6	FUNCTION: Active edge results in retrigger of following counters:			
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0			HORIZONTAL	VERTICAL	ODD/EVEN	COLOR FIELD SEQ
0	0	0	0	0											x	VS	rising	horizontal	vertical	(n-interl.)	
0	0	0	0	1											x	VS	falling	horizontal	vertical	(n-interl.)	
0	0	1	0	0											x	VS	rising		vertical		
0	0	1	0	1											x	VS	falling		vertical		
0	1	0	0	0											x	FS	rising	horizontal	vertical	odd field	
0	1	0	0	1											x	FS	falling	horizontal	vertical	odd field	
0	1	1	0	0											x	FS	rising		vertical	odd field	
0	1	1	0	1											x	FS	falling		vertical	odd field	
1	0	0	0	0											0	FSEQ8	rising	horizontal	vertical	odd field	1st of 8 fields
1	0	0	0	1											0	FSEQ8	falling	horizontal	vertical	odd field	1st of 8 fields
1	0	1	0	0											0	FSEQ8	rising		vertical	odd field	1st of 8 fields
1	0	1	0	1											0	FSEQ8	falling		vertical	odd field	1st of 8 fields
1	0	0	0	0											1	FSEQ4	rising	horizontal	vertical	odd field	1st of 8 fields
1	0	0	0	1											1	FSEQ4	falling	horizontal	vertical	odd field	1st of 8 fields
1	0	1	0	0											1	FSEQ4	rising		vertical	odd field	1st of 8 fields
1	1	1	0	1											1	FSEQ4	falling		vertical	odd field	1st of 8 fields
1	1	x	x	x											x	n.a		reserved, do not use			
x	x	x	1	x											x	n.a.	output	RCV1 is output, see Table 3			
								–	x	x	x	x	x	x	F	FISE		Select field frequency (V-pulse sequence) select clocks per line defines FSEQ as 4 or 8 field sequence			
x	x	x	x	F	x	x	x									PRCV1		Select RCV1 signal porlarity			
x	x	x	F	x	x	x	x									ORCV1		Input or Output of RCV1 signal			
x	x	F	x	x	x	x	x									TRCV2		RCV1 or RCV2 for horizontal trigger			
F	F	x	x	x	x	x	x									SRCV1		Select RCV1 signal function			

4.2 Pin 7 as Input: RCV2

If pin 7 is selected as input, RCV2 signal can carry just line synchronization information like horizontal sync HS, or input data gating function like HREF or CBN. The horizontal re-trigger function and the data input gating function can be utilized seoarately, or they combined. The actual function of RCV2 input is defined via the CBLF bit, ORCV2 bit, PRCV2 bit and TRCV2 bit, all in subaddress 6Chex. Table 7 describes signal meaning and effect of RCV1 as input at pin 6.

Table 7. Selection of RCV2 input signal function on pin 7

("x" defines other functions/signals)

BITS IN SUBADDRESS 6Chex								SHORT NAME	RCV2 INPUT	FUNCTION DESCRIPTION
7	6	5	4	3	2	1	0		pin 7	
							F	PRCV2		Polarity of RCV2
						F		ORCV2		I/O of RCV2
					F			CBLF		RCV2 in VBI (see FAL and LAL)
		F						TRCV2		Select horizontal trigger from RCV1/2
		0			0	0	–		any input	but not used for re-trigger or gating
		0			1	0	0		input high	enable V-port data input for encoding
									input low	disable V-port data input for encoding
		0			1	0	1		input low	enable V-port data input for encoding
									input high	disable V-port data input for encoding
		1			0	0	0		rising edge	horizontal re-trigger, with HTRIG
		1			0	0	1		falling edge	horizontal re-trigger, with HTRIG
		1			1	0	0		rising edge	horizontal re-trigger, with HTRIG
									input high	disable V-port data input for encoding
									input low	enable V-port data input for encoding
		1			1	0	1		falling edge	horizontal re-trigger, with HTRIG
									input low	disable V-port data input for encoding
									input high	enable V-port data input for encoding
		x			x	1	x		output	RCV2 is output, see Table 5

5.0 SYNC TIMING DEPENDENCIES

The selected “active” edge of the external timing reference signal RCV1 or RCV2 loads the internal horizontal counter with the HTRIG value. At the end of the line the counter is automatically reset, and all timing signals are in phase with the requesting re-trigger. This horizontal counter also defines the begin and end points of the raster control output signals.

The effect of VTRIG for vertical synchronization timing is very similar.

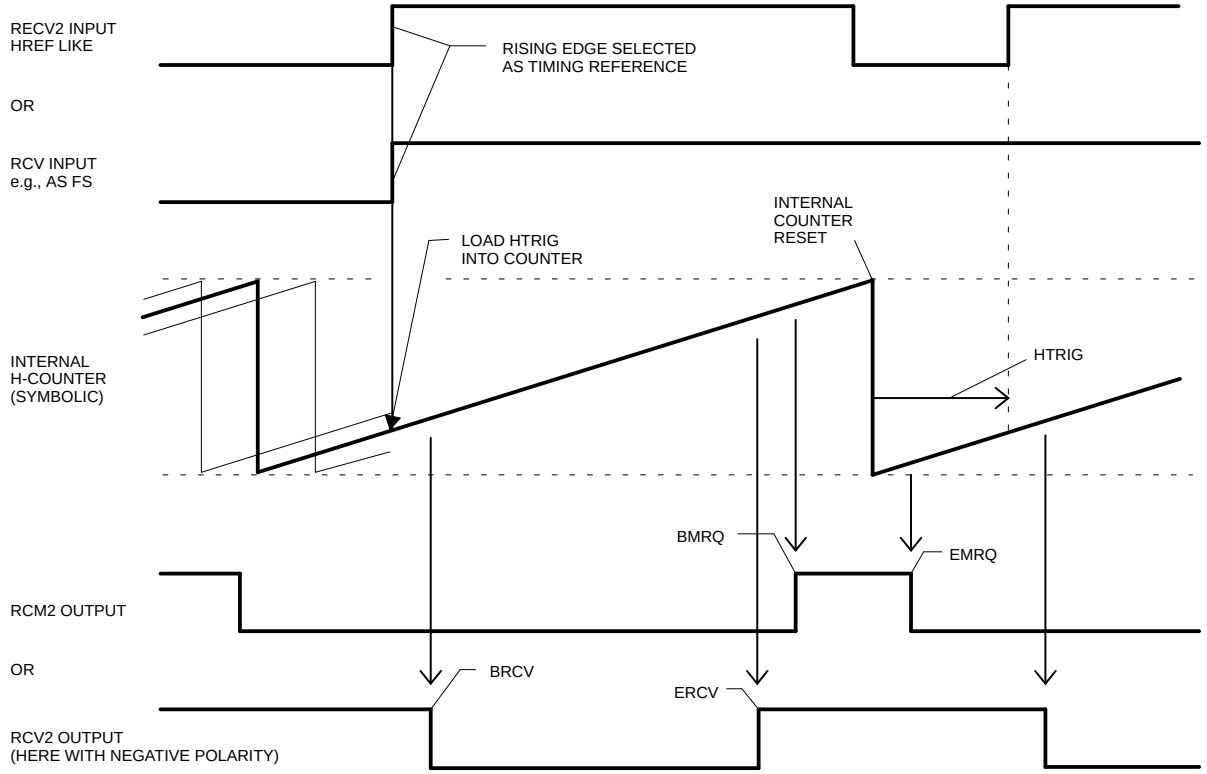

Figure 3. Horizontal ti ming for re-trigger and raster control output signal definition

6.0 APPLICATION EXAMPLE

Figure 4 points out several of those features that can be realized in an application with SAA7188A (or SAA7187). Two or more digital video encoder devices can be locked to each other. All their analog video outputs are completely in phase: horizontally, vertically and also the subcarrier. One of the devices functions as timing master, the other ones work in sync slave mode. The master device provides on RCM1 the color field sequence indication signal FSEQ, which transports horizontal and vertical reference as well as subcarrier phase reference via the color field sequence indication. The RCV1 inputs of the other devices are set to FSEQ function and also used to trigger line timing. VTRIG and HTRIG are both set to zero.

RCM2 output of the master device can be freely defined in horizontal timing. By that it can be used as input data gating signal (HREF–gate) at the RCV2 inputs of the other encoder devices. This RCM2 output signal of the master device (or of each device) could also be fed back to its own RCV2 input for input data gating function.

RCM1 and RCM2 outputs of the slave devices can be used as trigger and timing signals for the digital video signal sources. RCM1 can be chosen as a vertical sync, or as an odd/even signal. RCM2 can be defined as an HS for trigger and counting purposes, or it can be used as a source gating signal. It can be placed ‘early’ to compensate for pipeline delay on the data delivery side, such as memory access, etc.

If the RCV2 pins of the slave (and/or the master) device are not used as gating input, they could be switched to output, and could be used as (early) enabling signal (CBN) at the signal source. In that case even VBI blanking is supported. (This option is not shown in Figure 4).

The digital encoder that works as timing master in the configuration of Figure 4 can be genlocked to an analog video reference signal via digital encoder circuitry. For this purpose, the SAA7188A can be combined with the SAA7151B, SAA7157 and TDA8708/09. The SAA7187 can be combined with the SAA7191B, SAA7197 and TDA8708/09 or with the SAA7110. The digital real-time decoder system locks itself to the analog reference video signal and generates line-locked clock, horizontal and vertical sync signals, and the real-time control signal RTC. If the encoder runs with the line-locked clock of the decoder, it is important to also have the RTC wire connected, in order to maintain the correct subcarrier frequency in the encoder, same as in the analog reference signal. To have the same clock at both the decoder and encoder side is very interesting in some applications; for example, as a frame buffer as it avoids the complications of an asynchronous two-clock system.

The SAA7151B or other decoder can provide a pair of vertical and horizontal syncs as VS and HS, or provide an odd/even signal FS (“ODD” on pin 39 of SAA7151B, for example) to synchronize the digital encoder to the reference video signal, and also into the correct interlace sequence. Proper programming of HTRIG and VTRIG can adjust pipeline processing delay in decoder and/or frame buffer circuitry. If FS from the decoder is used as RCV1 input for the first “master” encoder, it can also be utilized as a horizontal reference signal. Then RCV2 is free to be used as gating input, fed by the RCM2 output, or it can be switched to output a CBN-like signal to one of the video signal sources.

Figure 4 shows a rather complex system, but the various timing techniques, as discussed above, can be applied in simpler systems, too.

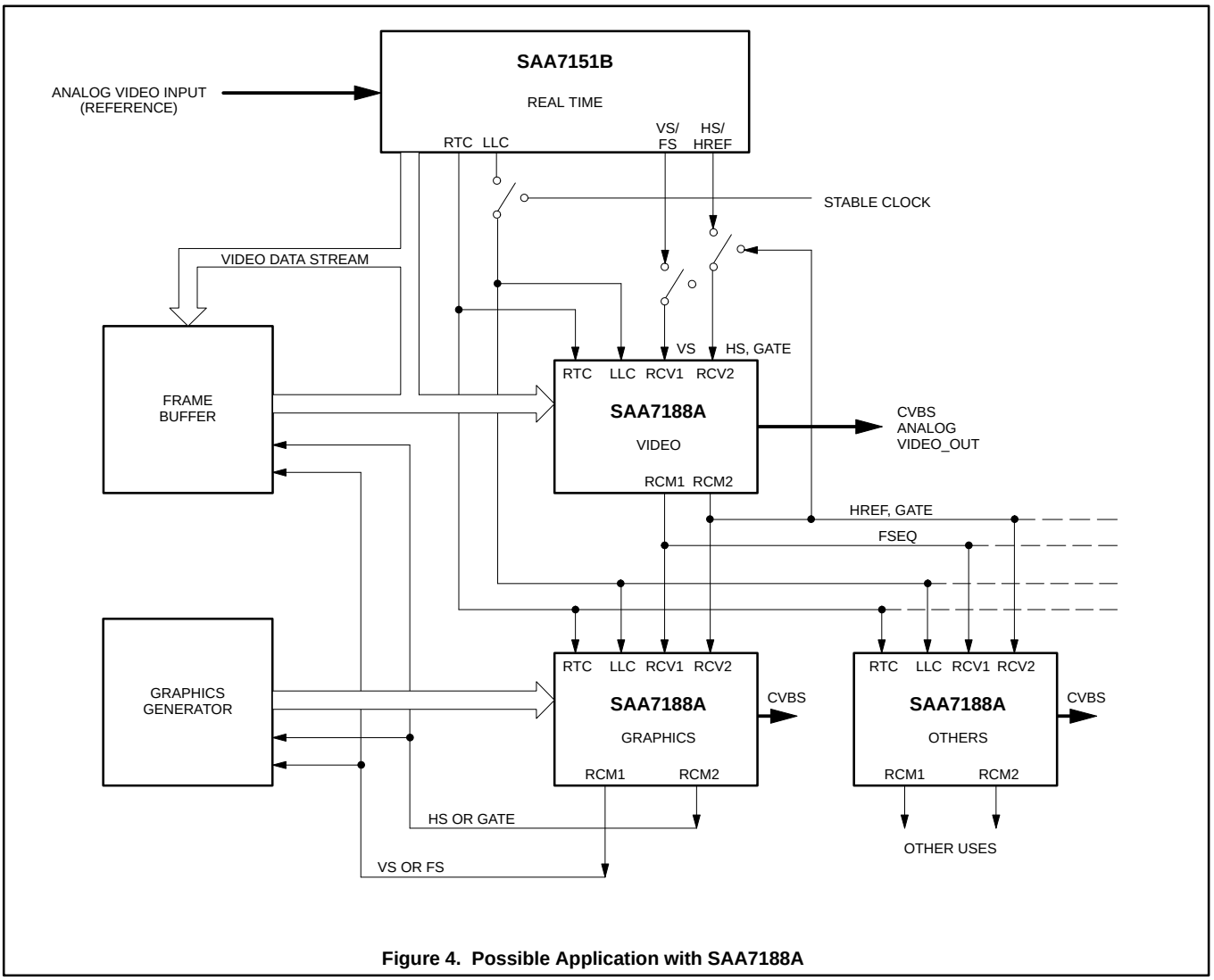

Figure 4. Possible Application with SAA7188A

7.0 APPENDIX: SOME PROGRAMMING TABLES

7.1 Synchronization Signals (6C, 6D, 70)

7.1.1 Subaddress 6C hex

Table 8. Program for RCV1 and RCV2 function at pin 6 and pin 7 in subaddress 6C-hex

BITS IN SUBADDRESS 6Chex								SHORT NAME	FUNCTION DESCRIPTION	DEFAULT AFTER RESET
7	6	5	4	3	2	1	0			
								PRCV2		
							0		RCV2 is active high, rising edge is timing reference	0
							1		RCV2 is active low, falling edge is timing reference	
								SRVC2	CBLF & ORCV2	
					0	0			RCV2 is input, has no input data gating function, but can be used for horizontal re-trigger, see TRCV2	00
					0	1			RCV2 is output, horizontal (timing) reference signal in all lines, begin and end freely programmable by BRCV and ERCV	
					1	0			RCV2 is input, and has input data gating function, can also be used for horizontal re-trigger, see TRCV2	
					1	1			RCV2 is output, can be used as external composite blanking signal, horizontal begin and end defined by BRCV and ERCV, vertial first active line defined by FAL, first inactive line defined by LAL (FAL – LAL, then all lines active).	
								PRCV1		
				0					RCV1 is active high, rising edge is timing reference	0
				1					RCV1 is active low, falling edge is timing reference	
								ORCV1		
			0						RCV1 is input	0
			1						RCV1 is input	
								TRCV2		
		0							Horizontal re-trigger by RCV1, RCV1 must be input	0
		1							Horizontal re-trigger by RCV2, RCV2 must be input	
								SRCV1		
0	0								VS (vertical sync), every field	00
0	1								FS (frame sync), odd_/even	
1	0								FSEQ color field sequence indication	
1	1								n.a.; don't use this combination	
0	0	0	0	0	0	0	0	00 hex	default after reset IC is prepared to accept an odd/_even signal at RCV1 (rising edge at begin of first field)	0000 0000

7.1.2 Subaddress 6D hex

Table 9. Program for RCM1 at pin 29 and "Line 21" encoding in subaddress 6D-hex

BITS IN SUBADDRESS 6Dhex								SHORT NAME	FUNCTION DESCRIPTION
7	6	5	4	3	2	1	0		
								CCEN	"Line 21" encoding, Closed Caption and Extented Data service
						0	0		no "line 21" encoding in either field
						0	1		"Line 21" encoding in first (odd) field only (extented data), data content as programmed in subaddress 69hex and 6Ahex
						1	0		"Line 21" encoding in second (even) field only (Closed Caption), data content as programmed in subaddress 67hex and 68hex
						1	1		"Line 21" encoding in both fields
								SRCM	select type of field reference output signal on pin 29 RCM1
				0	0				VS (vertical sync), active high during serration pulses (3 or 2.5 lines)
				0	1				FS (frame sync), active low during odd field, high during even field
				1	0				FSEQ color (field sequence indication signal), active high during first field of four fields, if FISE = 1 (60 Hz, 525 lines) first field of eight fields, if FISE = 0 (50 Hz, 625 lines)
				1	1				n.a.; do not use this combination
0	0	0	0						reserved

7.1.3 Subaddress 70 hex

Table 10. Program for VTRIG and VBI (vertical blanking interval) in subaddress 70-hex

BITS IN SUBADDRESS 70hex								SHORT NAME	FUNCTION DESCRIPTION
7	6	5	4	3	2	1	0		
								VTRIG	vertical trigger phase offset
			x	x	x	x	x		half line number, in which vertical/field trigger input occurs
								SBLBN	Vertical Blanking Interval (VBI)
		0							blanking is enforced in all lines outside FAL-to-LAL, (First Active Line to Last Active Line, see subaddress 7B, 7C, and 7D)
		1							blanking is only enforced only during equalization and serration (vertical sync) pulses, i.e., 9 (60Hz) or 7.5 (50Hz) lines, signal insertion a/o encoding also outside FAL-to-LAL, allowing data, time code or test signal insertion in regular VBI
								PHRES	color subcarrier reset mode, to support SC-H coupling
0	0								continuously running color subcarrier oscillation, e.g., for remote genlock RTC mode
0	1								color subcarrier phase reset every second line
1	0								color subcarrier phase reset every eighth field (PAL)
1	1								color subcarrier phase reset every fourth field (NTSC)

7.2 Video Standard Parameters (61, 70, 60)

7.2.1 Subaddress 60 hex

Table 11. Basic video standard parameters in subaddress 61-hex

BITS IN SUBADDRESS 61-hex								SHORT NAME	FUNCTION DESCRIPTION	DEFAULT AFTER RESET
7	6	5	4	3	2	1	0			
								FISE	field frequency mode select	
							0		50 Hz, 312.5 lines per field, 5 V-sync serration pulses etc, (start pre-equalization pulses 310 lines after field start) 864 (CCIR) pixels per line, i.e., 1778 LLC, 13.5 MHz 944 (SQP) pixels per line, i.e., 1888 LLC, 14.75 MHz FSEQ generates 4 field sequence	
							1		60 Hz, 262.5 lines per field, 6 V-sync serration pulses etc, (start pre-equalization pulses 259.5 lines after field start) 858 (CCIR) pixels per line, i.e., 1716 LLC, 13.5 MHz 780 (SQP) pixels per line, i.e., 1560 LLC, 12.27 MHz FSEQ generates 8 field sequence	1
								PAL	switch of subcarrier phase for V-component in alternative lines	
						0			no color subcarrier phase toggle switch, for NTSC encoding	0
						1			PAL-switch, i.e., subcarrier phase switch (±45° toggle) for V-color component in alternative lines, for PAL encoding	
								SCBW	chrominance bandwidth	
					0				extended chrominance bandwidth, e.g., option for S-video output	
					1				standard chrominance bandwidth	1
								RTCE	Real Time Control enable	
				0					no Real Time Control applied, standard subcarrier generation, relies on clock LLC stability	0
				1					Real Time Control of subcarrier frequency generation, RTC connection from appropriate Philips decoder needed	
								YGS	luminance gain select	
			0						luminance (black to white) is adjusted to 100 IRE	
			1						luminance (black to white) is adjusted to 92.5 IRE, giving room for 7.5 IRE setup, e.g., for NTSC	1
								INPI	PAL switch phase	
		0							nominal (standard) phase of PAL-switch	0
		1							opposite to standard, e.g., to adjust pipeline delay in RTC mode	
								DOWN	analog output (DACs)	
	0								DACs in normal operation, analog output of encoded video signal	0
	1								DACs are switched to lowest output voltage	
0									reserved	0
0	0	0	1	0	1	0	1	15 hex	default after reset	0001 0101

7.2.2 Subaddress 70 hex

Table 12. Program for subcarrier phase reset (SC-H) in subaddress 70-hex

BITS IN SUBADDRESS 70hex								SHORT NAME	FUNCTION DESCRIPTION
7	6	5	4	3	2	1	0		
								VTRIG	vertical trigger phase offset
			x	x	x	x	x		half line number, in which vertical/field trigger input occurs
								SBLBN	Vertical Blanking Interval (VBI)
		0							blanking is enforced in all lines outside FAL-to-LAL, (First Active Line to Last Active Line, see subaddress 7B, 7C, and 7D)
		1							blanking is only enforced only during equalization and serration (vertical sync) pulses, i.e., 9 (60Hz) or 7.5 (50Hz) lines, signal insertion a/o encoding also outside FAL-to-LAL, e.g., data, time code or test signal insertion in regular VBI
								PHRES	color subcarrier reset mode, to support SC-H coupling
0	0								continuously running color subcarrier oscillation, e.g., for remote genlock RTC mode
0	1								color subcarrier phase reset every second line
1	0								color subcarrier phase reset every eighth field (PAL)
1	1								color subcarrier phase reset every fourth field (NTSC)

7.2.3 Subaddress 60 hex

Table 13. Program for cross color reduction in analog CVBS-out under subaddress 60-hex

BITS IN SUBADDRESS 60hex								SHORT NAME	FUNCTION DESCRIPTION
7	6	5	4	3	2	1	0		
		0	0	0	0	0	0		reserved
								CCRS	Cross Color Reduction, reducing cross talk from luminance into chrominance as support for the testination receiver / decoder filter are active only from FAL-to-LAL, i.e., active video
0	0								standard CVBS, straight addition of luminance and chrominance signals
0	1								notch filter at 4.5 Mhz in luminance signal before adding chrominance, e.g., for PAL color subcarrier or NTSC sound carrier
1	0								notch filter at 3.3 Mhz in luminance signal before adding chrominance, wide and deep, e.g., for NTSC color subcarrier
1	1								notch filter at 3.3 Mhz in luminance signal before adding chrominance, more narrow than other one, e.g., for NTSC color subcarrier

7.3 Input Data Format and Signal Flow (3A, 6B)

7.3.1 Subaddress 3A hex, SAA7188A only

Table 14. Program for input data de-formating in subaddress 3A-hex

BITS IN SUBADDRESS 3A-hex								BIT NAME	FUNCTION DESCRIPTION	DEFAULT AFTER RESET
7	6	5	4	3	2	1	0			
								MUV2C	(M-port chroma two's complement)	
							0		Cb-Cr data at M-port is expected in two's complement	
							1		Cb-Cr data at M-port is expected in offset binary (acc. to CCIR 656)	1
								MY2C	(M-port luminance two's complement)	
						0			Y data at M-port is expected in two's complement around medium gray	
						1			Y data at M-port is expected in straight binary (acc. to CCIR 656)	1
								VUV2C	(V/D-port chroma two's complement)	
					0				Cb-Cr data at V/D-port is expected in two's complement (compare DTV-mode of SAA7151B)	0
					1				Cb-Cr data at V/D-port is expected in offset binary (CCIR-mode)	
								VY2C	(V-port luminance two's complement)	
				0					Y data at V-port is expected in two's complement around medium gray	0
				1					Y data at V-port is expected in straight binary (CCIR- and DTV-mode)	
								V656	data format at V-port and D-port	
			0						16 bit YUV interface formed by V-port = Y & D-port = UV	
			1						8-bit wide CCIR656 compatible data format at V-port	1
	0	0							reserved	00
								CBENB	internal color bar test signal switch	
0									normal encoding of input data	0
1									color bar test signal via encoding of LUT values	
0	0	0	1	0	0	1	1	13 hex	default after reset	0001 0011

7.3.2 Subaddress 6B hex, SAA7188A only

Table 15. Program for input data selection in subaddress 6B-hex

BITS IN SUBADDRESS 6B-hex								SEL_ED Pin 18	BIT NAME FUNCTION DESCRIPTION
7	6	5	4	3	2	1	0		
									MODIN defines data from which port gets encoded
0	0							–	data from M-port gets encoded
0	1							1	data from M-port gets encoded
0	1							0	data from V(/D)-port gets encoded
1	0							–	data from V(/D)-port gets encoded
1	1							1	data from V(/D)-port gets encoded
1	1							0	data from M-port gets encoded
		0	x	x	x	x	x		other function: line number for closed caption encoding

7.4 Input Data Formats (subaddress 3A), SAA7187 only

7.4.1 Subaddress 3A hex, SAA7187 only

Table 16. Program for input data de-formating in subaddress 3A-hex

BITS IN SUBADDRESS 3A-hex								BIT NAME	FUNCTION DESCRIPTION	DEFAULT AFTER RESET
7	6	5	4	3	2	1	0			
								FMT	Input Data Formats	
						0	0		YUV 4:4:4 on 24 pins, Y on VP1, V=Cr on VP2, U=Cb on VP3	00
						0	1		YUV 4:2:2 on 16 pins, Y on VP1, U=Cb and V=Cr multipexed on VP3	
						1	0		YUV 4:2:2 on 8 pins, on VP1, multipexed according to CCIR-656	
						1	1		reserved	
								VUVC	chroma two's complement	
					0				Cb-Cr input data is expected in two's complement	0
					1				Cb-Cr input data is expected in offset binary (CCIR-mode)	
								VY2C	luminance two's complement	
				0					Y data at V-port is expected in two's complement around medium gray	0
				1					Y data at V-port is expected in straight binary (CCIR- and DTV-mode)	
	0	0	0						reserved	000
								CBENB	internal color bar test signal switch	
0									normal encoding of input data	0
1									color bar test signal via encoding of LUT values	
0	0	0	0	0	0	0	0		00 hex default after reset	0000 0000