8-Bit Parallel-Out Serial Shift Registers

LS164

FEATURES

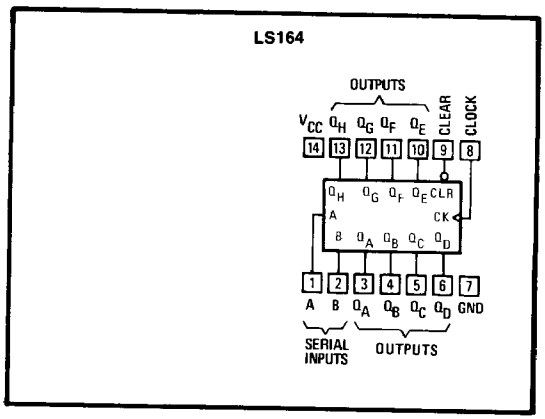
- Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Asynchronous Clear

DESCRIPTION

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

9LS/54LS devices are characterized for operation over the full military temperature range of −55°C to 125°C; 9LS/74LS devices are characterized for operation from 0°C to 70°C.

PIN-OUT DIAGRAM



FUNCTION TABLES

INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	Q_A	$Q_B \ldots Q_H$	
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

H = high level (steady state), L = low level (steady state)

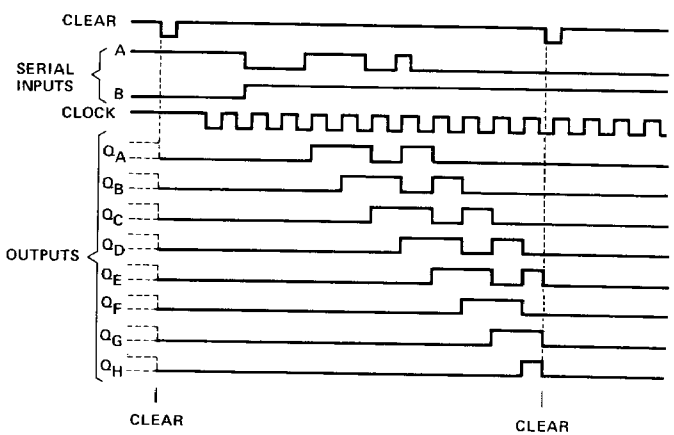
X = irrelevant (any input, including transitions)

↑ = transition from low to high level.

Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B or Q_H, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

TYPICAL CLEAR, SHIFT, AND CLEAR SEQUENCES



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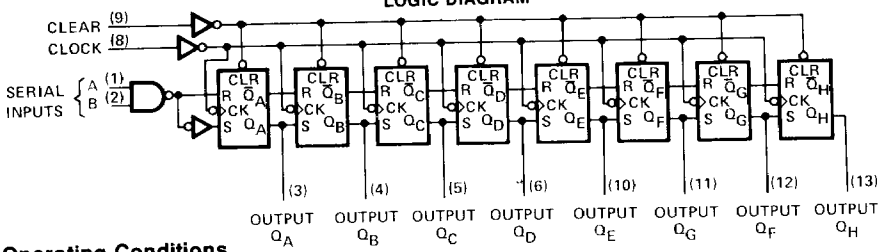
LOGIC DIAGRAM



Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear input pulse, t_w	20			20			ns
Data setup time, t_{setup} (see Figure 1)	15			15			ns
Data hold time, t_{hold} (see Figure 1)	5			5			ns
Operating free-air temperature, T_A	-55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*		9LS/54LS			9LS/74LS			Unit
			Min	Typ**	Max	Min	Typ**	Max	
V_{IH}			2			2			V
V_{IL}					0.7			0.8	V
V_I	V_{CC}=MIN, I_I=-18mA				-1.5			-1.5	V
V_{OH}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max, I_{OH}=-400μA		2.5	3.5		2.7	3.5		V
V_{OL}	V_{CC}=MIN, V_{IH}=2V, V_{IL}=V_{IL}max	I_{OL}=4mA		0.25	0.4		0.25	0.4	V
		I_{OL}=8mA					0.35	0.5	
I_I	V_{CC}=MAX, V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX, V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX, V_I=0.4V				-0.4			-0.4	mA
I_{OS}†	V_{CC}=MAX		-15		-100	-15		-100	mA
I_{CC}††	V_{CC}=MAX			16	27		16	27	mA

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5V, T_A = 25°C.
†Not more than one output should be shorted at a time.
††I_{CC} is measured with outputs open, serial inputs grounded, the clock input at 2.4V, and a momentary ground, then 4.5V applied to clear.

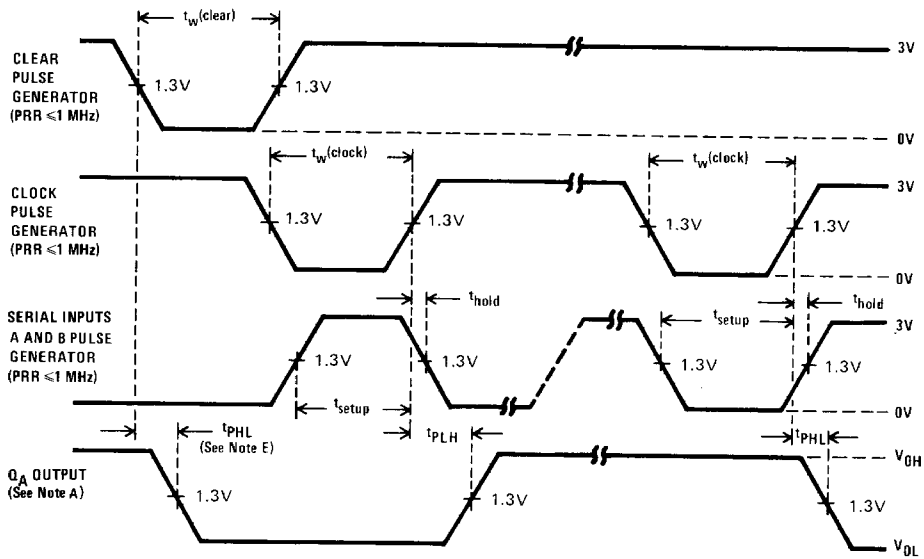
Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameter	-55°C			+25°C			+125°C			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. 1, page 2-95 and Fig. A, page 2-174)										
f_{max}				25	36					MHz
t_{PHL}		26	38		24	36		26	38	ns
t_{PLH}		20	30		17	27		20	30	ns
t_{PHL}		24	35		21	32		24	35	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. 1, page 2-95 and Fig. A, page 2-174)										
t_{PHL}		29	42		27	40		29	42	ns
t_{PLH}		23	34		20	31		23	34	ns
t_{PHL}		27	39		24	36		27	39	ns

Note: AC specification shown under -55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS only.

FIGURE 1

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES: A. Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.

B. Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.