

### Description

The 5P49EE502-166 is a programmable clock generator intended for low-power, battery-operated applications. There are 4 individually programmable PLLs connected to 5 outputs, allowing up to 5 different output frequencies. All PLLs are driven from a common reference clock which can come from a crystal or an external oscillator.

The IDT5P49EE502 datasheet contains detailed information on how to configure this device.

### Typical Applications

- Battery-powered, portable devices

### Output Features

- 5 single-ended LVTTTL/LVCMOS outputs
- 2 V<sub>DDO</sub> rails support 1.8V, 2.5V, 3.3V output swing
- Each output can be connected to either of the 2 V<sub>DDO</sub> rails

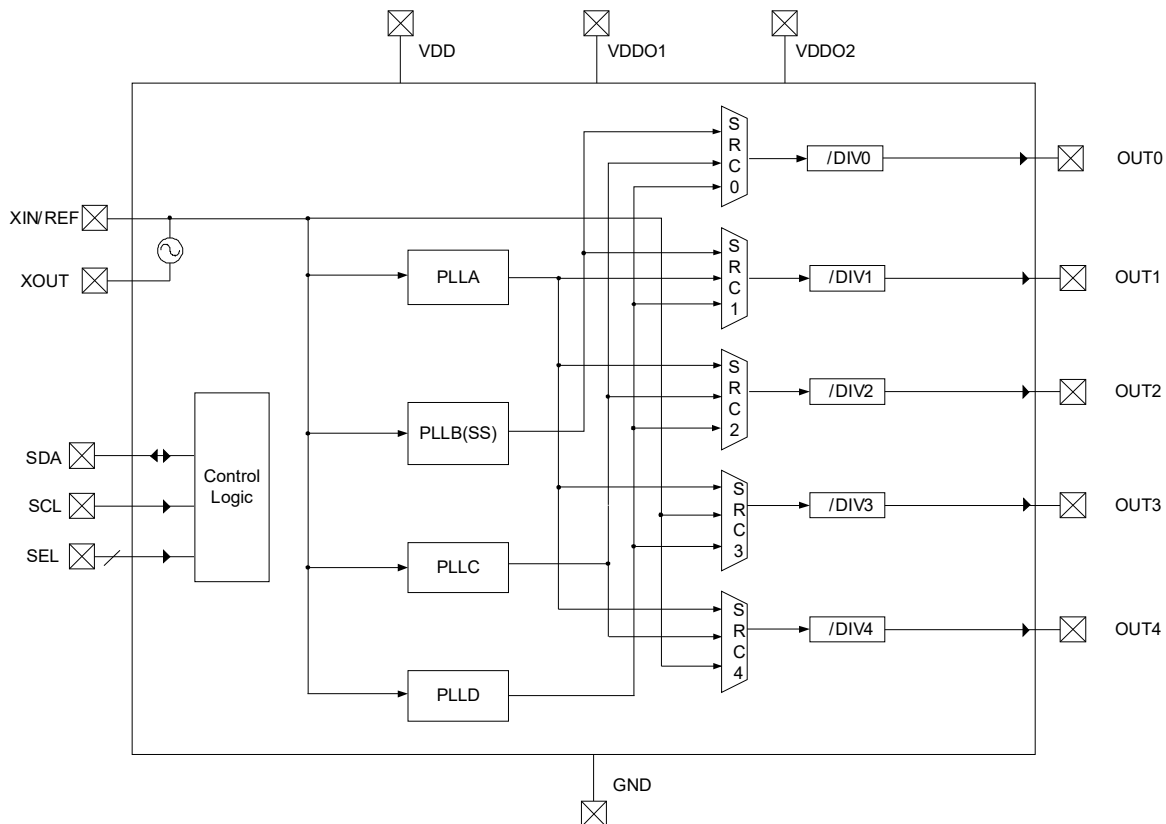
### Features

- 1.8V core; minimal power consumption
- Power-down/Sleep Mode; supports power management
- Programmable slew rate for each output; allows tuning for various line lengths
- 120MHz maximum output frequency; supports wide range of frequency in mobile device
- One spread spectrum PLL with adjustable modulation rate and amplitude; EMI reduction and the ability to spread video clocks with no visible artifacts
- 5.0V tolerant SMBus interface works with legacy controllers
- Space saving 3 x 3 mm 20-VFQFPN; minimal board space
- -40°C to +85°C industrial operating range

### Key Specifications

- 4 PLLs
- Programmable via I<sup>2</sup>C
- Internal non-volatile EEPROM holds 3 configurations

### Block Diagram



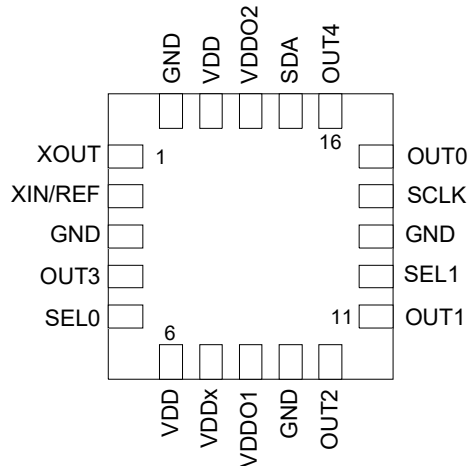
## Output Selection Table

SEL Config Setting		Input	Input Frequency (MHz)	OUT0 (MHz)	OUT1 (MHz)	OUT2 (MHz)	OUT3 (MHz)	OUT4 (MHz)	Spread (%)
S1	S0								
0	0	Crystal	25	Power down/Sleep mode					–
0	1	Crystal	25	Hi-Z	Hi-Z	50	50	50	–
1	0	Crystal	25	Hi-Z	50	50	50	50	–
1	1	Crystal	25	50	50	50	50	50	–
Driver Type		-	-	3.3V LVCMOS	3.3V LVCMOS	3.3V LVCMOS	3.3V LVCMOS	3.3V LVCMOS	–
Connection		-	VDDO1	VDDO1	VDDO1	VDDO1	VDDO1	VDDO2	–

## Output Voltage Table

	V <sub>DDO1</sub> Pin 8	V <sub>DDO2</sub> Pin 18
V <sub>DD</sub> (V)	3.3	3.3

## Pin Assignment



3 x 3 mm 20-VFQFPN

## Pin Descriptions

Pin Name	Pin #	I/O	Pin Type	Pin Description
XOUT	1	O	LVTTTL	MHz CRYSTAL_OUT – Reference crystal feedback. Float pin if using reference input clock.
XIN/ REF	2	I	LVTTTL	MHz CRYSTAL_IN – Reference crystal input or external reference clock input. Maximum clock input voltage is 1.8V.
GND	3		Power	Connect to ground.
OUT3	4	O	Output	Buffered reference clock output. Single-ended output voltage levels are register controlled by either V <sub>DDO1</sub> or V <sub>DDO2</sub> .
SEL0 *	5	I	LVTTTL	Configuration select pin. Weak internal pull-down resistor.
V <sub>DD</sub>	6		Power	Device power supply. Connect to 1.8V.
V <sub>DDx</sub>	7		Power	Device power supply. Connect to 1.8V.

V <sub>DDO1</sub>	8		Power	Device power supply. Connect to 1.8 to 3.3V. V <sub>DDO1</sub> must be the highest voltage on the device. Using register settings, select output voltage levels for OUT0–OUT3.
GND	9		Power	Connect to ground.
OUT2	10	O	Adjustable	Configurable clock output 2. Single-ended output voltage levels are register controlled by either V <sub>DDO1</sub> or V <sub>DDO2</sub> .
OUT1	11	O	Adjustable	Configurable clock output 1. Single-ended output voltage levels are register controlled by either V <sub>DDO1</sub> or V <sub>DDO2</sub> .
SEL1*	12	I	LVTTL	Configuration select pin. Weak internal pull-down resistor.
GND	13		Power	Connect to ground.
SCLK	14	I	LVTTL	I <sup>2</sup> C clock. Logic levels set by V <sub>DDO1</sub> . 5V tolerant.
OUT0	15	O	Adjustable	Configurable clock output 0. Single-ended output voltage levels are register controlled by either V <sub>DDO1</sub> or V <sub>DDO2</sub> .
OUT4	16	O	Adjustable	Configurable clock output 8. Single-ended output voltage levels controlled by V <sub>DDO2</sub> .
SDA	17	I/O	Open Drain	Bidirectional I <sup>2</sup> C data. Logic levels set by V <sub>DDO1</sub> . 5V tolerant.
V <sub>DDO2</sub>	18		Power	Device power supply. Connect to 1.8 to 3.3V. Using register settings, select output voltage levels for OUT0–OUT4.
V <sub>DD</sub>	19		Power	Device power supply. Connect to 1.8V.
GND	20		Power	Connect to ground.

Note \*: SEL pins should be controlled by 1.8V LVTTL logic; 3.3V tolerant.

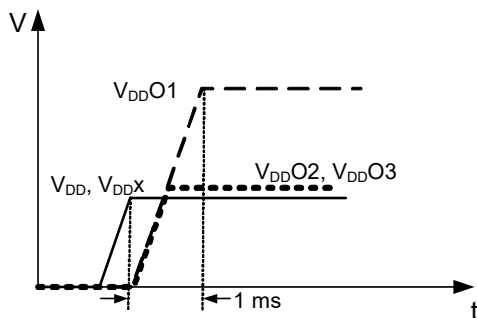
Note 1: Outputs are user programmable to drive single-ended 1.8V/2.5V/3.3V LVTTL as indicated above. Always completely power-up V<sub>DD</sub> and V<sub>DDx</sub> prior to applying V<sub>DDO</sub> power.

Note 2: Default configuration CLK3 = buffered reference output. All other outputs are off.

Note 3: Do not power up with SEL[1:0] = 00 (in Power-down/Sleep mode).

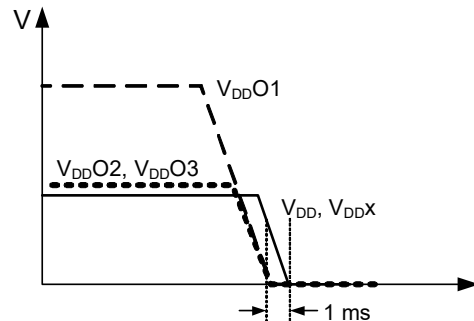
### Ideal Power Up Sequence

- 1) V<sub>DD</sub> and V<sub>DDx</sub> must come up first, followed by V<sub>DDO</sub>
- 2) V<sub>DDO1</sub> must come up within 1ms after V<sub>DD</sub> and V<sub>DDx</sub> come up
- 3) V<sub>DDO2</sub> must be equal to, or lower than, V<sub>DDO1</sub>
- 4) V<sub>DD</sub> and V<sub>DDx</sub> have approx. the same ramp rate
- 5) V<sub>DDO1</sub> and V<sub>DDO2</sub> have approx. same ramp rate



### Ideal Power Down Sequence

- 1) V<sub>DDO</sub> must drop first, followed by V<sub>DD</sub> and V<sub>DDx</sub>
- 2) V<sub>DD</sub> and V<sub>DDx</sub> must come down within 1ms after V<sub>DDO1</sub> comes down
- 3) V<sub>DDO2</sub> must be equal to, or lower than, V<sub>DDO1</sub>
- 4) V<sub>DD</sub> and V<sub>DDx</sub> have approx. the same ramp rate
- 5) V<sub>DDO1</sub> and V<sub>DDO2</sub> have approx. same ramp rate



### Crystal Input (XIN/REF)

The crystal oscillators should be fundamental mode quartz crystals; overtone crystals are not suitable. Crystal frequency should be specified for parallel resonance with 50Ω maximum equivalent series resonance. 0

ONXTALB = 0 bit needs to be set for XIN/REF.

### Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These

capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground.

The crystal capacitors are internal to the device and have an effective value of 4pF.

## Programming the Device

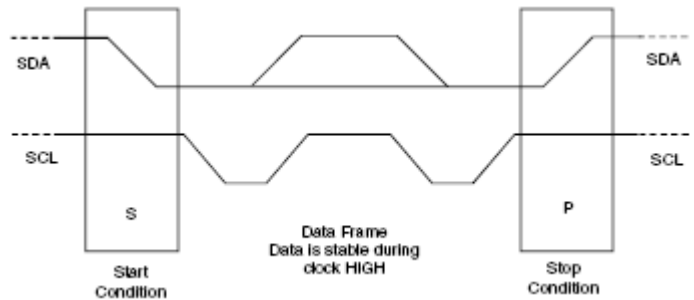
I<sup>2</sup>C may be used to program the 5P49EE502-166.

– Device (slave) address = 7'b1101010

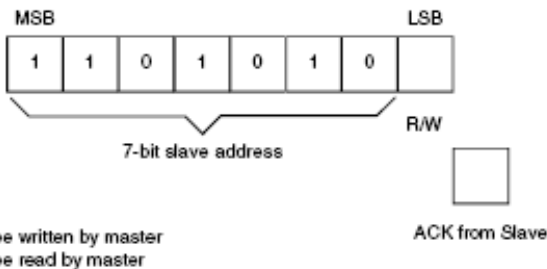
### I<sup>2</sup>C Programming

The 5P49EE502-166 is programmed through an I<sup>2</sup>C-Bus serial interface, and is an I<sup>2</sup>C slave device. The read and write transfer formats are supported. The first byte of data after a write frame to the correct slave address is interpreted as the register address; this address auto-increments after each byte written or read.

The frame formats are shown in the following illustration.



Framing



The first byte transmitted by the Master is the Slave Address followed by the R/W bit. The Slave acknowledges by sending a '1' bit.

### First Byte Transmitted on I<sup>2</sup>C Bus

## External I<sup>2</sup>C Interface Condition

### KEY:

- From Master to Slave
- From Master to Slave, but can be omitted if followed by the correct sequence  
Normally data transfer is terminated by a STOP condition generated by the Master. However, if the Master still wishes to communicate on the bus, it can generate a repeated START condition, and address another Slave address without first generating a STOP condition.
- From Slave to Master

### SYMBOLS:

- ACK - Acknowledge (SDA LOW)
- NACK - Not Acknowledge (SDA HIGH)
- Sr - Repeated Start Condition
- S - START Condition
- P - STOP Condition

## EEPROM Interface

The 5P49EE502-166 can store its configuration in an internal EEPROM. The contents of the device's internal programming registers can be saved to the EEPROM by issuing a save instruction (ProgSave) and can be loaded back to the internal programming registers by issuing a restore instruction (ProgRestore).

To initiate a save or restore using I<sup>2</sup>C, only two bytes are transferred. The Device Address is issued with the read/write bit set to "0", followed by the appropriate command code. The save or restore instruction executes after the STOP condition

is issued by the Master, during which time the 5P49EE502-166 will not generate Acknowledge bits. The 5P49EE502-166 will acknowledge the instructions after it has completed execution of them. During that time, the I<sup>2</sup>C bus should be interpreted as busy by all other users of the bus.

On power-up of the 5P49EE502-166, an automatic restore is performed to load the EEPROM contents into the internal programming registers. The 5P49EE502-166 will be ready to accept a programming instruction once it acknowledges its 7-bit I<sup>2</sup>C address.

## Progwrite

S	Address	R/W	ACK	Command Code	ACK	Register	ACK	Data	ACK	P
	7-bits	0	1-bit	8-bits: xxxxxx00	1-bit	8-bits	1-bit	8-bits	1-bit	

### Progwrite Command Frame

Writes can continue as long as a Stop condition is not sent and each byte will increment the register address.

## Progreed

Note: If the expected read command is not from the next higher register to the previous read or write command, then set a known “read” register address prior to a read operation by issuing the following command:

S	Address	R/W	ACK	Command Code	ACK	Register	ACK	P
	7-bits	0	1-bit	8-bits: xxxxxx00	1-bit	8-bits	1-bit	

### Prior to Progreed Command Set Register Address

The user can ignore the STOP condition above and use a repeated START condition instead, straight after the slave acknowledgment bit (i.e., followed by the Progreed command):

S	Address	R/W	ACK	ID Byte	ACK	Data_1	ACK	Data_2	ACK	Data_last	NACK	P
	7-bits	1	1-bit	8-bits	1-bit	8-bits	1-bit	8-bits	1-bit	8-bits	1-bit	

### Progreed Command Frame

## Progsave

S	Address	R/W	ACK	Command Code	ACK	P
	7-bits	0	1-bit	8-bits: xxxxxx01	1-bit	

Note:

PROGWRITE is for writing to the 5P49EE502-166 registers.

PROGREAD is for reading the 5P49EE502-166 registers.

PROGSAVE is for saving all the contents of the

5P49EE502-166 registers to the EEPROM.

PROGRESTORE is for loading the entire EEPROM contents to the 5P49EE502-166 registers.

## Progrestore

S	Address	R/W	ACK	Command Code	ACK	P
	7-bits	0	1-bit	8-bits: xxxxxx10	1-bit	

During PROGRESTORE, outputs will be turned off to ensure that no improper voltage levels are experienced before initialization.

## I<sup>2</sup>C Bus DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>IH</sub>	Input HIGH Level		0.7xV <sub>DDO1</sub>		5.5	V
V <sub>IL</sub>	Input LOW Level				0.3xV <sub>DDO1</sub>	V
V <sub>HYS</sub>	Hysteresis of Inputs		0.05xV <sub>DDO1</sub>			V
I <sub>IN</sub>	Input Leakage Current				±1.0	µA
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 3 mA			0.4	V

## I<sup>2</sup>C Bus AC Characteristics for Standard Mode<sup>1</sup>

Symbol	Parameter	Min	Typ	Max	Unit
F <sub>SCLK</sub>	Serial Clock Frequency (SCL)	0		100	kHz
t <sub>BUF</sub>	Bus free time between STOP and START	4.7			µs
t <sub>SU:START</sub>	Setup Time, START	4.7			µs
t <sub>HD:START</sub>	Hold Time, START	4			µs
t <sub>SU:DATA</sub>	Setup Time, data input (SDA)	250			ns
t <sub>HD:DATA</sub>	Hold Time, data input (SDA) <sup>2</sup>	0			µs
t <sub>OVD</sub>	Output data valid from clock			3.45	µs
C <sub>B</sub>	Capacitive Load for Each Bus Line			400	pF
t <sub>R</sub>	Rise Time, data and clock (SDAT, SCLK)			1000	ns
t <sub>F</sub>	Fall Time, data and clock (SDAT, SCLK)			300	ns
t <sub>HIGH</sub>	HIGH Time, clock (SCLK)	4			µs
t <sub>LOW</sub>	LOW Time, clock (SCLK)	4.7			µs
t <sub>SU:STOP</sub>	Setup Time, STOP	4			µs

1. No activity is allowed on I<sup>2</sup>C lines until V<sub>DD</sub> > 1.62V.

2. A device must internally provide a hold time of at least 300ns for the SDAT signal (referred to the V<sub>IH</sub>(MIN) of the SCLK signal) to bridge the undefined region of the falling edge of SCLK.

## I<sup>2</sup>C Bus AC Characteristics for Fast Mode<sup>1</sup>

Symbol	Parameter	Min	Typ	Max	Unit
F <sub>SCLK</sub>	Serial Clock Frequency (SCL)	0		400	kHz
t <sub>BUF</sub>	Bus free time between STOP and START	1.3			µs
t <sub>SU:START</sub>	Setup Time, START	0.6			µs
t <sub>HD:START</sub>	Hold Time, START	0.6			µs
t <sub>SU:DATA</sub>	Setup Time, data input (SDA)	100			ns
t <sub>HD:DATA</sub>	Hold Time, data input (SDA) <sup>1</sup>	0			µs
t <sub>OVD</sub>	Output data valid from clock			0.9	µs
C <sub>B</sub>	Capacitive Load for Each Bus Line			400	pF
t <sub>R</sub>	Rise Time, data and clock (SDA, SCL)	20 + 0.1xC <sub>B</sub>		300	ns
t <sub>F</sub>	Fall Time, data and clock (SDA, SCL)	20 + 0.1xC <sub>B</sub>		300	ns
t <sub>HIGH</sub>	HIGH Time, clock (SCL)	0.6			µs
t <sub>LOW</sub>	LOW Time, clock (SCL)	1.3			µs
t <sub>SU:STOP</sub>	Setup Time, STOP	0.6			µs

1. No activity is allowed on I<sup>2</sup>C lines until V<sub>DD</sub> > 1.62V.

2. A device must internally provide a hold time of at least 300ns for the SDAT signal (referred to the V<sub>IH</sub>(MIN) of the SCLK signal) to bridge the undefined region of the falling edge of SCLK.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 5P49EE502-166. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Symbol	Description	Min	Max	Unit
$V_{DD}$	Internal Power Supply Voltage	-0.5	4.6	V
$V_I$	Input Voltage <sup>1</sup>	-0.5	4.6	V
$V_O$	Output Voltage (not to exceed 4.6 V) <sup>1</sup>	-0.5	$V_{DD}+0.5$	V
$T_J$	Junction Temperature		150	°C
$T_{STG}$	Storage Temperature	-65	150	°C

1. Input negative and output voltage ratings may be exceeded if the input and output current ratings are observed.

## Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
$V_{DD}$	Power supply voltage for $V_{DD}$ pins supporting core and outputs	1.71	1.8	1.89	V
$V_{DDX}$	Power supply voltage for crystal oscillator. Use filtered analog power supply if available.	1.71	1.8	1.89	V
$V_{DDOX}$	3.3V $V_{DDO}$ Range	3.14	3.3	3.47	V
$T_A$	Operating temperature, ambient	-40		+85	°C
$C_{LOAD\_OUT}$	Maximum load capacitance (3.3V LVTTTL only)			15	pF
$F_{IN}$	External reference crystal		25		MHz
	External reference clock CLKIN		25		MHz
$t_{PU}$	Power-up time for all $V_{DD}$ s to reach minimum specified voltage (power ramps must be monotonic)	0.05		5	ms

## Capacitance ( $T_A = +25\text{ °C}$ , $f = 1\text{ MHz}$ )

Symbol	Parameter	Min	Typ	Max	Unit
$C_{IN}$	Input Capacitance (CLKIN, SDA, SCL, SEL[2:0])		3	7	pF
Pull-down Resistor	CLKIN, SEL[2:0]		180		k $\Omega$

## Crystal Specifications

XTAL_FREQ	Crystal frequency		25		MHz
XTAL_MIN	Minimum crystal load capacitance	3.5			pF
XTAL_MAX	Maximum crystal load capacitance			35.5	pF
XTAL_V <sub>PP</sub>	Voltage swing (peak-to-peak, nominal)	1.5	2.3	3.2	V



## DC Electrical Characteristics for $V_{DDOx} = 3.3V$ LVTTL <sup>1</sup>

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{OH}$	Output HIGH Voltage		2.4		$V_{DDO}$	V
$V_{OL}$	Output LOW Voltage				0.4	V
$I_{OZDD}$	Output Leakage Current	3-state outputs. $V_O = V_{DDOx}$ or GND.			10	$\mu A$

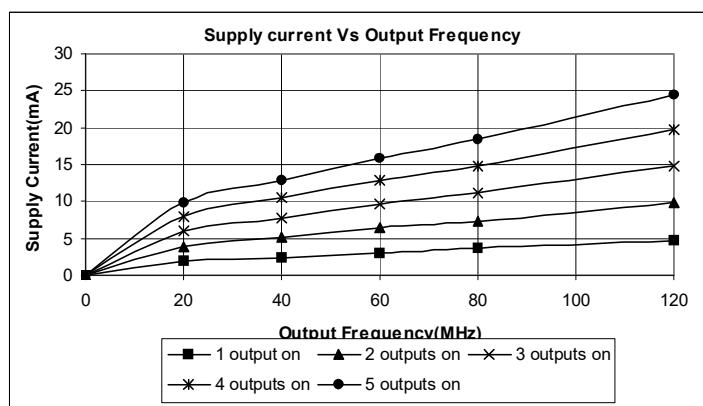
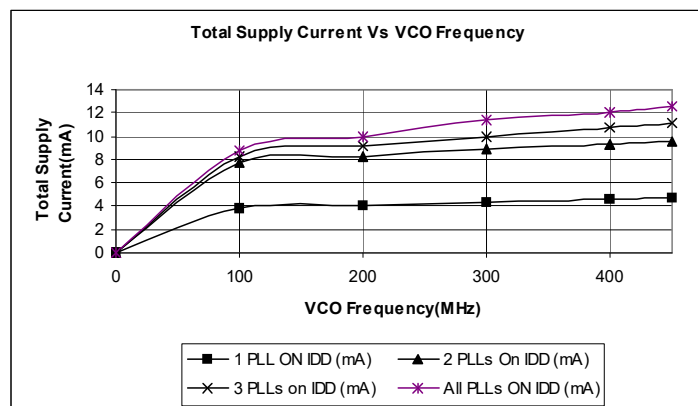
Note 1: See "Recommended Operating Conditions" table. Always completely power up  $V_{DD}$  and  $V_{DDx}$  before applying  $V_{DDO}$ .

## DC Current Consumption <sup>1</sup>

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$I_{DDO1}$	Current for $V_{DDO1}$ Pin	$V_{DDO1} = 3.3V$ .			25	mA
$I_{DDO2}$	Current for $V_{DDO2}$ Pin	$V_{DDO2} = 3.3V$ .			5	mA
$I_{DD}$	Current for $V_{DD}$ Pin	$V_{DD} = 1.8V$ .			15	mA
$I_{DDx}$	Current for $V_{DDx}$ Pin	$V_{DDx} = 1.8V$ .			5	mA
$I_{DDPD}$	Power Down Current	SEL[1:0] = 00, total current			100	$\mu A$

Note 1: See "Recommended Operating Conditions" table. Always completely power up  $V_{DD}$  and  $V_{DDx}$  before applying  $V_{DDO}$ .

## Power Supply Characteristics for LVTTL Outputs



1. See "Recommended Operating Conditions" table. Always completely power-up  $V_{DD}$  and  $V_{DDx}$  prior to applying  $V_{DDO}$  power.

## AC Timing Electrical Characteristics – All Outputs and Inputs

(Spread spectrum generation = Off)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$f_{IN}^1$	Input Frequency	Input frequency limit (CLKIN)		25		MHz
		Input frequency limit (XIN/REF)		25		MHz
t2	Input Duty Cycle	Duty Cycle for input	40		60	%
t3	Output Duty Cycle	Measured at $V_{DDO}/2$ , all outputs except Reference output	45		55	%
		Measured at $V_{DDO}/2$ , Reference output	40		60	%
$t_R$	Rise Time	20% to 80% (measured with 5pF), $V_{DDO} = 3.3V \pm 5\%$		550	1000	ps
$t_F$	Fall Time	80% to 20% (measured with 5pF), $V_{DDO} = 3.3V \pm 5\%$		550	1000	ps

## AC Timing Electrical Characteristics – OUT0–4

(Spread spectrum generation = Off)

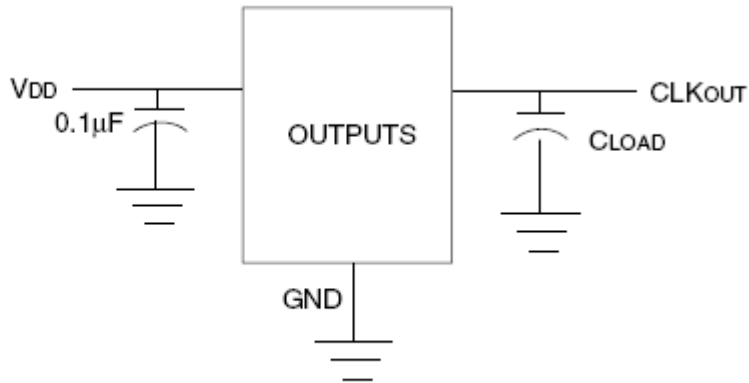
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
t4 <sup>2</sup>	Slew Rate, SLEW[1:0] = 10	Output clock slew rate, 20% to 80% of V <sub>DD0</sub> = 3.3V (Output Load = 5pF)		3.7		V/ns
t5 <sup>3</sup>	Clock Jitter	Peak-to-peak period jitter			200	ps
t6	Output Skew	Skew between output to output on the same bank			75	ps

## AC Timing Electrical Characteristics – PLL Lock Time

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
t7 <sup>4</sup>	Lock Time	PLL lock time from power-up		10	20	ms
t8	Lock Time	PLL lock time from exiting shutdown mode			2	ms

1. Practical lower frequency is determined by loop filter settings.
2. A slew rate of 2.75V/ns or greater should be selected for output frequencies of 100MHz or higher.
3. Max value represents worst case configuration. Typical value represents average across all configurations.
4. Includes loading the configuration bits from EEPROM to PLL registers. It does not include EEPROM programming/write time.

## Test Circuits and Conditions <sup>1</sup>

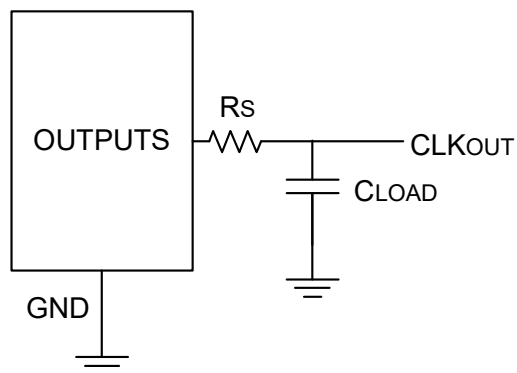


**NOTE:**

1. All V<sub>CC</sub> pins must be tied together.

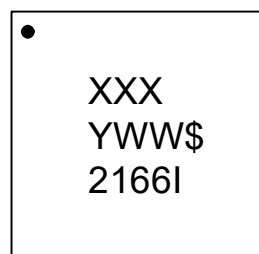
Test Circuits for DC Outputs

## Termination Scheme (Block Diagram)



LVTTL output load: ~7pF for each output.

## Marking Diagram



Notes:

- “XXX” is the last three characters of the Asm lot.
- “YWW” is the last digit of the year and week that the part was assembled.
- “\$” is the mark code.
- Line 3 is the truncated part number.
- “I” at the end of part number indicates industrial temperature range.

## Thermal Characteristics 20-VFQFPN

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	$\theta_{JA}$	Still air.		64		°C/W
	$\theta_{JA}$	1 m/s air flow.		56.6		°C/W
	$\theta_{JA}$	3 m/s air flow.		51.8		°C/W
Thermal Resistance Junction to Case	$\theta_{JC}$			84.3		°C/W

## Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

[www.renesas.com/us/en/document/psc/20-vfqfpn-package-outline-drawing30-x-30-x-090-mm-040mm-pitch-165-x-165-mm-epadndg20p2](http://www.renesas.com/us/en/document/psc/20-vfqfpn-package-outline-drawing30-x-30-x-090-mm-040mm-pitch-165-x-165-mm-epadndg20p2)

## Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
5P49EE502-166NDGI	Trays	3 x 3 mm 20-VFQFPN	-40° to +85° C
5P49EE502-166NDGI8	Reel	3 x 3 mm 20-VFQFPN	-40° to +85° C

“G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

## Revision History

Date	Description of Change
May 10, 2019	<ul style="list-style-type: none"> <li>Updated Rise/Fall Time specifications in “AC Timing Electrical Characteristics – All Outputs and Inputs” table.</li> <li>Updated Slew Rate specifications in “AC Timing Electrical Characteristics – OUT0–4” table.</li> </ul>
November 14, 2017	Initial release.





RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Sept 13, 2018	Rev 01	Change QFN to VFQFPN
Mar 30, 2016	Rev 00	Initial Release

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