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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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6AM12

Silicon N-Channel/P-Channel Complementary Power MOS FET Array



ADE-208-1216 (Z)
1st. Edition
Mar. 2001

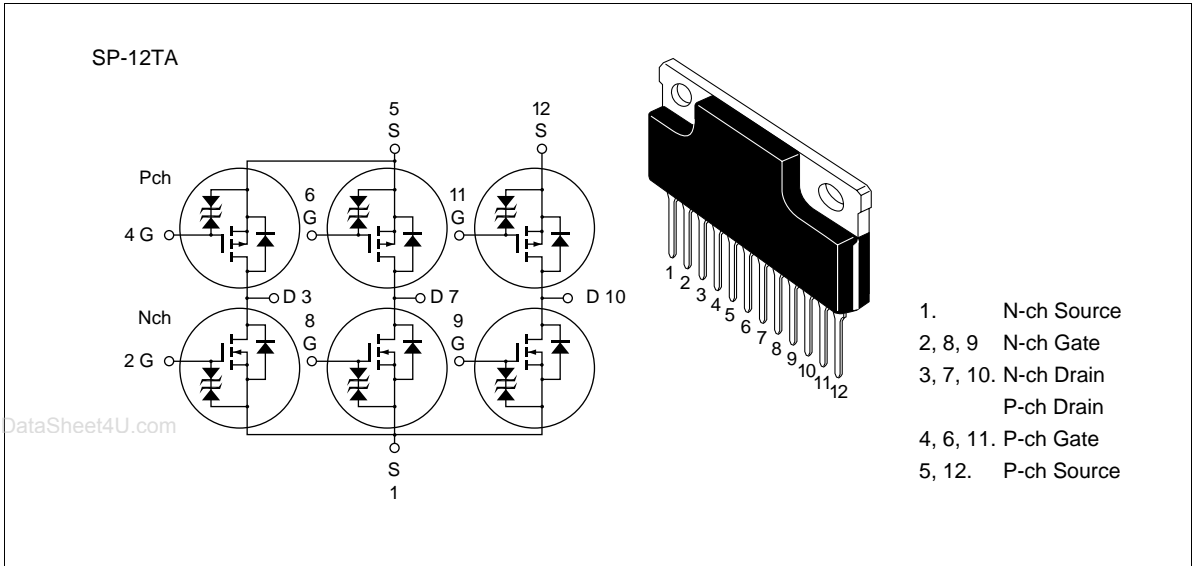
Application

High speed power switching

Features

- Low on-resistance
N-channel: $R_{DS(on)} \leq 0.17$, $V_{GS} = 10$ V, $I_D = 4$ A
P-channel: $R_{DS(on)} \leq 0.2$, $V_{GS} = -10$ V, $I_D = -4$ A
- Capable of 4 V gate drive
- Low drive current
- High speed switching
- High density mounting
- Suitable for H-bridged motor driver

Outline



Absolute Maximum Ratings (T_a = 25°C)

Item	Symbol	Ratings		Unit
		Nch	Pch	
Drain to source voltage	V _{DSS}	60	-60	V
Gate to source voltage	V _{GSS}	±20	±20	V
Drain current	I _D	7	-7	A
Drain peak current	I _{D(pulse)} ^{*1}	28	-28	A
Body to drain diode reverse drain current	I _{DR}	7	-7	A
Channel dissipation	Pch (T _c = 25°C) ^{*2}	42		W
Channel dissipation	Pch ^{*2}	4.8		W
Channel temperature	T _{ch}	150		°C
Storage temperature	T _{stg}	-55 to +150		°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%

2. 6 devices operation

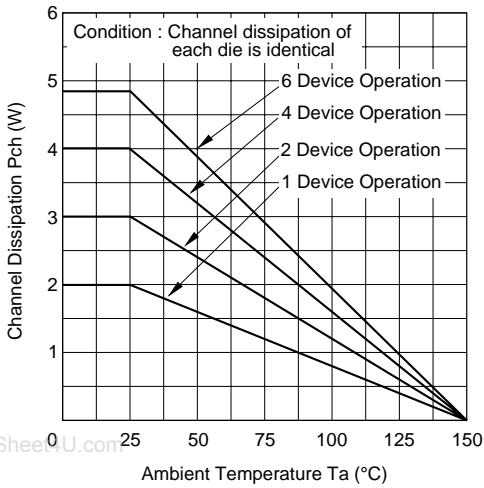
Electrical Characteristics (Ta = 25°C) (1 Unit)

Item	Symbol	N channel			P channel			Unit	Test conditions
		Min	Typ	Max	Min	Typ	Max		
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	-60	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	± 20	—	—	V	$I_G = \pm 100 \mu\text{A}, V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	250	—	—	-250	μA	$V_{DS} = 50 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	-1.0	—	-2.0	V	$I_D = 1 \text{ mA}, V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.13	0.17	—	0.15	0.2		$I_D = 4 \text{ A}, V_{GS} = 10 \text{ V}^{*1}$
		—	0.19	0.24	—	0.20	0.27		$I_D = 4 \text{ A}, V_{GS} = 4 \text{ V}^{*1}$
Forward transfer admittance	$ y_{fs} $	3.5	5.5	—	3.5	6.0	—	S	$I_D = 4 \text{ A}, V_{DS} = 10 \text{ V}^{*1}$
Input capacitance	C_{iss}	—	400	—	—	900	—	pF	$V_{DS} = 10 \text{ V}, V_{GS} = 0$
Output capacitance	C_{oss}	—	220	—	—	460	—	pF	$f = 1 \text{ MHz}$
Reverse transfer capacitance	C_{rss}	—	60	—	—	130	—	pF	
Turn-on delay time	$t_{d(on)}$	—	5	—	—	8	—	ns	$I_D = 4 \text{ A}, V_{GS} = 10 \text{ V},$
Rise time	t_r	—	45	—	—	50	—	ns	$R_L = 7.5$
Turn-off delay time	$t_{d(off)}$	—	150	—	—	170	—	ns	
Fall time	t_f	—	80	—	—	95	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.1	—	—	-1.05	—	V	$I_F = 7 \text{ A}, V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	110	—	—	180	—	ns	$I_F = 7 \text{ A}, V_{GS} = 0,$ $dI_F/dt = 50 \text{ A}/\mu\text{s}$

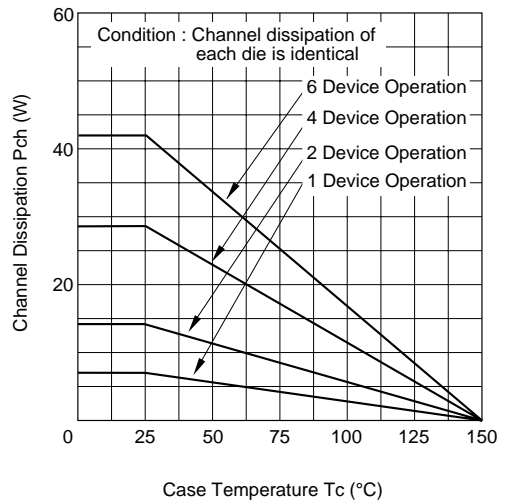
Note: 1. Pulse Test

Polarity of test conditions for P channel device is reversed.

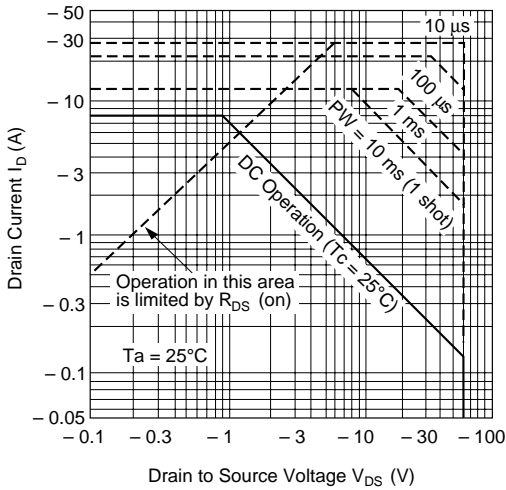
Maximum Channel Dissipation Curve



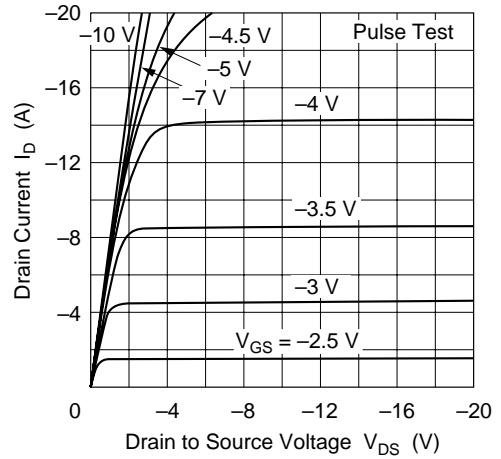
Maximum Channel Dissipation Curve

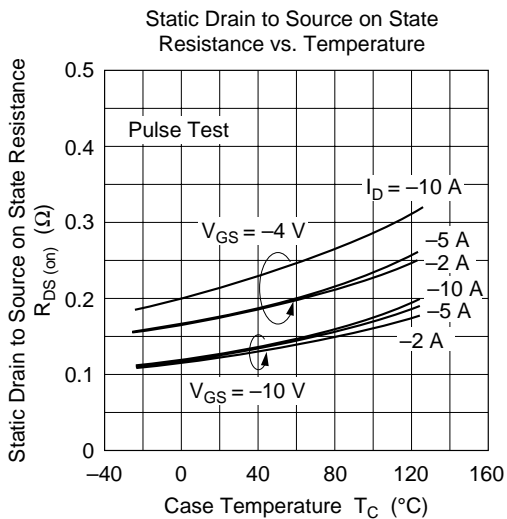
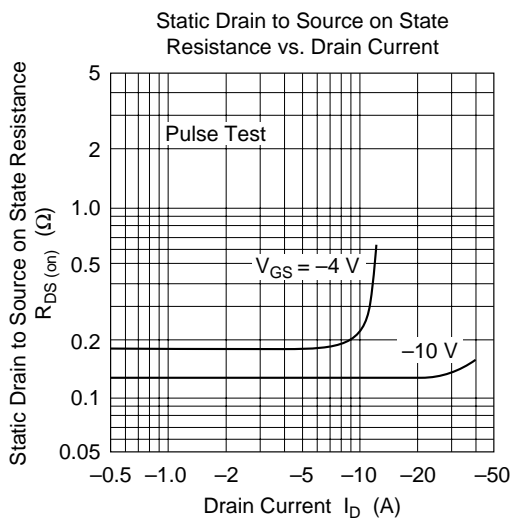
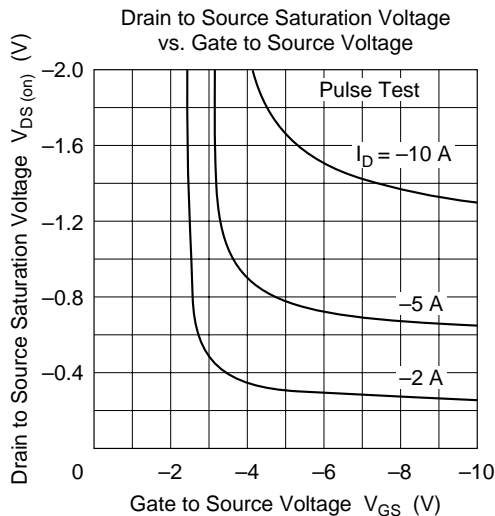
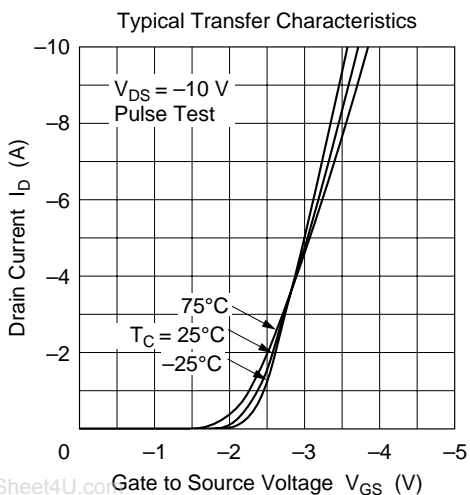


Maximum Safe Operation Area (P-Channel)

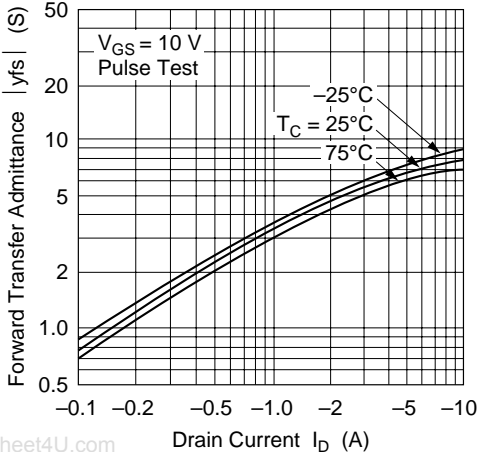


Typical Output Characteristics

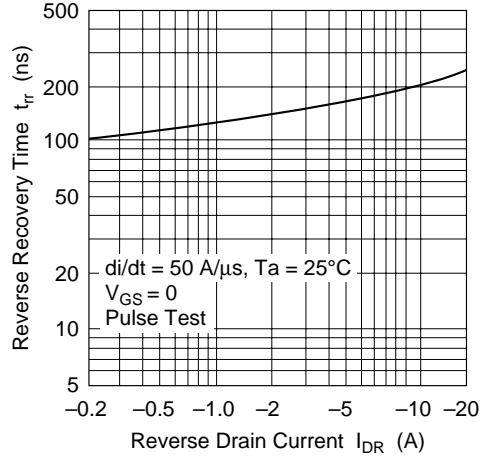




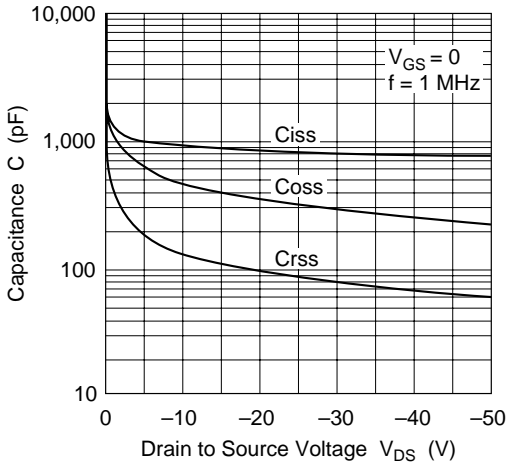
Forward Transfer Admittance vs. Drain Current



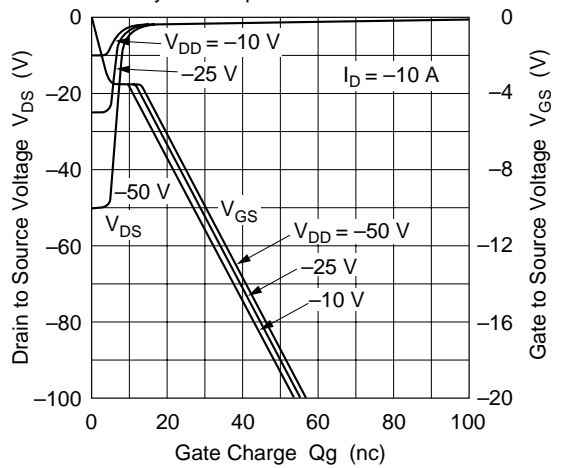
Body to Drain Diode Reverse Recovery Time

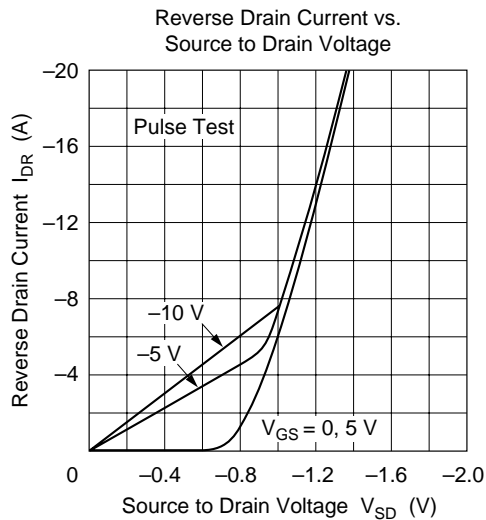
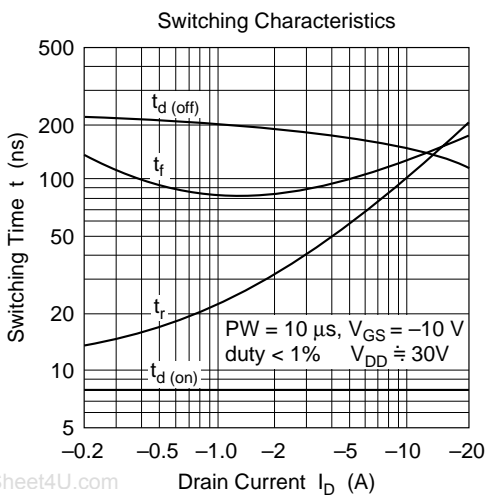


Typical Capacitance vs. Drain to Source Voltage



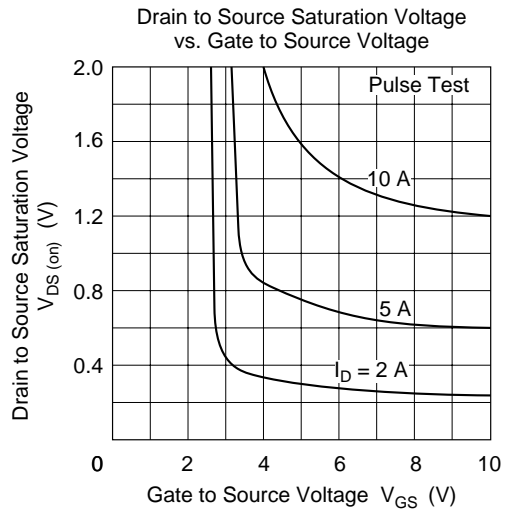
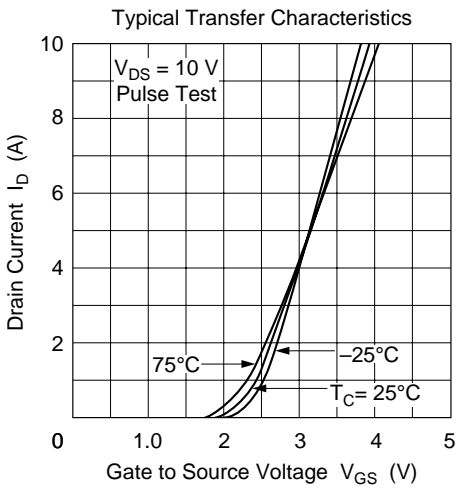
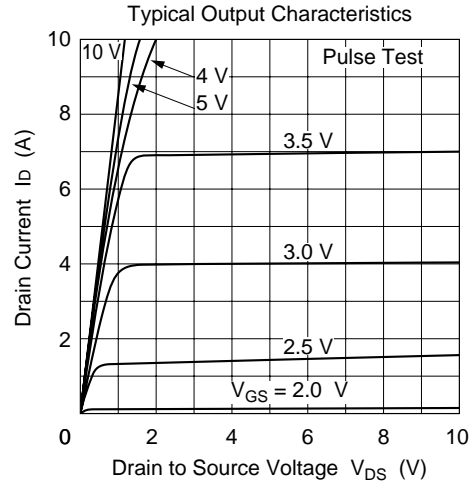
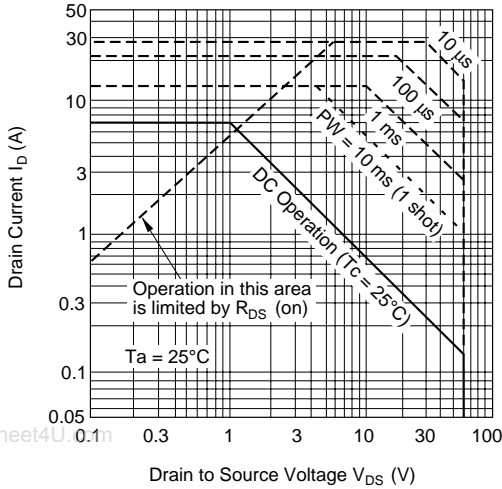
Dynamic Input Characteristics

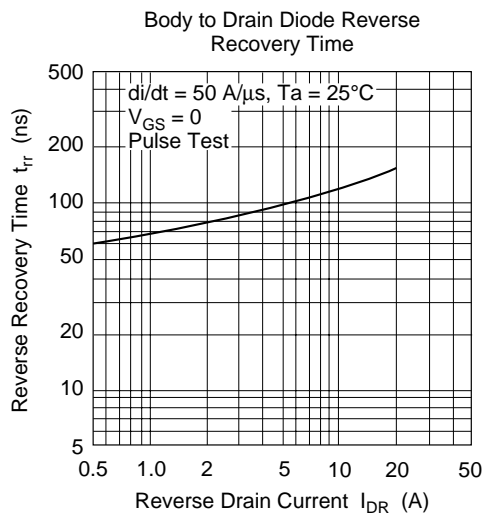
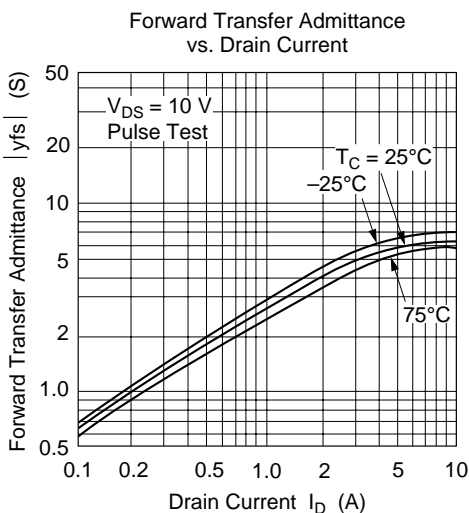
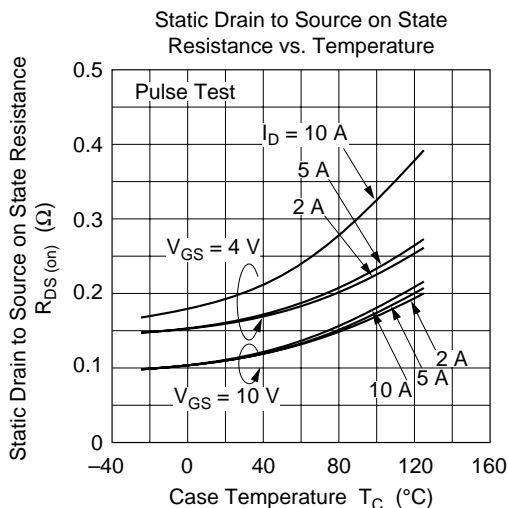
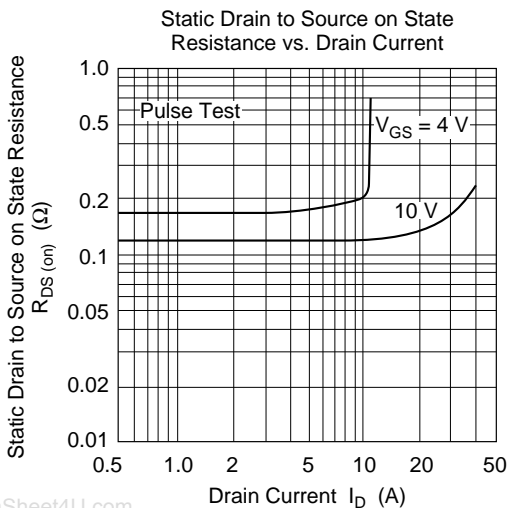




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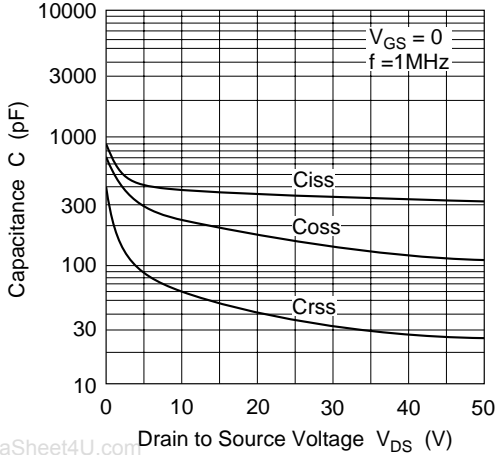
Maximum Safe Operation Area (N-Channel)



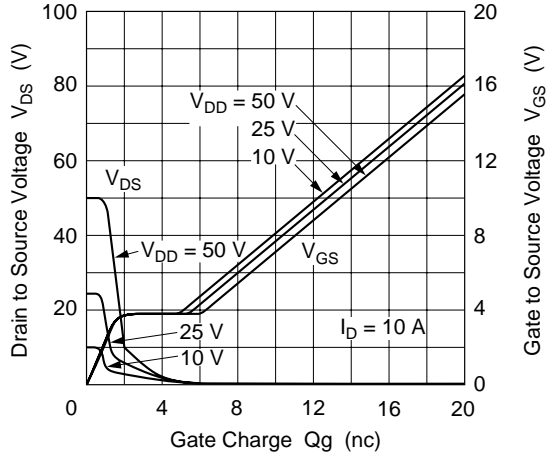


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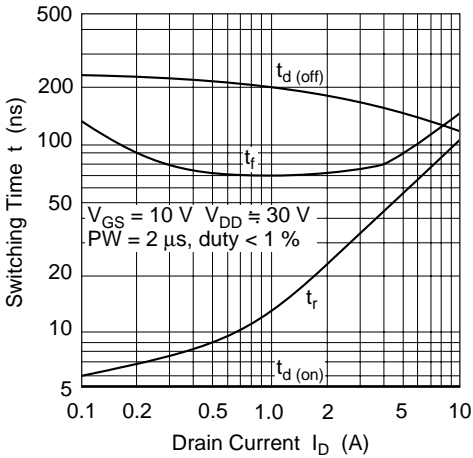
Typical Capacitance vs. Drain to Source Voltage



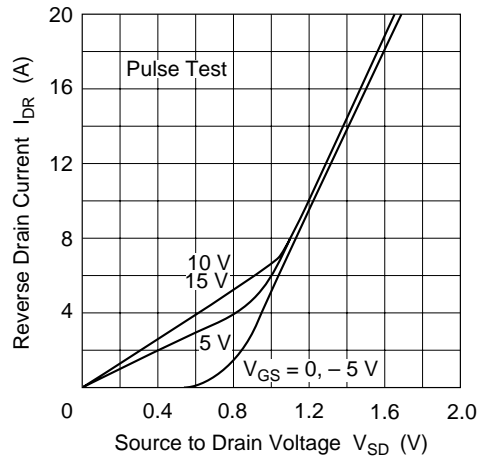
Dynamic Input Characteristics



Switching Characteristics



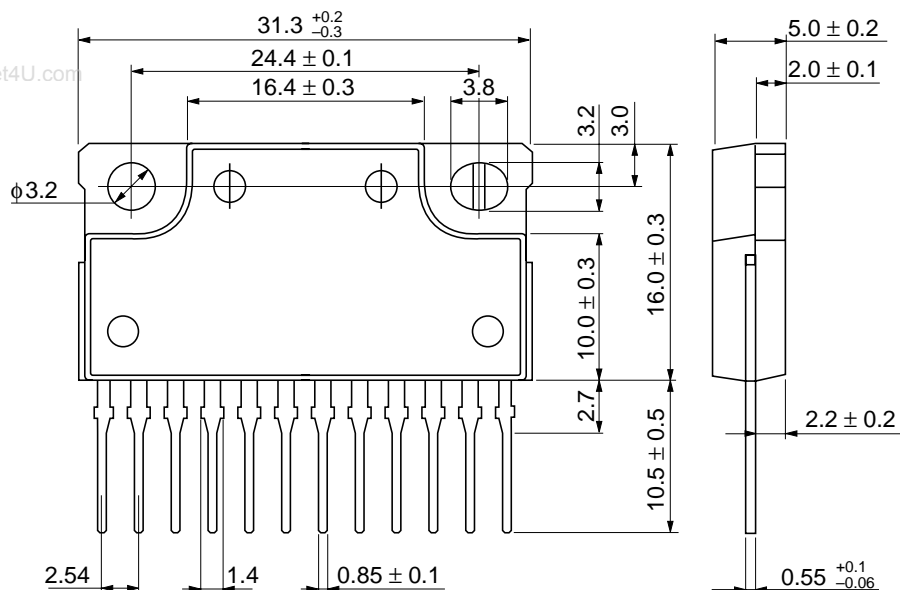
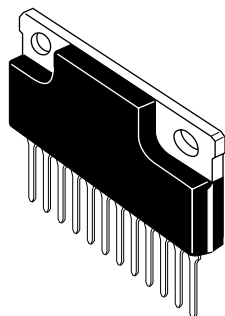
Reverse Drain Current vs. Source to Drain Voltage



Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	SP-12TA
JEDEC	—
EIAJ	—
Mass (reference value)	6.1 g

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