

**PERIPHERAL DRIVERS FOR  
HIGH-VOLTAGE, HIGH-CURRENT DRIVER APPLICATIONS**

**performance**

- Characterized for Use to 300 mA
- High-Voltage Outputs
- No Output Latch-Up at 30 V (After Conducting 300 mA)
- Medium-Speed Switching

**ease-of-design**

- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL- or DTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- Available in Plastic and Ceramic Packages

**SUMMARY OF SERIES 55460/75460**

DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGES
SN55460	AND <sup>†</sup>	J
SN55461	AND	JG
SN55462	NAND	JG
SN55463	OR	JG
SN55464	NOR	JG
SN75460	AND <sup>†</sup>	J, N
SN75461	AND	JG, P
SN75462	NAND	JG, P
SN75463	OR	JG, P
SN75464	NOR	JG, P

<sup>†</sup>With output transistor base connected externally to output of gate.

**description**

Series 55460/75460 dual peripheral drivers are functionally interchangeable with Series 55450B/75450B and Series 55460/75460 peripheral drivers, but are designed for use in systems that require higher breakdown voltages than either of those series can provide at the expense of slightly slower switching speeds. Typical applications include logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers. Series 55460 drivers are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ; Series 75460 drivers are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

The SN55460 and SN75460 are unique general-purpose devices each featuring two standard Series 54/74 TTL gates and two uncommitted, high-current, high-voltage, n-p-n transistors. These devices offer the system designer the flexibility of tailoring the circuit to the application.

The SN55461/SN75461, SN55462/SN75462, SN55463/SN75463, and SN55464/SN75464 are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic) with the output of the gates internally connected to the bases of the n-p-n output transistors.

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# SERIES 55460/75460

## DUAL PERIPHERAL DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN55460	SN55461 SN55462 SN55463 SN55464	SN75460	SN75461 SN75462 SN75463 SN75464	UNIT
Supply voltage, $V_{CC}$ (see Note 1)	7	7	7	7	V
Input voltage	5.5	5.5	5.5	5.5	V
Interemitter voltage (see Note 2)	5.5	5.5	5.5	5.5	V
$V_{CC}$ -to-substrate voltage	40		40		V
Collector-to-substrate voltage	40		40		V
Collector-base voltage	40		40		V
Collector-emitter voltage (see Note 3)	40		40		V
Collector-emitter voltage (see Note 4)	25		25		V
Emitter-base voltage	5		5		V
Off-state output voltage		35		35	V
Continuous collector or output current (see Note 5)	400	400	400	400	mA
Peak collector or output current ( $t_w \leq 10$ ms, duty cycle $\leq 50\%$ , see Note 5)	500	500	500	500	mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 6)	J package	1375	1025		mW
	JG package			825	
	N package		1150		
	P package			1000	
Operating free-air temperature range	-55 to 125	-55 to 125	0 to 70	0 to 70	°C
Storage temperature range	-65 to 150	-65 to 150	-65 to 150	-65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J or JG package		300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P package		260	260	°C

- NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise specified.  
 2. This is the voltage between two emitters of a multiple emitter transistor.  
 3. This value applies when the base-emitter resistance ( $R_{BE}$ ) is equal to or less than 500  $\Omega$ .  
 4. This value applies between 0 and 10 mA collector current when the base-emitter diode is open-circuited.  
 5. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.  
 6. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 11. In the J and JG packages, SN55460 through SN55464 chips are alloy-mounted; SN75460 through SN75464 chips are glass-mounted.

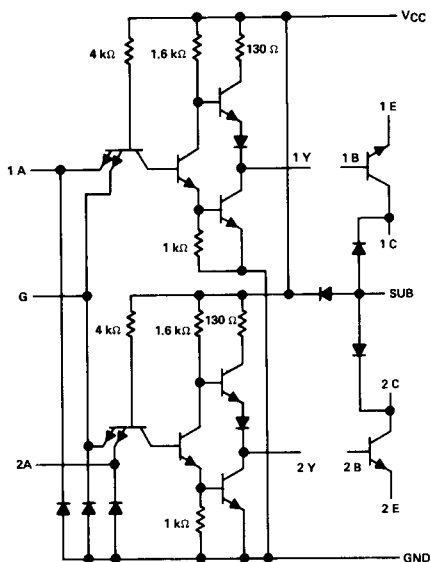
recommended operating conditions (see Note 7)

	SERIES 55460			SERIES 75460			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, $T_A$	-55		125	0	70		°C

NOTE 7: For SN55460 and SN75460 only, the substrate (pin 8) must always be at the most negative device voltage for proper operation.

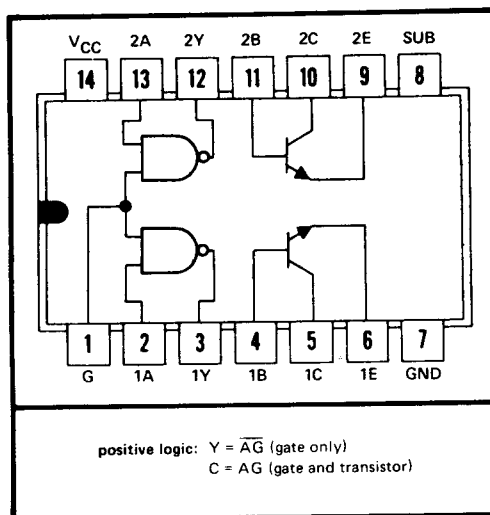
# TYPES SN55460, SN75460 DUAL PERIPHERAL POSITIVE-AND DRIVERS

schematic



Resistor values shown are nominal.

SN55460...J  
SN75460...J OR N  
DUAL-IN-LINE PACKAGE (TOP VIEW)



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

### TTL gates

PARAMETER	TEST CONDITIONS†	SN55460			SN75460			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IH</sub> High-level input voltage		2			2			V
V <sub>IL</sub> Low-level input voltage				0.8			0.8	V
V <sub>IK</sub> Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA	-1.2		-1.5	-1.2		-1.5	V
V <sub>OH</sub> High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -400 μA	2.4	3.3		2.4	3.3		V
V <sub>OL</sub> Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OL</sub> = 16 mA		0.25	0.5		0.25	0.4	V
I <sub>I</sub> Input current at maximum input voltage	input A			1			1	mA
	input G			2			2	
I <sub>IH</sub> High-level input current	input A			40			40	μA
	input G			80			80	
I <sub>IL</sub> Low-level input current	input A			-1.6			-1.6	mA
	input G			-3.2			-3.2	
I <sub>OS</sub> Short-circuit output current§	V <sub>CC</sub> = MAX	-18	-35	-55	-18	-35	-55	mA
I <sub>CCH</sub> Supply current, outputs high	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0		2.8	4		2.8	4	mA
I <sub>CCL</sub> Supply current, outputs low	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5 V		7	11		7	11	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time.

# TYPES SN55460, SN75460

## DUAL PERIPHERAL POSITIVE-AND DRIVERS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

### output transistors

PARAMETER	TEST CONDITIONS†	SN55460		SN75460		UNIT	
		MIN	TYP‡	MAX	MIN		TYP‡
V(BR)CBO Collector-Base Breakdown Voltage	I <sub>C</sub> = 100 μA, I <sub>E</sub> = 0	40			40		V
V(BR)CEO Collector-Emitter Breakdown Voltage	I <sub>C</sub> = 10 mA, I <sub>B</sub> = 0, See Note 8	25			25		V
V(BR)CER Collector-Emitter Breakdown Voltage	I <sub>C</sub> = 100 μA, R <sub>BE</sub> = 500 Ω	40			40		V
V(BR)EBO Emitter-Base Breakdown Voltage	I <sub>E</sub> = 100 μA, I <sub>C</sub> = 0	5			5		V
h <sub>FE</sub> Static Forward Current Transfer Ratio	V <sub>CE</sub> = 3 V, I <sub>C</sub> = 100 mA, T <sub>A</sub> = 25°C	See Note 8	25		25		
	V <sub>CE</sub> = 3 V, I <sub>C</sub> = 300 mA, T <sub>A</sub> = 25°C		30		30		
	V <sub>CE</sub> = 3 V, I <sub>C</sub> = 100 mA, T <sub>A</sub> = MIN		10		20		
	V <sub>CE</sub> = 3 V, I <sub>C</sub> = 300 mA, T <sub>A</sub> = MIN		15		25		
V <sub>BE</sub> Base-Emitter Voltage	I <sub>B</sub> = 10 mA, I <sub>C</sub> = 100 mA	See Note 8	0.85	1.2	0.85	1	V
	I <sub>B</sub> = 30 mA, I <sub>C</sub> = 300 mA	See Note 8	1	1.4	1	1.2	
V <sub>CE(sat)</sub> Collector-Emitter Saturation Voltage	I <sub>B</sub> = 10 mA, I <sub>C</sub> = 100 mA	See Note 8	0.25	0.5	0.25	0.4	V
	I <sub>B</sub> = 30 mA, I <sub>C</sub> = 300 mA	See Note 8	0.45	0.8	0.45	0.7	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

NOTE 8: These parameters must be measured using pulse techniques. t<sub>w</sub> = 300 μs, duty cycle ≤ 2%.

### switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

#### TTL gates

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub> Propagation delay time, low-to-high-level output	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 400 Ω, See Figure 1		22		ns
t <sub>PHL</sub> Propagation delay time, high-to-low-level output			8		ns

#### output transistors

PARAMETER	TEST CONDITIONS‡	MIN	TYP	MAX	UNIT	
t <sub>d</sub> Delay time	I <sub>C</sub> = 200 mA, I <sub>B(1)</sub> = 20 mA, I <sub>B(2)</sub> = -40 mA, V <sub>BE(off)</sub> = -1 V, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 50 Ω, See Figure 2		10		ns	
t <sub>r</sub> Rise time			16		ns	
t <sub>s</sub> Storage time				23		ns
t <sub>f</sub> Fall time				14		ns

‡Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

#### gates and transistors combined

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub> Propagation delay time, low-to-high-level output	I <sub>C</sub> ≈ 200 mA, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 50 Ω, See Figure 3		45	65	ns
t <sub>PHL</sub> Propagation delay time, high-to-low-level output			35	50	ns
t <sub>TLH</sub> Transition time, low-to-high-level output			10	20	ns
t <sub>THL</sub> Transition time, high-to-low-level output			10	20	ns
V <sub>OH</sub> High-level output voltage after switching	V <sub>S</sub> = 30 V, I <sub>C</sub> ≈ 300 mA, R <sub>BE</sub> = 500 Ω, See Figure 4	V <sub>S</sub> -10			mV

# TYPES SN55461, SN75461 DUAL PERIPHERAL POSITIVE-AND DRIVERS

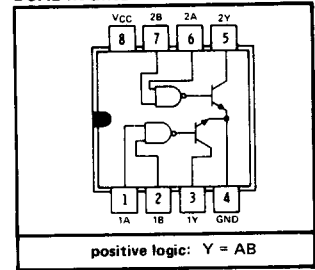
logic

FUNCTION TABLE  
(EACH DRIVER)

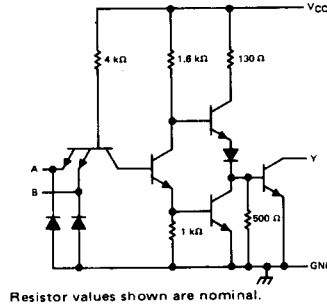
A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

H = high level, L = low level

SN55461 . . . JG  
SN75461 . . . JG OR P  
DUAL-IN-LINE PACKAGE (TOP VIEW)



schematic (each driver)



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN55461		SN75461		UNIT		
		MIN	TYP‡	MAX	MIN		TYP‡	MAX
V <sub>IH</sub>	High-level input voltage	2			2		V	
V <sub>IL</sub>	Low-level input voltage			0.8		0.8	V	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA		-1.2	-1.5	-1.2	-1.5	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>OH</sub> = 35 V		300		100	μA	
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 100 mA		0.25	0.5	0.25	0.4	V
		V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 300 mA		0.5	0.8	0.5	0.7	
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V		1		1	mA	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V		40		40	μA	
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V		-1		-1	-1.6	mA
I <sub>CCH</sub>	Supply current, outputs high	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5 V		8	11	8	11	mA
I <sub>CCL</sub>	Supply current, outputs low	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0		56	76	56	76	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low-to-high-level output		30	55	ns
t <sub>PHL</sub>	Propagation delay time, high-to-low-level output	I <sub>O</sub> ≈ 200 mA, C <sub>L</sub> = 15 pF, R <sub>L</sub> = 50 Ω, See Figure 3	25	40	ns
t <sub>TLH</sub>	Transition time, low-to-high-level output		8	20	ns
t <sub>THL</sub>	Transition time, high-to-low-level output		10	20	ns
V <sub>OH</sub>	High-level output voltage after switching		V <sub>S</sub> = 30 V, See Figure 4	I <sub>O</sub> ≈ 300 mA, V <sub>S</sub> -10	

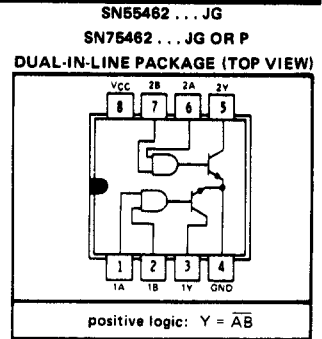
# TYPES SN55462, SN75462 DUAL PERIPHERAL POSITIVE-NAND DRIVERS

logic

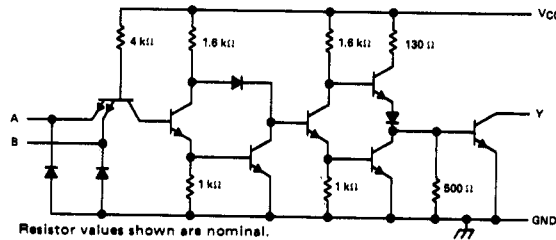
FUNCTION TABLE  
(EACH DRIVER)

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

H = high level, L = low level



schematic (each driver)



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN55462			SN75462			UNIT
		MIN	TYP <sup>†</sup>	MAX	MIN	TYP <sup>‡</sup>	MAX	
$V_{IH}$ High-level input voltage		2		0.8	2		0.8	V
$V_{IL}$ Low-level input voltage							0.8	V
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}$ , $I_I = -12 \text{ mA}$	-1.2	-1.5		-1.2	-1.5		V
$I_{OH}$ High-level output current	$V_{CC} = \text{MIN}$ , $V_{OH} = 35 \text{ V}$ , $V_{IL} = 0.8 \text{ V}$		300			100		$\mu\text{A}$
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $I_{OL} = 100 \text{ mA}$	0.25	0.5		0.25	0.4		V
	$V_{CC} = \text{MIN}$ , $V_{IH} = 2 \text{ V}$ , $I_{OL} = 300 \text{ mA}$	0.5	0.8		0.5	0.7		
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}$ , $V_I = 5.5 \text{ V}$		1			1		$\text{mA}$
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}$ , $V_I = 2.4 \text{ V}$		40			40		$\mu\text{A}$
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$		-1.1	-1.6		-1.1	-1.6	$\text{mA}$
$I_{CCH}$ Supply current, outputs high	$V_{CC} = \text{MAX}$ , $V_I = 0 \text{ V}$		13	17		13	17	$\text{mA}$
$I_{CCL}$ Supply current, outputs low	$V_{CC} = \text{MAX}$ , $V_I = 5 \text{ V}$		61	76		61	76	$\text{mA}$

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ \text{C}$ .

switching characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ \text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ Propagation delay time, low-to-high-level output	$I_O \approx 200 \text{ mA}$ , $C_L = 15 \text{ pF}$ , $R_L = 50 \Omega$ , See Figure 3	45	65		ns
$t_{PHL}$ Propagation delay time, high-to-low-level output		30	50		ns
$t_{TLH}$ Transition time, low-to-high-level output		13	25		ns
$t_{THL}$ Transition time, high-to-low-level output		10	20		ns
$V_{OH}$ High-level output voltage after switching	$V_S = 30 \text{ V}$ , See Figure 4	$V_S - 10$			mV

# TYPES SN55463, SN75463 DUAL PERIPHERAL POSITIVE-OR DRIVERS

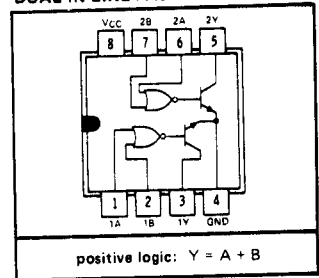
logic

FUNCTION TABLE  
(EACH DRIVER)

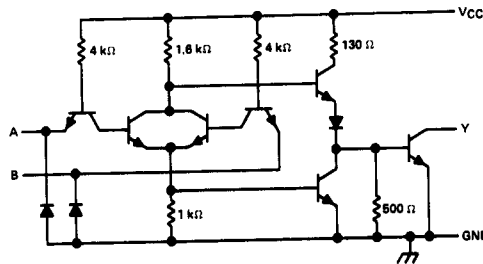
A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

H = high level, L = low level

SN55463 ... JG  
SN75463 ... JG OR P  
DUAL-IN-LINE PACKAGE (TOP VIEW)



schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN55463			SN75463			UNIT	
		MIN	TYP‡	MAX	MIN	TYP‡	MAX		
$V_{IH}$ High-level input voltage		2			2			V	
$V_{IL}$ Low-level input voltage				0.8			0.8	V	
$V_{IK}$ Input clamp voltage				-1.2	-1.5		-1.2	-1.5	V
$I_{OH}$ High-level output current	$V_{CC} = \text{MIN}$ , $V_{OH} = 3.5 \text{ V}$			300			100	$\mu\text{A}$	
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OL} = 100 \text{ mA}$		0.25	0.5		0.25	0.4	V	
	$V_{CC} = \text{MIN}$ , $V_{IL} = 0.8 \text{ V}$ , $I_{OL} = 300 \text{ mA}$		0.5	0.8		0.5	0.7		
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}$ , $V_I = 5.5 \text{ V}$			1			1	$\text{mA}$	
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}$ , $V_I = 2.4 \text{ V}$			40			40	$\mu\text{A}$	
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}$ , $V_I = 0.4 \text{ V}$		-1	-1.6		-1	-1.6	$\text{mA}$	
$I_{CCH}$ Supply current, outputs high	$V_{CC} = \text{MAX}$ , $V_I = 5 \text{ V}$		8	11		8	11	$\text{mA}$	
$I_{CCL}$ Supply current, outputs low	$V_{CC} = \text{MAX}$ , $V_I = 0$		58	76		58	76	$\text{mA}$	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.  
‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

switching characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$t_{PLH}$ Propagation delay time, low-to-high-level output	$I_O \approx 200 \text{ mA}$ , $C_L = 15 \text{ pF}$ , $R_L = 50 \Omega$ , See Figure 3		30	55	ns	
$t_{PHL}$ Propagation delay time, high-to-low-level output			25	40	ns	
$\tau_{TLH}$ Transition time, low-to-high-level output				8	25	ns
$\tau_{THL}$ Transition time, high-to-low-level output				10	25	ns
$V_{OH}$ High-level output voltage after switching	$V_S = 30 \text{ V}$ , See Figure 4	$V_S - 10$			mV	

# TYPES SN55464, SN75464

## DUAL PERIPHERAL POSITIVE-NOR DRIVERS

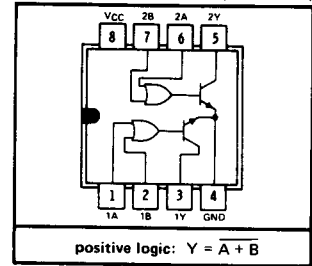
logic

FUNCTION TABLE  
(EACH DRIVER)

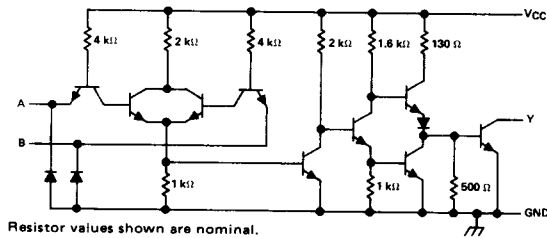
A	B	Y
L	L	H (off state)
L	H	L (on state)
H	L	L (on state)
H	H	L (on state)

H = high level, L = low level

SN55464 ... JG  
SN75464 ... JG OR P  
DUAL-IN-LINE PACKAGE (TOP VIEW)



schematic (each driver)



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN55464		SN75464		UNIT	
		MIN	TYP‡	MAX	MIN		TYP‡
$V_{IH}$ High-level input voltage		2			2	V	
$V_{IL}$ Low-level input voltage				0.8		V	
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$	-1.2	-1.5	-1.2	-1.5	V	
$I_{OH}$ High-level output current	$V_{CC} = \text{MIN}, V_{OH} = 25 \text{ V}, V_{IL} = 0.8 \text{ V}$		300		100	$\mu\text{A}$	
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 100 \text{ mA}$	0.25	0.5	0.25	0.4	V	
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 300 \text{ mA}$	0.5	0.8	0.5	0.7		
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$		1		1	mA	
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$		40		40	$\mu\text{A}$	
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		-1	-1.6	-1	mA	
$I_{CCH}$ Supply current, outputs high	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		14	19	14	19	mA
$I_{CCL}$ Supply current, outputs low	$V_{CC} = \text{MAX}, V_I = 5 \text{ V}$		67	85	67	85	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.  
‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$ .

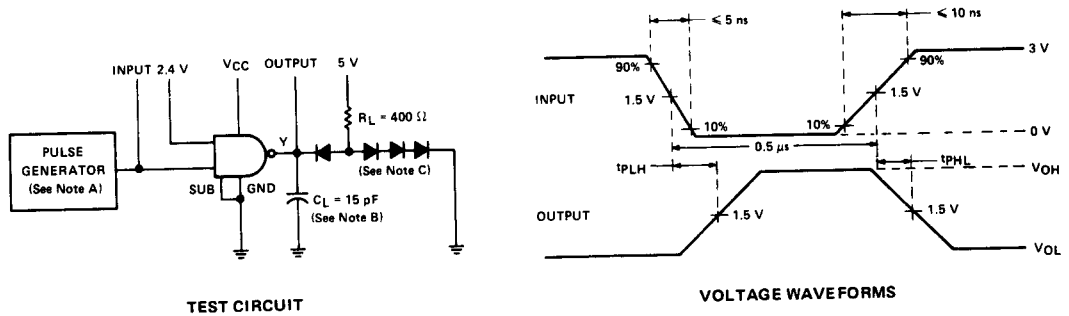
switching characteristics,  $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ Propagation delay time, low-to-high-level output	$I_O \approx 200 \text{ mA}, C_L = 15 \text{ pF}, R_L = 50 \Omega,$ See Figure 3	40	65		ns
$t_{PHL}$ Propagation delay time, high-to-low-level output		30	50		ns
$t_{TLH}$ Transition time, low-to-high-level output		8	20		ns
$t_{THL}$ Transition time, high-to-low-level output		10	20		ns
$V_{OH}$ High-level output voltage after switching	$V_S = 30 \text{ V}, I_O \approx 300 \text{ mA},$ See Figure 4	$V_S - 10$			mV



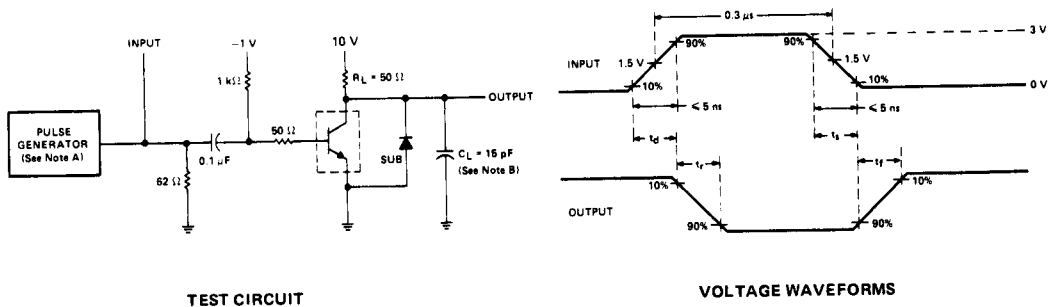
# SERIES 55460/75460 DUAL PERIPHERAL DRIVERS

## PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz,  $Z_{out} \approx 50 \Omega$ .  
 B.  $C_L$  include probe and jig capacitance.  
 C. All diodes are 1N3064.

**FIGURE 1—PROPAGATION DELAY TIMES, EACH GATE (SN55460 AND SN75460 ONLY)**

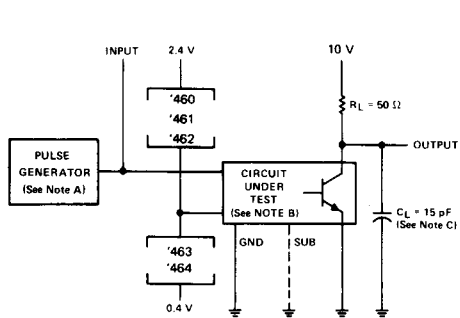


- NOTES: A. The pulse generator has the following characteristics: duty cycle  $< 1\%$ ,  $Z_{out} \approx 50 \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.

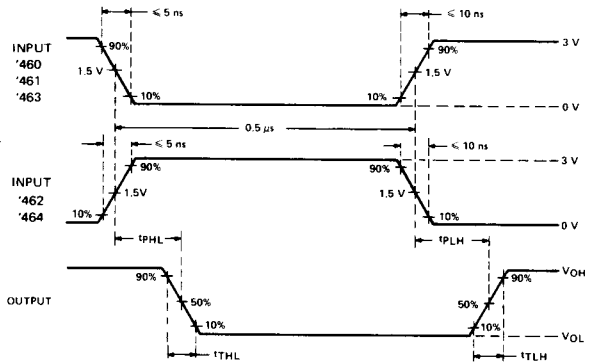
**FIGURE 2—SWITCHING TIMES, EACH TRANSISTOR (SN55460 AND SN75460 ONLY)**

# SERIES 55460/75460 DUAL PERIPHERAL DRIVERS

## PARAMETER MEASUREMENT INFORMATION



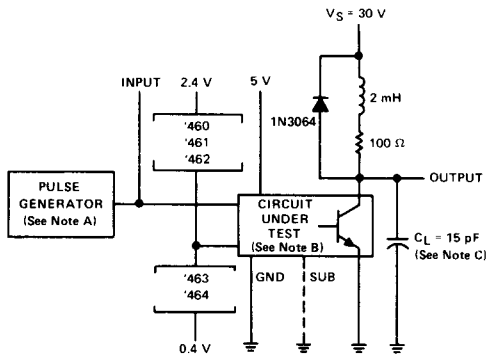
TEST CIRCUIT



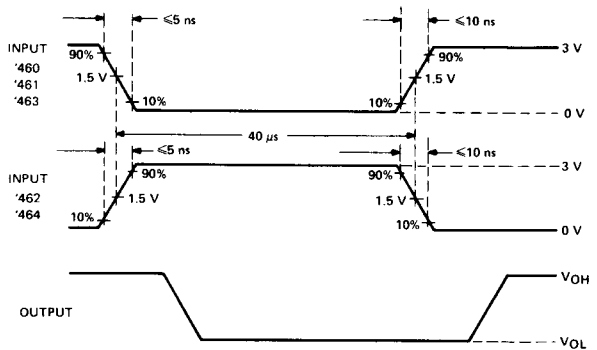
VOLTAGE WAVEFORMS

- NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz,  $Z_{out} \approx 50 \Omega$   
 B. When testing SN55460 or SN75460, connect output Y to transistor base and ground the substrate terminal.  
 C.  $C_L$  includes probe and jig capacitance.

FIGURE 3—SWITCHING TIMES OF COMPLETE DRIVERS



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz,  $Z_{out} = 50 \Omega$ .  
 B. When testing SN55460 or SN75460, connect output Y to transistor base with a 500- $\Omega$  resistor from there to ground, and ground the substrate terminal.  
 C.  $C_L$  includes probe and jig capacitance.

FIGURE 4—LATCH-UP TEST OF COMPLETE DRIVERS