

VCO + phase comparator for TV

BU2370FV

BU2370FV is a VCO+phase comparator IC used to construct PLL system. Adopting external LPF and divider can generate the PLL system and low jitter clocks. Output can be switched into half.

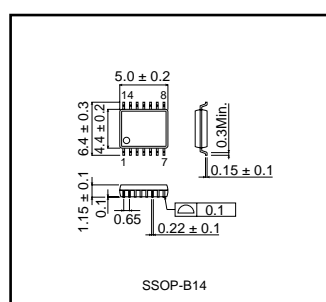
●Applications

TV

●Features

- 1) VCO can oscillate output (20MHz to 60MHz)
- 2) High-speed edge trigger type phase comparator
- 3) Can control VCO, and phase comparator independently
- 4) 3.3V signal power supply
- 5) Small SSOP-B14 package

●External dimensions (Unit : mm)



●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V _{DD}	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5 to V _{DD} +0.5	V
Operating temperature range	T _{stg}	-30 to +125	°C
Power dissipation	P _d	350	mW

*An operation is not guaranteed.

*Derating : 3.5mW/°C for operation above Ta=25°C.

*Radiation resistance design is not used.

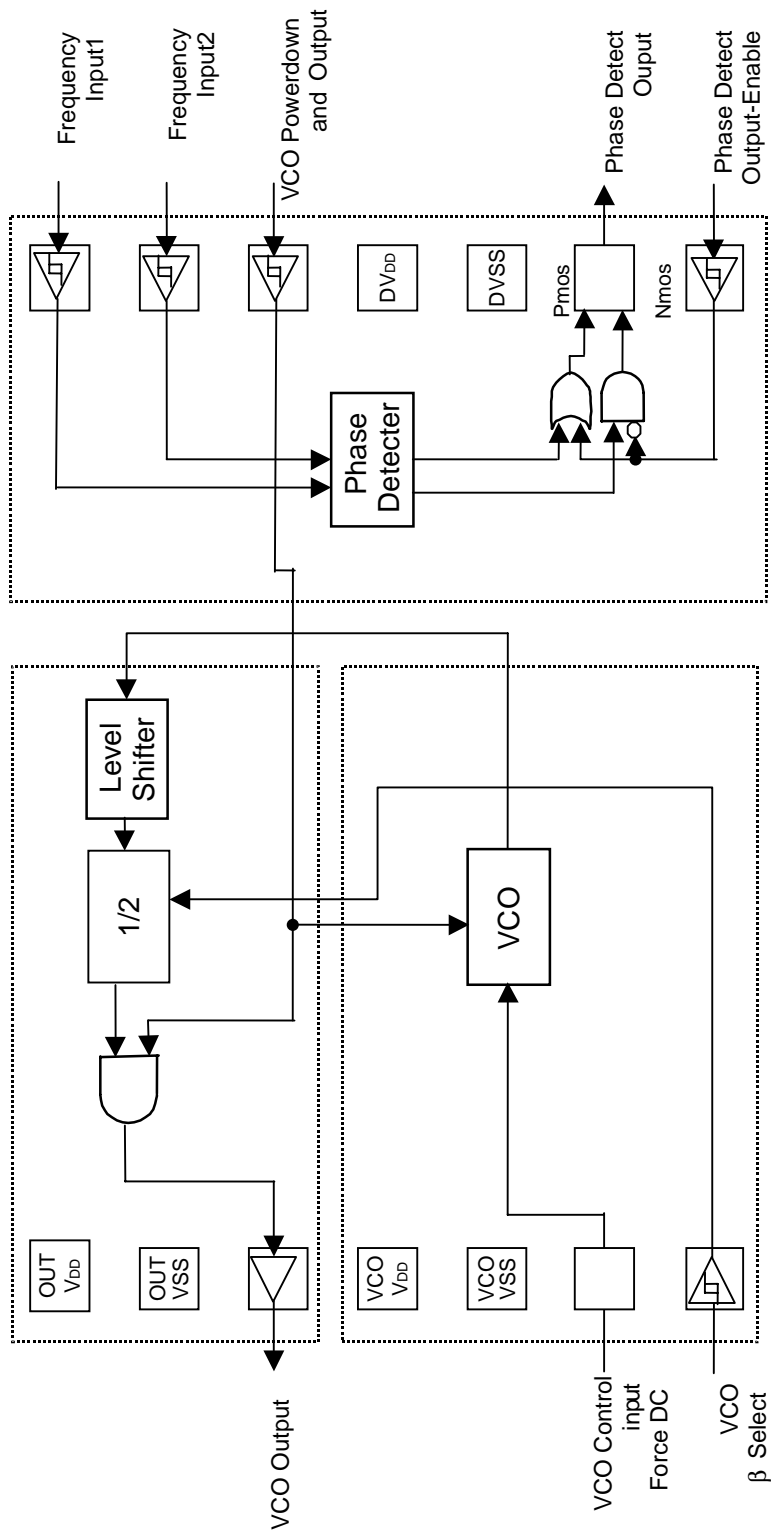
*Power dissipation is measured when BU2370FV is placed on the board.

●Recommended operating conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V _{DD}	3.15	-	3.45	V
Input H voltage range	V _{IH}	0.8V _{DD}	-	V _{DD}	V
Input L voltage range	V _{IL}	0	-	0.2V _{DD}	V
Operating temperature	T _{opr}	-20	-	70	°C
Output load	C _L	-	-	15	pF

Multimedia ICs

●Block diagram



Multimedia ICs

●Pin descriptions

Pin No.	Pin name	Functions
1	Out V _{DD}	V _{DD} for VCO-OUT
2	Out GND	GND for VCO-OUT
3	VCO OUT	VCO output
4	VCO V _{DD}	VCO analog V _{DD}
5	VCO GND	VCO analog GND
6	VCO IN	VCO control Pin
7	FSEL1	VCO β collect H : 30[MHz/V] L : 15[MHz/V]
8	PDE	PD control pin H : PD Disable (Hi impedance) L : PD Enable
9	PD OUT	PD output
10	DGND	Digital GND for PD
11	DV _{DD}	Digital V _{DD} for PD
12	VCOE	VCO control Pin H : VCO out Disable (output L fix) L : VCO out Enable
13	FIN-A	PD input
14	FIN-B	PD input

Multimedia ICs

●Input / output circuits

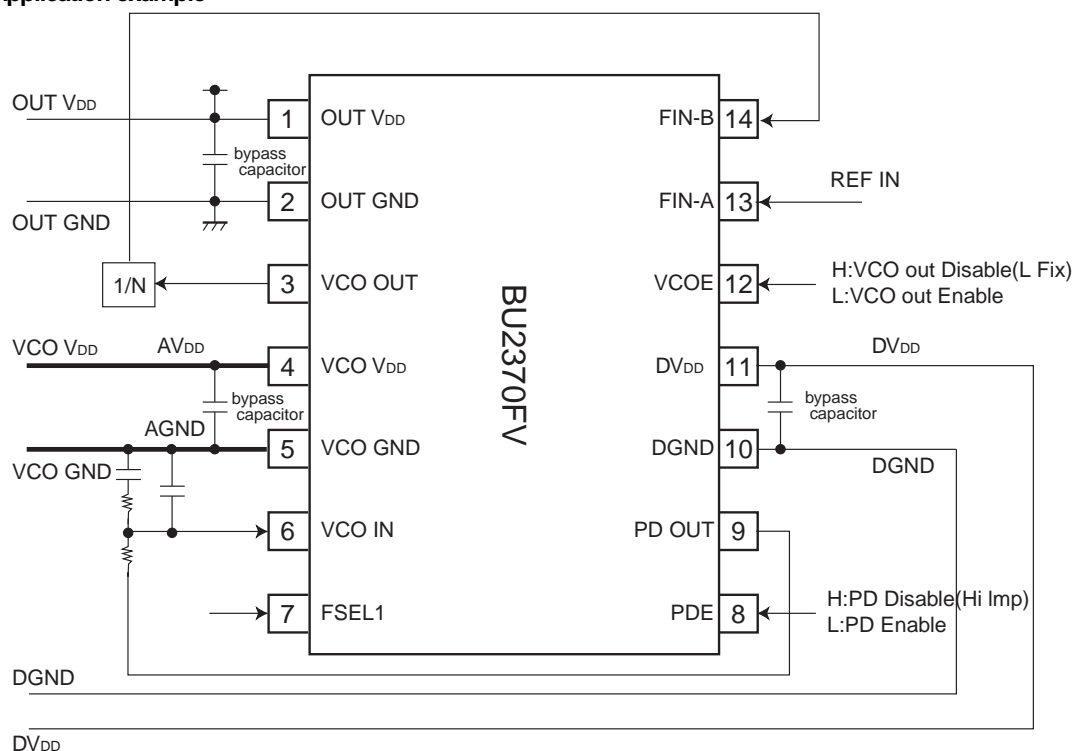
Pin No.	Equivalent circuit
Output PIN (Pin 3)	
Output PIN (Pin 9)	
Input PIN (Schmitt trigger) (Pin 7, 8, 12, 13, 14)	
Input PIN (Pin 6)	

Multimedia ICs

●Electrical characteristics (Unless otherwise noted, $T_a=25^{\circ}\text{C}$, $V_{CC}=3.3\text{V}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating current consumption	I_{DD}	-	20	-	mA	60MHz oscillation when output loaded
VCO						
Input control voltage range (Pin 6)	VID	1	-	3	V	
Input H voltage (Pin 6)	I _{IH}	-0.1	0	0.1	μA	Inflow current when V_{DD} applied to input
Input L voltage (Pin 6)	I _{IL}	-0.1	0	0.1	μA	Outflow current when GND applied to input
Max. oscillation frequency 1	F _{MAX1}	30	-	-	MHz	FSEL=L
Max. oscillation frequency 2	F _{MAX2}	60	-	-	MHz	FSEL=H
Min. oscillation frequency 1	F _{MIN1}	-	-	15	MHz	FSEL=L
Min. oscillation frequency 2	F _{MIN2}	-	-	30	MHz	FSEL=H
Frequency sensitivity 1	β_1	-	15	-	MHz/V	FSEL=L
Frequency sensitivity 2	β_2	-	30	-	MHz/V	FSEL=H
Output duty	Duty	45	50	55	%	at 1/2 V_{DD}
Rise-time	t_r	-	2.5	-	nsec	Time is from V_{DD} 0.2 to V_{DD} 0.8
Fall-time	t_f	-	2.5	-	nsec	Time is from V_{DD} 0.2 to V_{DD} 0.8

●Application example



This line is noise source. But if power line and GND are divided into two, this line becomes AV_{DD} , $AGND$

DV_{DD} , $DGND$

OUT DV_{DD} , OUT GND

Please take care this Power line. Because this line is most weak indigitalnoise. So this line must be separated from digital_ V_{DD} , GND. And place bypass capacitor ($0.01\mu\text{F}$) for power pin as close to BU2370FV as possible.

And place bypass capacitor ($0.01\mu\text{F}$) for power pin as close to BU2370FV as possible.

This line is most noise source. So it should be separated from Analog. And this line should be connected V_{DD} of external V_{CC} -outdivide. And place bypass capacitor ($0.01\mu\text{F}$) for power pin as close to BU2370FV as possible.

*Recommend to use capacitor that is better to reduce high frequency noise.

*Recommend to control (FSEL1, PDE, VCOE) by power line. (DV_{DD} , $DGND$)

Appendix

Notes

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