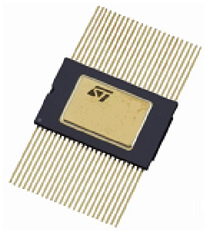
54VCXH163245

Datasheet

Rad-hard 16-bit transceiver, 1.8 V to 3.3 V bidirectional level shifter



Ceramic Flat-48

The upper metallic lid is not electrically connected to any pins, nor to the IC die inside the package

Product status link
54VCXH163245

Features

- Dual supply bidirectional level shifter
- Voltage range from 1.6 V to 3.6 V
- Separated enable pin for 3-state output
- Internal 26 Ω limiting resistor on each A side output buffer
- Bus hold
- Fail safe
- Cold spare
- Hermetic package
- 300 k/rad (Si) at any Mil1019 dose rate
- SEL immune to 110 MeV.cm^2/mg LET ions

Description

The 54VCXH163245 is a rad-hard advanced high-speed CMOS, 16-bit bidirectional, multi-purpose transceiver with 3-state outputs and cold sparing.

Designed to be used as an interface between a 3.3 V bus and a 1.8 V bus in mixed 3.3 V/1.8 V supply systems, it achieves high-speed operations while maintaining the CMOS low power dissipation.

All pins have cold spare buffers to change them to high impedance when V_{DD} is tied to ground.

This IC is intended for a two-way asynchronous communication between data buses. The direction of data transmission is determined by the nDIR inputs.

1 Functional description

Figure 1. Logic diagram

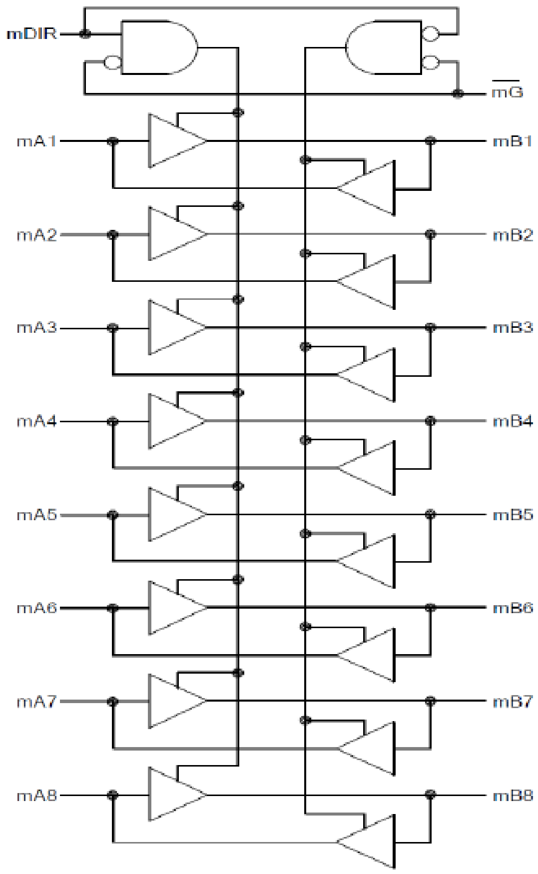


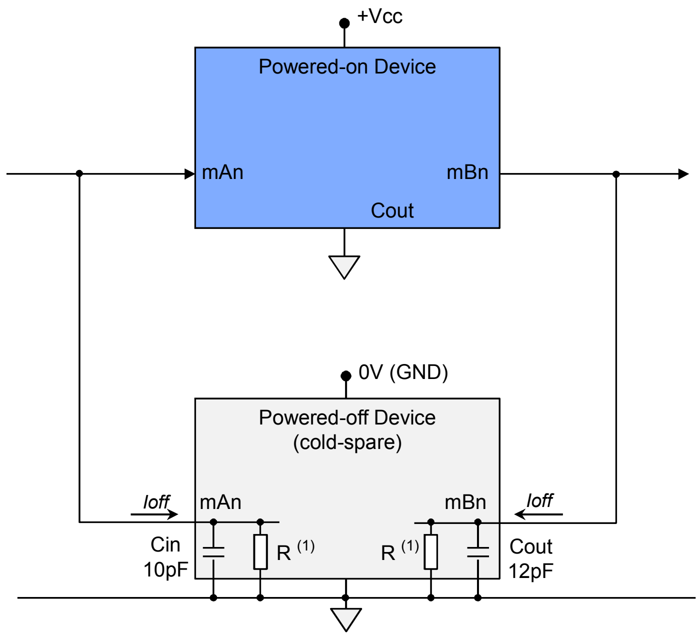
Table 1. Truth table

Inputs		Function		Outputs	Comments
m G	mDIR	Bus A	Bus B		
L	L	Output	Input	A = B	H = high-voltage level L = low-voltage level Z = high impedance X = irrelevant or don't care
L	H	Input	Output	B = A	
H	X	Z	Z	Z	

1.1 Cold spare

The 54VCXH163245 features a cold spare input and output buffer. In high reliability applications, cold sparing enables a redundant device to be tied to the data bus with its power supply at 0 V (V_{CC} = 0 V) without affecting the bus signals or injecting current from the I/Os to the power supplies. Cold sparing also allows redundant devices that are not powered to be switched on when required only. Power consumption is therefore reduced by switching off the redundant circuit. This has no impact on the application. Cold sparing is achieved by implementing a high impedance between I/Os and V_{CC}. The ESD protection is ensured through a non-conventional dedicated structure. Using cold spare on Bus A and Bus B separately is not allowed. In cold spare, both V_{CCA} and V_{CCB} must be at 0 V.

Figure 2. Cold spare and cold redundancy



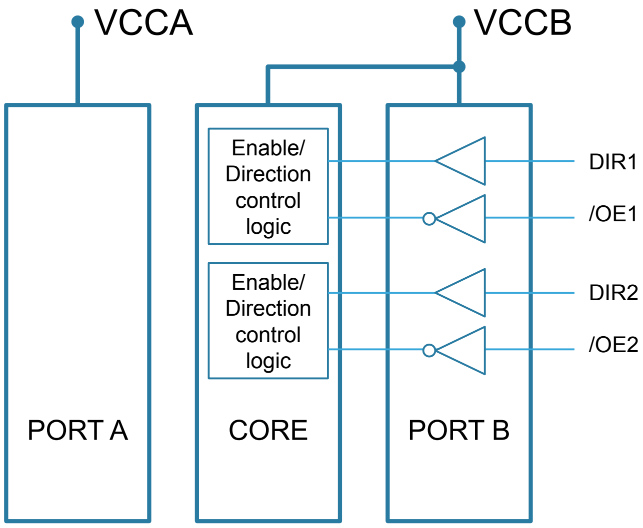
1. R = Ioff/V_{CC}

1.2 Power-up and operating

During power-up, all outputs should be forced to high impedance by setting /OEx high, after VCCA and VCCB are switched on, /OEx can be set low. In this manner any transient and erroneous signals during power-up are avoided.

- In power-up:
  VCCB must be powered up before VCCA
- In operating mode, to guarantee proper operation functionality after power-up:
  VCCA has to be above or equal to VCCB (VCCB higher than VCCA is forbidden)
- In power-down:
  VCCA must be powered down before VCCB.

Figure 3. Power supply domain



Note: *Control signals on DIRx and /OEx, corresponding CMOS logic levels that apply to all control inputs are: V_{ILmax} = 0.3xVCCB and V_{IHmin} = 0.7xVCCB.*
For a proper operation, connect power to all VCC and ground all GND pins (i.e., no floating VCC or GND pins).
Tie all unused inputs to GND.

1.3 Pin connections and description

Figure 4. Pin connections

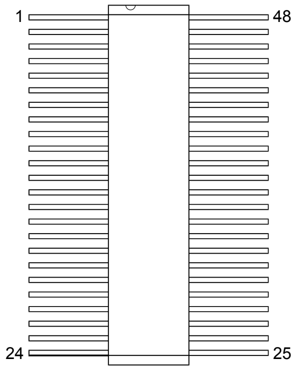


Table 2. Pin description

Device type	All		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	1DIR	25	$\overline{2G}$
2	1B1	26	2A8
3	1B2	27	2A7
4	GND	28	GND
5	1B3	29	2A6
6	1B4	30	2A5
7	V_{CCB}	31	V_{CCA}
8	1B5	32	2A4
9	1B6	33	2A3
10	GND	34	GND
11	1B7	35	2A2
12	1B8	36	2A1
13	2B1	37	1A8
14	2B2	38	1A7
15	GND	39	GND
16	2B3	40	1A6
17	2B4	41	1A5
18	V_{CCB}	42	V_{CCA}
19	2B5	43	1A4
20	2B6	44	1A3
21	GND	45	GND
22	2B7	46	1A2
23	2B8	47	1A1
24	2DIR	48	$\overline{1G}$

2 Absolute maximum ratings and operating conditions

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. Unless otherwise noted, all voltages are referenced to GND. The limits for the parameters specified herein apply over the full specified V_{CC} range and case temperature range of -55 °C to 125 °C.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (V_{CCA} and V_{CCB})[1]	-0.5 to 4.6	V
V_{IA}	DC input voltage range port A	-0.5 to 4.6	
V_{IB}	DC input voltage range port B	-0.5 to 4.6	
G/DIR	DC input voltage range G and DIR	-0.5 to 4.6	
V_{OA}	DC output voltage range port A	-0.5 to V_{CCA} + 0.5 V	
V_{OB}	DC output voltage range port B	-0.5 to V_{CCB} + 0.5 V	
I_{IA}	DC input currents port A, anyone input	± 20	mA
I_{IB}	DC input currents port B, anyone input	± 20	
T_{stg}	Storage temperature range	-65 to 150	°C
T_L	Lead temperature (10 s)	300	
T_J	Junction temperature range	175	
R_{thjc}	Thermal resistance junction-to-case [2]	22	°C/W
ESD	HBM: human body model [3]	2	kV

1. *V_{CCA} must be higher or equal to V_{CCB}. (V_{CCB} higher than V_{CCA} is forbidden).*
2. *Short-circuits can cause excessive heating and destructive dissipation. Values are typical.*
3. *Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.*

In Table 4. Operating conditions below, unless otherwise noted, all voltages are referenced to GND.

Table 4. Operating conditions

Symbol	Parameter	Value	Unit
V_{CCA}	Supply voltages [1]	1.4 to 3.6	V
V_{CCB}			
V_I	Input voltage	0 to 3.6	
V_O	Output voltage	0 to V_{CC}	
T_{op}	Operating temperature	-55 to 125	°C
d_t/d_v	Input rise and fall time, V_{CC} = 3 V [2]	0 to 10	ns/V

1. *V_{CCA} must be higher or equal to V_{CCB}. (V_{CCB} higher than V_{CCA} is forbidden).*
2. *Derates system propagation delays by difference in rise time to switch point for t_r or t_f > 1 ns/V.*

3 Electrical characteristics

In Table 5. Electrical characteristics below, T_{op} = -55 °C to 125 °C, V_{CC} = 1.4 V to 3.6 V, unless otherwise specified. Each input/output, as applicable, is tested at the specified temperature, for the specified limits. Non-designated output terminals are high level logic, low level logic or open, except for all I_{CC} tests, where the output terminals are open. When performing these tests, the current meter must be placed in the circuit so that all current flows through the meter.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions		V_{CCA} (V)	V_{CCB} (V)	Min.	Max.	Unit
V_{IC-}	Negative input clamp voltage	I_{IN} = -1 mA		Open	Open	-1.5	-0.4	V
V_{OH}	High-level output voltage	Bus A output V_{IN} = V_{IH}(min) or V_{IL}(max)	I_{OH} = -100 µA	3	2.3	2.8		
			I_{OH} = -8 mA	3	2.3	2.4		
			I_{OH} = -8 mA	3	1.65	2.4		
			I_{OH} = -6 mA	2.3	1.65	1.8		
		Bus B output V_{IN} = V_{IH}(min) or V_{IL}(max)	I_{OH} = -100 µA	3	2.3	2.1		
			I_{OH} = -18 mA	3	2.3	1.7		
			I_{OH} = -6 mA	3	1.65	1.25		
			I_{OH} = -6 mA	2.3	1.65	1.25		
V_{OL}	Low-level output voltage	Bus A output V_{IN} = V_{IH}(min) or V_{IL}(max)	I_{OL} = 100 µA	3	2.3		0.2	
			I_{OL} = 8 mA	3	2.3		0.55	
			I_{OL}= 8 mA	3	1.65		0.55	
			I_{OL} = 6 mA	2.3	1.65		0.4	
		Bus B output V_{IN} = V_{IH}(min) or V_{IL}(max)	I_{OL} = 100 µA	3	2.3		0.2	
			I_{OL} = 18 mA	3	2.3		0.6	
			I_{OL} = 6 mA	3	1.65		0.3	
			I_{OL} = 6 mA	2.3	1.65		0.3	
V_{IH}	High-level input voltage	Bus A		1.8	1.8	0.65 x V_{CCA}		
				2.5	2.5	1.6		
				3.3	3.3	2		
		Bus B		1.8	1.8	0.65 x V_{CCB}		
				2.5	2.5	1.6		
				3.3	3.3	2		
V_{IL}	Low-level input voltage	Bus A		1.8	1.8		0.35 x V_{CCA}	V
				2.5	2.5		0.7	
				3.3	3.3		0.8	
		Bus B		1.8	1.8		0.35 x V_{CCB}	
				2.5	2.5		0.7	
				3.3	3.3		0.8	

Symbol	Parameter	Test conditions		V_{CCA} (V)	V_{CCB} (V)	Min.	Max.	Unit
I_{IH}	Input leakage current high	On nDIR and $\overline{G}$: For input under test: V_{IN} = V_{CC} For all other inputs: V_{IN} = V_{CC} or GND		3.6	2.7		5	
I_{IL}	Input leakage current low	On nDIR and $\overline{G}$: For input under test: V_{IN} = GND For all other inputs: V_{IN} = V_{CC} or GND		3.6	2.7	-5		
I_{CCH}	Quiescent current, output high	DIR and $\overline{G}$ = V_{CCB} or GND: For Bus A, V_{IN} = V_{CCA} or GND For Bus B, V_{IN} = V_{CCB} or GND		3.6	3.6		20	
I_{CCL}	Quiescent current, output low	DIR and $\overline{G}$ = V_{CCB} or GND: For Bus A, V_{IN} = V_{CCA} or GND For Bus B, V_{IN} = V_{CCB} or GND		3.6	3.6		20	
ΔI_{CC}	Quiescent current delta, TTL input levels	For input under test: V_{IH} = V_{CC} - 0.6 V For all other inputs: V_{IN} = V_{CC} or GND		3.6	3.6		750	μA
I_{CCZ}	Quiescent current, output three-state	DIR and $\overline{G}$ = V_{CCB} or GND: For Bus A, V_{IN} = V_{CCA} or GND For Bus B, V_{IN} = V_{CCB} or GND		3.6	3.6		20	
I_{OZH}	Three-state output leakage current high	V_{IN} = V_{IH} min. or V_{IL} max, V_{OUT} = V_{CC} or GND		3.6	2.7		5	
I_{OZL}	Three-state output leakage current low	V_{IN} = V_{IH} min. or V_{IL} max, V_{OUT} = V_{CC} or GND		3.6	2.7	-5		
I_{OFF}	Power-off leakage current (cold spare)	DIR and $\overline{G}$ = GND to 3.6 V: For Bus A, V_{IN} = V_{CCA} to 3.6 V For Bus B, V_{IN} = V_{CCB} to 3.6 V		0	0	-10	10	
$I_{I(HOLD)}$	Input hold current	Bus A	V_{INA} = 0.7 V	2.3	1.65	45		μA
			V_{INA} = 1.6 V	2.3	1.65		-45	
			V_{INA} = 0.8 V	3	1.65	75		
			V_{INA} = 2 V	3	1.65		-75	
			V_{INA} = 0.8 V	3	2.3	75		
			V_{INA} = 2 V	3	2.3		-75	
			V_{INA} 0 to 3.6 V	3.6	2.7		±500	
		Bus B	V_{INB} = 0.57 V	2.3	1.65	25		
			V_{INB} = 1.07 V	2.3	1.65		-25	
			V_{INB} = 0.57 V	3	1.65	25		
			V_{INB} = 1.07 V	3	1.65		-25	
			V_{INB} = 0.7 V	3	2.3	45		

Symbol	Parameter	Test conditions	V_{CCA} (V)	V_{CCB} (V)	Min.	Max.	Unit
$I_{I(HOLD)}$	Input hold current	Bus B, V_{INB} = 1.6 V	3	2.3		-45	µA
		Bus B, V_{INB} 0 to 2.7 V	3.6	2.7		±500	
C_{IN}	Input capacitance	Tc = 25 °C (1)	GND	GND		10	pF
C_{OUT}	Output capacitance		GND	GND		12	
C_{PD}	Power dissipation capacitance, 1 MHz		3.3	2.5		20	
—	Functional tests	V_{IN} = V_{IH} min. or V_{IL} max.	3.6 V	1.8 V	L	H	—
			2.7 V	2.3 V			
t_{PHL1} and t_{PLH1}	Propagation delay time mAn to mBn	C_L = 30 pF min., R_L = 500 Ω	2.5	1.8		6	ns
			3.3	1.8		6	
			3.3	2.5		5.5	
t_{PHL2} and t_{PLH2}	Propagation delay time mBn to mAn	C_L = 30 pF min., R_L = 500 Ω	2.5	1.8		7.5	
			3.3	1.8		7	
			3.3	1.8		7	
t_{PZL1}	Propagation delay time, output enable, m$\overline{G}$ to mBn	C_L = 30 pF min., R_L = 500 Ω	2.5	1.8		10	
			3.3	1.8		10	
			3.3	2.5		7	
t_{PZH1}			2.5	1.8		10	
			3.3	1.8		10	
			3.3	2.5		7	
t_{PZL2}	Propagation delay time, output enable, m$\overline{G}$ to mAn	C_L = 30 pF min., R_L = 500 Ω	2.5	1.8		8.5	
			3.3	1.8		8.5	
			3.3	2.5		8	
t_{PZH2}			2.5	1.8		8.5	
			3.3	1.8		8.5	
			3.3	2.5		8	
t_{PLZ1}	Propagation delay time, output disable, m$\overline{G}$ to mBn	C_L = 30 pF min., R_L = 500 Ω	2.5	1.8		6	ns
			3.3	1.8		6	
			3.3	2.5		5.5	
t_{PHZ1}			2.5	1.8		6	
			3.3	1.8		6	
			3.3	2.5		5.5	
t_{PLZ2}	Propagation delay time, output disable, m$\overline{G}$ to mAn	C_L = 30 pF min., R_L = 500 Ω	2.5	1.8		7.5	
			3.3	1.8		7	
			3.3	2.5		7	
t_{PHZ2}			2.5	1.8		7.5	
			3.3	1.8		7	
			3.3	2.5		7	

1. *C_{IN}, C_{OUT}, and C_{PD} are measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and C_{OUT} are measured between the designated terminal and GND at a frequency of 1 MHz. This test may be performed at 10 MHz and guaranteed, if not tested, at 1 MHz. The DC bias for the pin under test (V_{BIAS}) = 2.5 V or 3.0 V. For C_{IN}, C_{OUT}, and C_{PD}, all applicable pins are tested on five devices with zero failures. Power dissipation capacitance (C_{PD}) determines both the power consumption (PD) and dynamic current consumption (IS), where: PD = $(C_{PD} + C_L) (V_{CC} \times V_{CC}) f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$, IS = $(C_{PD} + C_L) V_{CC} f + I_{CC} + n \times d \times \Delta I_{CC}$. For both P_D and I_S, n is the number of device inputs at TTL levels, d is the duty cycle of the input signal, f is the frequency of the input signal, and C_L is the external output load capacitance.*

4 Radiations

Total dose (Mil1019 dose rate): all parameters are post-irradiation guaranteed by wafer-lot acceptance (after dose, all guaranteed electrical parameters are tested on a sample of units of each wafer lot). All parameters provided in Table 5. Electrical characteristics apply to both pre- and post-irradiation. The 54VCXH163245 is a pure CMOS product. The irradiation is performed at high dose rates.

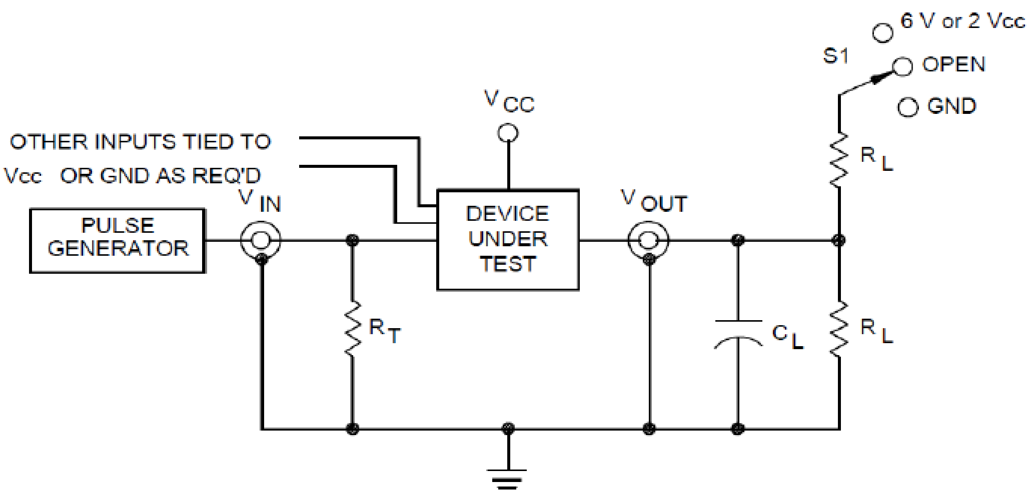
Heavy-ions: the behavior of the product when submitted to heavy ions is guaranteed by qualification and is not tested in production. Heavy-ion trials are performed on qualification lots only.

Table 6. Radiations

Type	Features	Value	Unit
TID	Total Ionizing dose, high-dose rate (50 - 300 rad/s) up to:	300	krad
Heavy ions	SEL immune (at 125 °C) up to:	110	MeV.cm²/mg
	SEU immune up to:	18.5	

5 Test circuit

Figure 5. Test circuit



1. C_L = 50 pF or equivalent (includes jig and probe capacitance), R_T = Z_{OUT} of pulse generator (typically 50 Ω), V_{REF} = 0.5 V_{DD}. I_{SRC} is set to -1.0 mA and I_{SNK} is set to 1.0 mA for t_{PHL} and t_{PLH} measurements. Input signal from pulse generator: V_I = 0.0 V to V_{DD}; f = 10 MHz; t_r = 1.0 V/ns ±0.3 V/ns; t_f = 1.0 V/ns ±0.3 V/ns; tr and tf are measured from 0.1 V_{DD} to 0.9 V_{DD} and from 0.9 V_{DD} to 0.1 V_{DD} respectively.
2. When measuring t_{PLH} and t_{PHL}: S1 = open
3. When measuring t_{PLZ} and t_{PZL}: S1 = 2VCC for VCC = 1.8 V and VCC = 2.3 V to 2.7 V; S1 = 6.0 V for VCC = 3.0 V to 3.6 V.
4. When measuring t_{PHZ} and t_{PZH}: S1 = GND.
5. The t_{PZL} and t_{PZH} reference waveform is for the output under test with internal conditions set so that the output is low at V_{OL} except when disabled by the output enable control. The t_{PZL} and t_{PZH} reference waveform is for the output under test with internal conditions set so that the output is high at V_{OH} except when disabled by the output enable control.
6. C_L = 30 pF minimum or equivalent (includes test jig and probe capacitance)
7. RT = 50 Ω or equivalent, R_L = 500 Ω or equivalent
8. Input signal from pulse generator: V_{IN} = 0.0 V to V_{IH}; PRR = 1 MHz; ZO = 50Ω; tr = 2.0 ns; tf = 2.0 ns; tr and tf are measured from 10 % of V_{IH} to 90 % of V_{IH} and from 90 % of V_{IH} to 10 % of V_{IH}, respectively; duty cycle = 50 percent.
9. Timing parameters are tested at a minimum input frequency of 1 MHz

Table 7. Voltage points for measurements

Symbol	Parameter	V_{CC}	
		1.8 V, 2.3 V, and 2.7 V	3 V to 3.6 V
V_{IH}	High-level input voltage	V_{CC}	2.7 V
V_M	Middle threshold voltage point	$V_{CC}/2$	1.5 V
V_X	Low threshold voltage point	V_{OL} + 0.15 V	V_{OL} + 0.3 V
V_Y	High threshold voltage point	V_{OH} - 0.15 V	V_{OH} - 0.3 V

Figure 6. Propagation delay

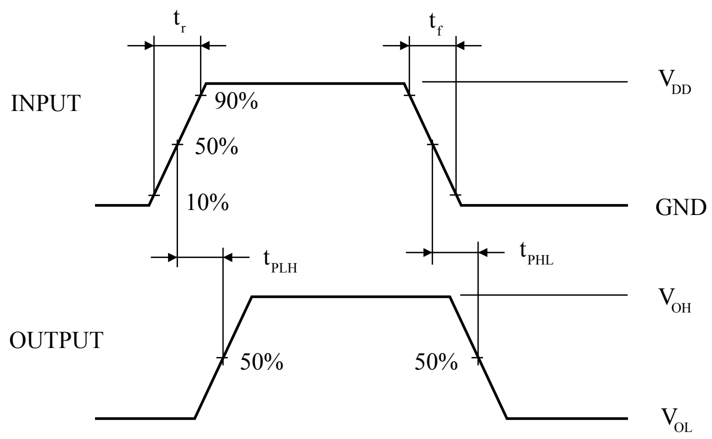


Figure 7. Enable and disable times

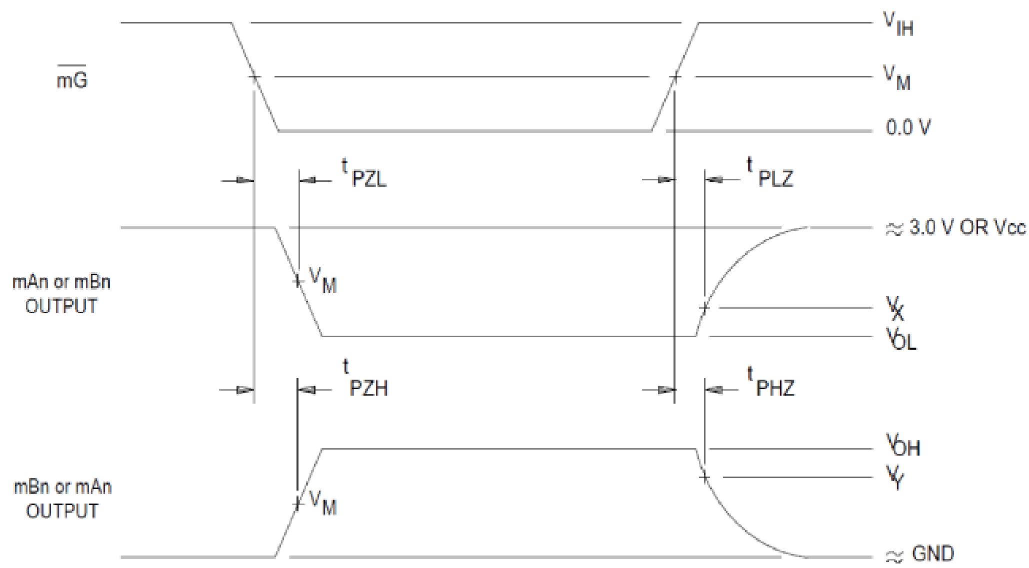
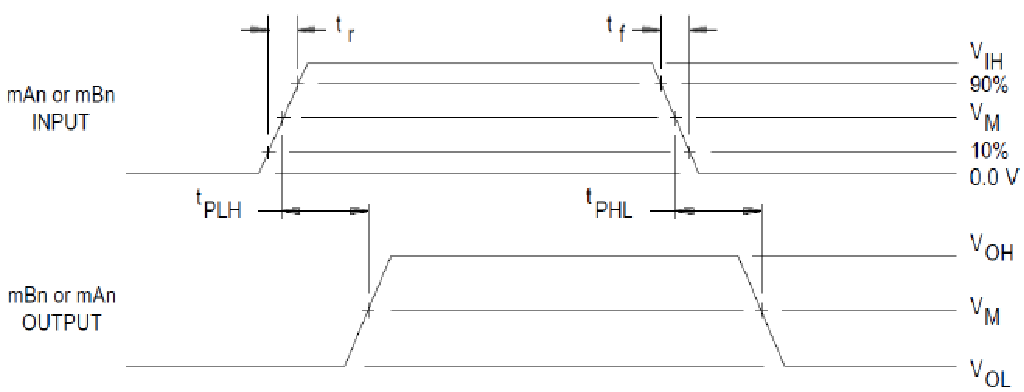


Figure 8. Propagation delay times



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 Ceramic Flat-48 package information

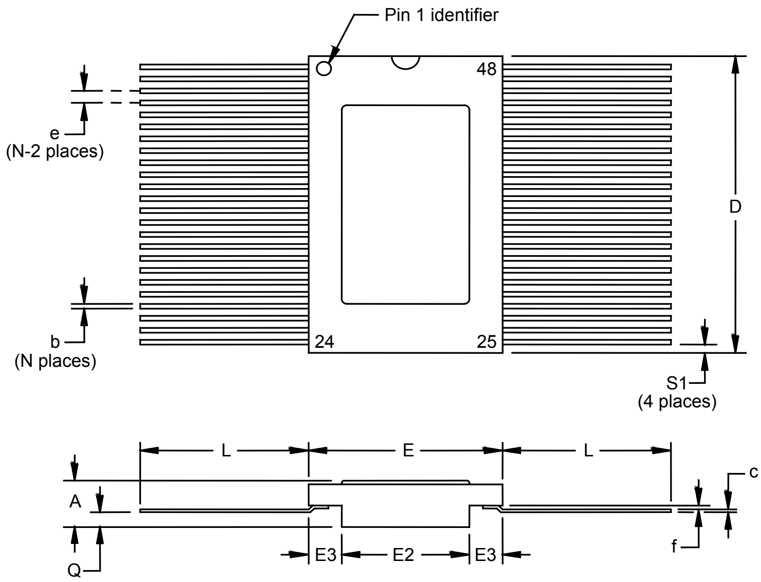


Figure 9. Ceramic Flat-48 package outline

Table 8. Ceramic Flat-48 mechanical data

Ref.	Dimensions					
	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.18	2.47	2.72	0.086	0.097	0.107
b	0.20	0.254	0.30	0.008	0.010	0.012
c	0.12	0.15	0.18	0.005	0.006	0.007
D	15.57	15.75	15.92	0.613	0.620	0.627
E	9.52	9.65	9.78	0.375	0.380	0.385
E2	6.22	6.35	6.48	0.245	0.250	0.255
E3	1.52	1.65	1.78	0.060	0.065	0.070
e		0.635			0.025	
f		0.20			0.008	
L	6.85	8.38	9.40	0.270	0.330	0.370
Q	0.66	0.79	0.92	0.026	0.031	0.036
S1	0.25	0.43	0.61	0.010	0.017	0.024

7 Ordering information

Table 9. Order code

Order code	SMD(1)	Quality level	Temp. range	Mass	Package	Marking(2)	Packing
RHFXH163245K1	-	Engineering model	-55 to +125 °C	1.50 g	Flat-48	-	Conductive strip pack
RHFXH163245K01V	5962F1120701VXC	QML-V flight				5962F1120701VXC	

1. *Standard microcircuit drawing.*
2. *Specific marking only. Complete marking includes the following:*
   - *ST logo*
   - *Date code (date the package was sealed) in YYWWA (year, week, and lot index of week)*
   - *Country of origin (FR= France)*

Note: Contact your ST sales office for information regarding the specific conditions for products in die form.

8 Other information

8.1 Date code

The date code (date the package was sealed) is structured as follows:

- Engineering model: 3yywwz
- Flight model: yywwz

Where:

yy = last two digits of the year, ww = week digits, z = lot index of the week

8.2 Product documentation

Each product shipment includes a set of associated documentation within the shipment box. This documentation depends on the quality level of the products, as detailed in the table below.

The certificate of conformance is provided on paper whatever the quality level. For QML parts, complete documentation, including the certificate of conformance, is provided on a CDROM.

Table 10. Product documentation

<table>
<tr><th>Quality level</th><th>Item</th></tr>
<tr><td>Engineering model</td><td>Certificate of conformance including:
• Customer name
• Customer purchase order number
• ST sales order number and item
• ST part number
• Quantity delivered
• Date code
• Reference to ST datasheet
• Reference to TN1181 on engineering models
• ST Rennes assembly lot ID</td></tr>
<tr><td rowspan="7">QML-V Flight</td><td>Certificate of Conformance including:
• Customer name
• Customer purchase order number
• ST sales order number and item
• ST part number
• Quantity delivered
• Date code
• Serial numbers
• Group C reference
• Group D reference
• Reference to applicable SMD
• ST Rennes assembly lot ID</td></tr>
<tr><td>Quality control inspection (groups A, B, C, D, E)</td></tr>
<tr><td>Screening electrical data in/out summary</td></tr>
<tr><td>Precap report</td></tr>
<tr><td>PIND (particle impact noise detection) test</td></tr>
<tr><td>SEM (scanning electronic microscope) inspection report</td></tr>
<tr><td>X-ray plates</td></tr>
</table>

Revision history

Table 11. **Document revision history**

Date	Revision	Changes
27-Jul-2016	1	Initial release
15-Sep-2016	2	Table 4: "Absolute maximum ratings": updated V_{IA} value and added G/DIR parameter. Table 5: "Operating conditions": updated V_I value
29-Sep-2016	3	*Section 1.1: "Cold spare"*: updated text *Section 1.2: "Power-up"*: updated footnotes of *Figure 3: "Power-up"*
30-Nov-2017	4	Updated Heavy ions value Table 7: "Radiations"
17-Sep-2018	5	Updated Figure 3. Power supply domain and Section 1.2 Power-up and operating, Section 1.3 Pin connections and description and Section 7 Ordering information. Minor text changes.
13-Jul-2021	6	Updated Section Features and Section 1.2 Power-up and operating.
14-Sep-2021	7	Updated Section Description.

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