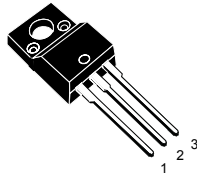
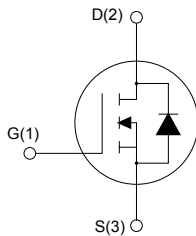


N-channel 950 V, 275 mΩ typ., 18 A, MDmesh DK5 Power MOSFET in a TO-220FP package



TO-220FP



AM01475v1_noZen_noTab


Product status link
[STF20N95DK5](#)
Product summary

| | |
|-------------------|-------------|
| Order code | STF20N95DK5 |
| Marking | 20N95DK5 |
| Package | TO-220FP |
| Packing | Tube |

Features

| Order code | V _{DS} | R _{DS(on)} max. | I _D |
|-------------|-----------------|--------------------------|----------------|
| STF20N95DK5 | 950 V | 330 mΩ | 18 A |

- Fast-recovery body diode
- Best R_{DS(on)} x area
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is part of the MDmesh DK5 fast-recovery diode series. The MDmesh DK5 combines very low recovery charge (Q_{rr}) and recovery time (t_{rr}) with an excellent improvement in R_{DS(on)} * area and one of the most effective switching behaviors, ideal for half bridge and full bridge converters.

1 Electrical ratings

Table 1. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|---|------------|------------------|
| V_{GS} | Gate-source voltage | ± 30 | V |
| I_D | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ | 18 | A |
| | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 11 | |
| $I_{DM}^{(1)}$ | Drain current (pulsed) | 72 | A |
| P_{TOT} | Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$ | 28 | W |
| $dv/dt^{(2)}$ | Peak diode recovery voltage slope | 50 | V/ns |
| $dv/dt^{(3)}$ | MOSFET dv/dt ruggedness | 50 | V/ns |
| V_{ISO} | Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$, $T_C = 25\text{ }^\circ\text{C}$) | 2.5 | kV |
| T_{stg} | Storage temperature range | -55 to 150 | $^\circ\text{C}$ |
| T_J | Operating junction temperature range | | $^\circ\text{C}$ |

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 18\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS}(\text{peak}) \leq V_{(BR)DSS}$, $V_{DD} = 760\text{ V}$.
3. $V_{DS} \leq 760\text{ V}$.

Table 2. Thermal data

| Symbol | Parameter | Value | Unit |
|------------|---|-------|---------------------------|
| R_{thJC} | Thermal resistance, junction-to-case | 4.4 | $^\circ\text{C}/\text{W}$ |
| R_{thJA} | Thermal resistance, junction-to-ambient | 62.5 | $^\circ\text{C}/\text{W}$ |

Table 3. Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|----------|--|-------|------|
| I_{AR} | Maximum current during repetitive or single pulse avalanche | 6 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$) | 520 | mJ |

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 4. On/off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-----------------------------------|---|------|------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$ | 950 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{GS} = 0\text{ V}$, $V_{DS} = 950\text{ V}$ | | | 1 | μA |
| | | $V_{GS} = 0\text{ V}$, $V_{DS} = 950\text{ V}$, $T_C = 125\text{ °C}^{(1)}$ | | | 100 | μA |
| I_{GSS} | Gate source leakage current | $V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$ | | | ± 10 | μA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DD} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$ | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$, $I_D = 9\text{ A}$ | | 275 | 330 | m Ω |

1. Defined by design, not subject to production test.

Table 5. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------------|---------------------------------------|--|------|------|------|----------|
| C_{iss} | Input capacitance | $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$ | - | 1600 | - | pF |
| C_{oss} | Output capacitance | | - | 76 | - | pF |
| C_{rss} | Reverse transfer capacitance | | - | 5 | - | pF |
| $C_{o(tr)}^{(1)}$ | Equivalent capacitance time related | $V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }760\text{ V}$ | - | 169 | - | pF |
| $C_{o(er)}^{(2)}$ | Equivalent capacitance energy related | | - | 60 | - | pF |
| R_G | Intrinsic gate resistance | $f = 1\text{ MHz}$, $I_D = 0\text{ A}$ | - | 4 | - | Ω |
| Q_g | Total gate charge | $V_{DD} = 760\text{ V}$, $I_D = 18\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15. Test circuit for gate charge behavior) | - | 50.7 | - | nC |
| Q_{gs} | Gate source charge | | - | 7.8 | - | nC |
| Q_{gd} | Gate drain charge | | - | 34.2 | - | nC |

1. $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

2. $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

Table 6. Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DS} = 475\text{ V}$, $I_D = 9\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ | - | 23 | - | ns |
| t_r | Rise time | | - | 23 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform) | - | 74 | - | ns |
| t_f | Fall time | | - | 25.4 | - | ns |

Table 7. Source-drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|---|------|------|------|---------------|
| I_{SD} | Source-drain current | | - | | 18 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 72 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD} = 18\text{ A}, V_{GS} = 0\text{ V}$ | - | | 1.5 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 9\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$ | - | 150 | | ns |
| Q_{rr} | Reverse recovery charge | $V_{DD} = 60\text{ V}$ | - | 1 | | μC |
| I_{RRM} | Reverse recovery current | (see Figure 16. Test circuit for inductive load switching and diode recovery times) | - | 13.5 | | A |
| t_{rr} | Reverse recovery time | $I_{SD} = 9\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$ | - | 264 | | ns |
| Q_{rr} | Reverse recovery charge | $V_{DD} = 60\text{ V}, T_J = 150\text{ }^\circ\text{C}$ | - | 2.9 | | μC |
| I_{RRM} | Reverse recovery current | (see Figure 16. Test circuit for inductive load switching and diode recovery times) | - | 22 | | A |

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

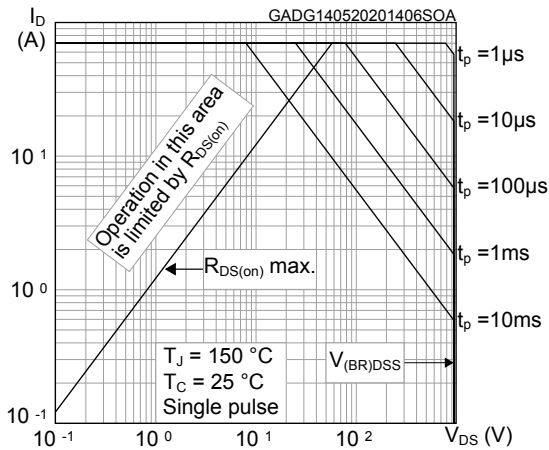


Figure 2. Maximum transient thermal impedance

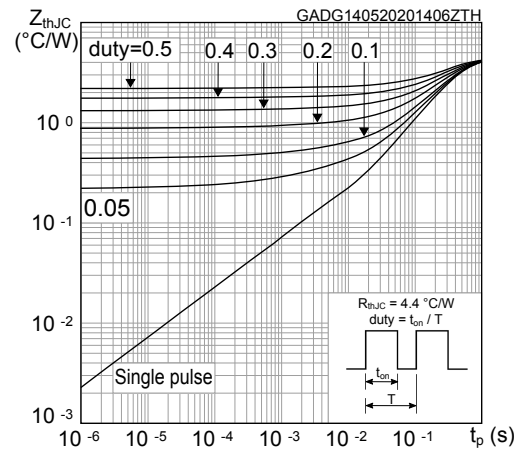


Figure 3. Output characteristics

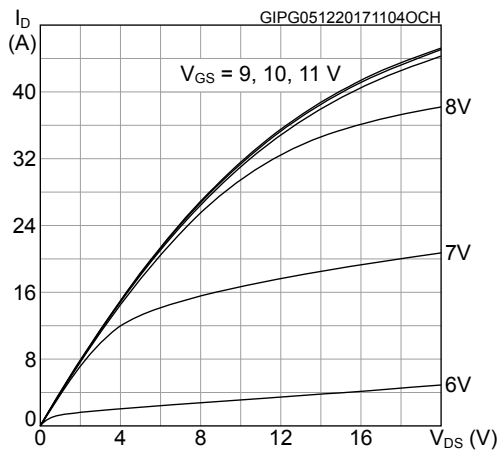


Figure 4. Transfer characteristics

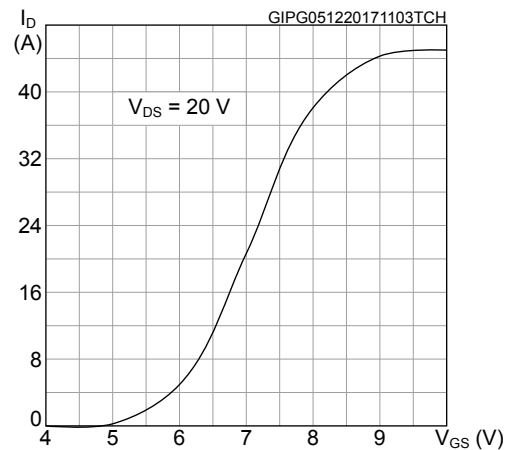


Figure 5. Gate charge vs gate-source voltage

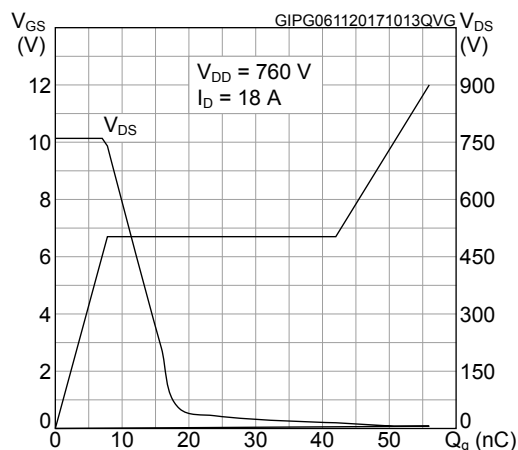


Figure 6. Static drain-source on-resistance

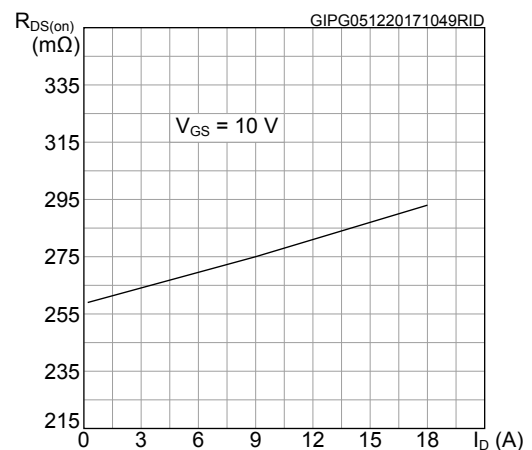


Figure 7. Capacitance variations

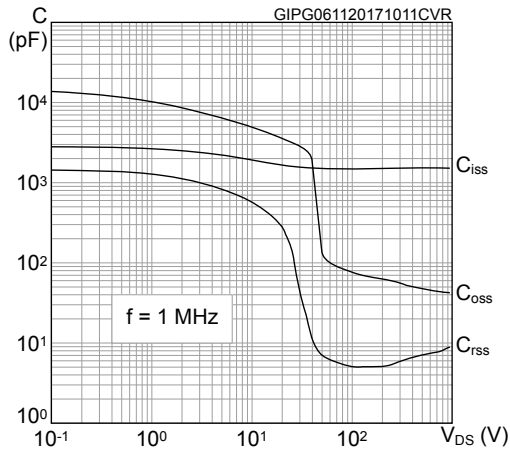


Figure 8. Output capacitance stored energy

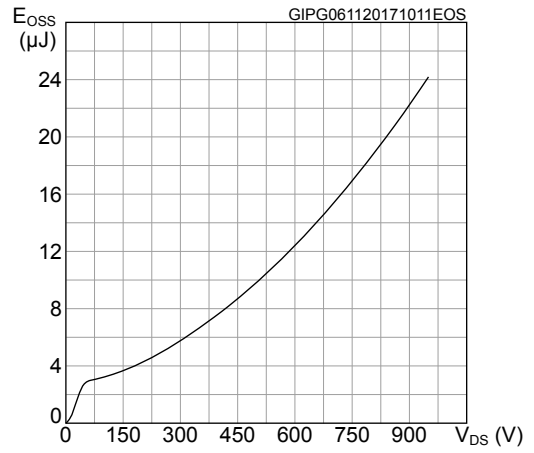


Figure 9. Normalized gate threshold voltage vs temperature

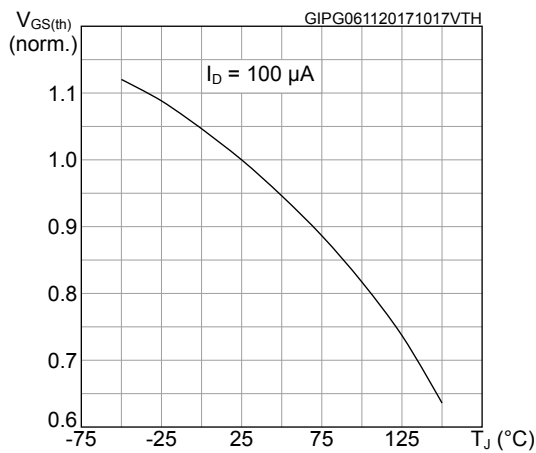


Figure 10. Normalized on-resistance vs temperature

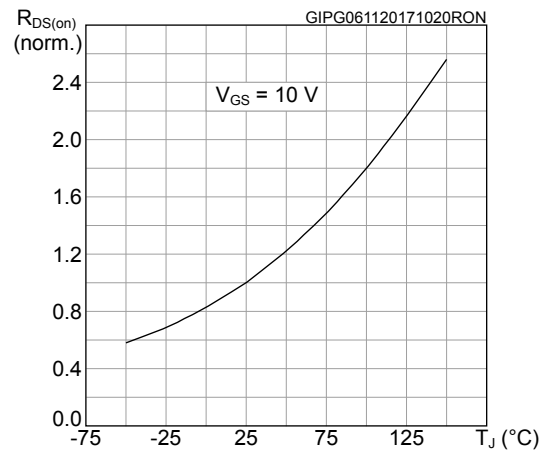


Figure 11. Normalized V_(BR)DSS vs temperature

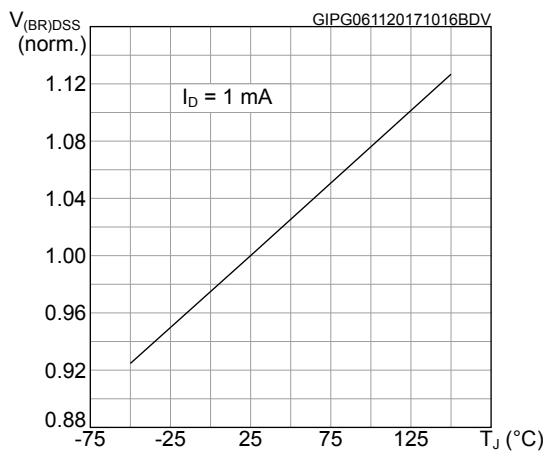


Figure 12. Source-drain diode forward characteristics

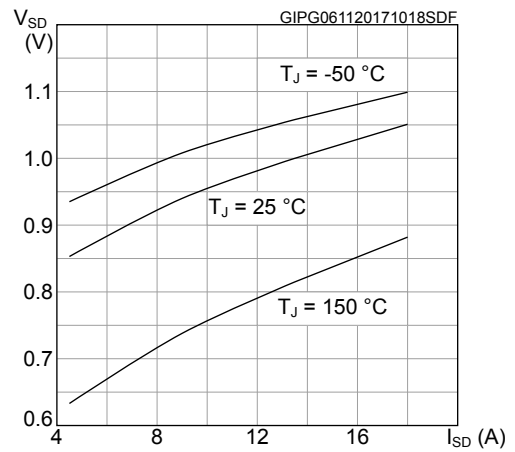
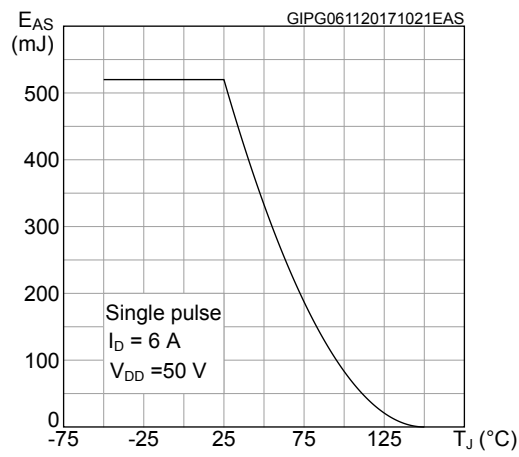
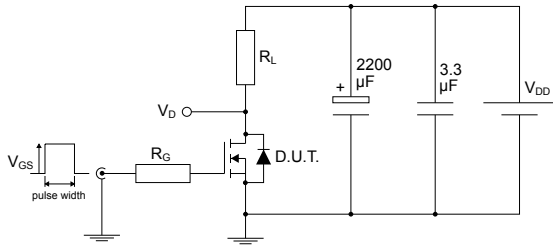


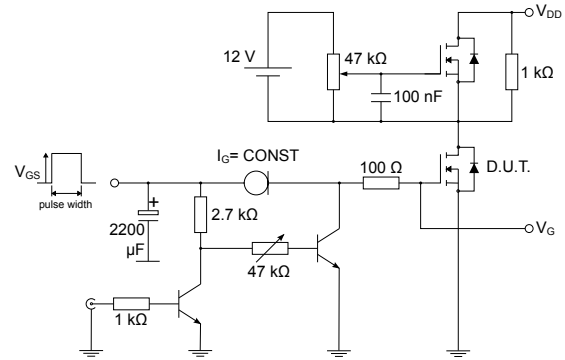
Figure 13. Maximum avalanche energy vs starting T_J



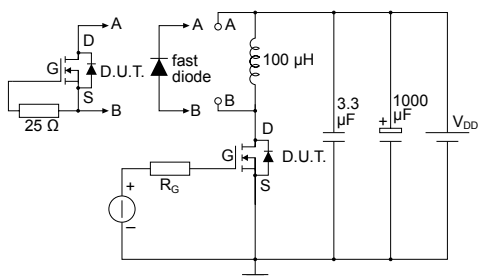
3 Test circuits

Figure 14. Test circuit for resistive load switching times


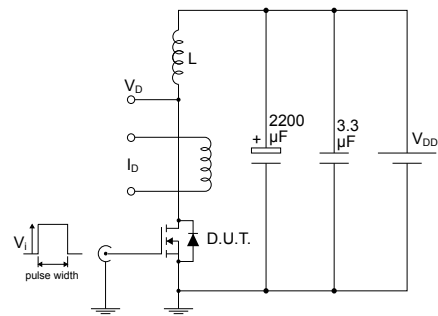
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Figure 15. Test circuit for gate charge behavior


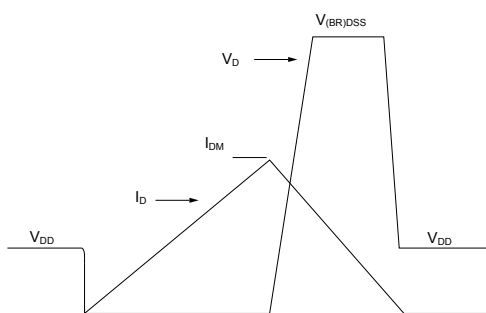
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Figure 16. Test circuit for inductive load switching and diode recovery times


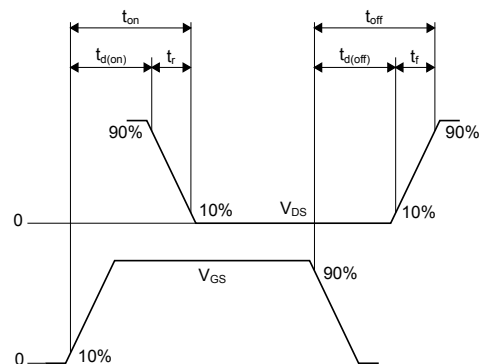
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Figure 17. Unclamped inductive load test circuit


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Figure 18. Unclamped inductive waveform


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Figure 19. Switching time waveform


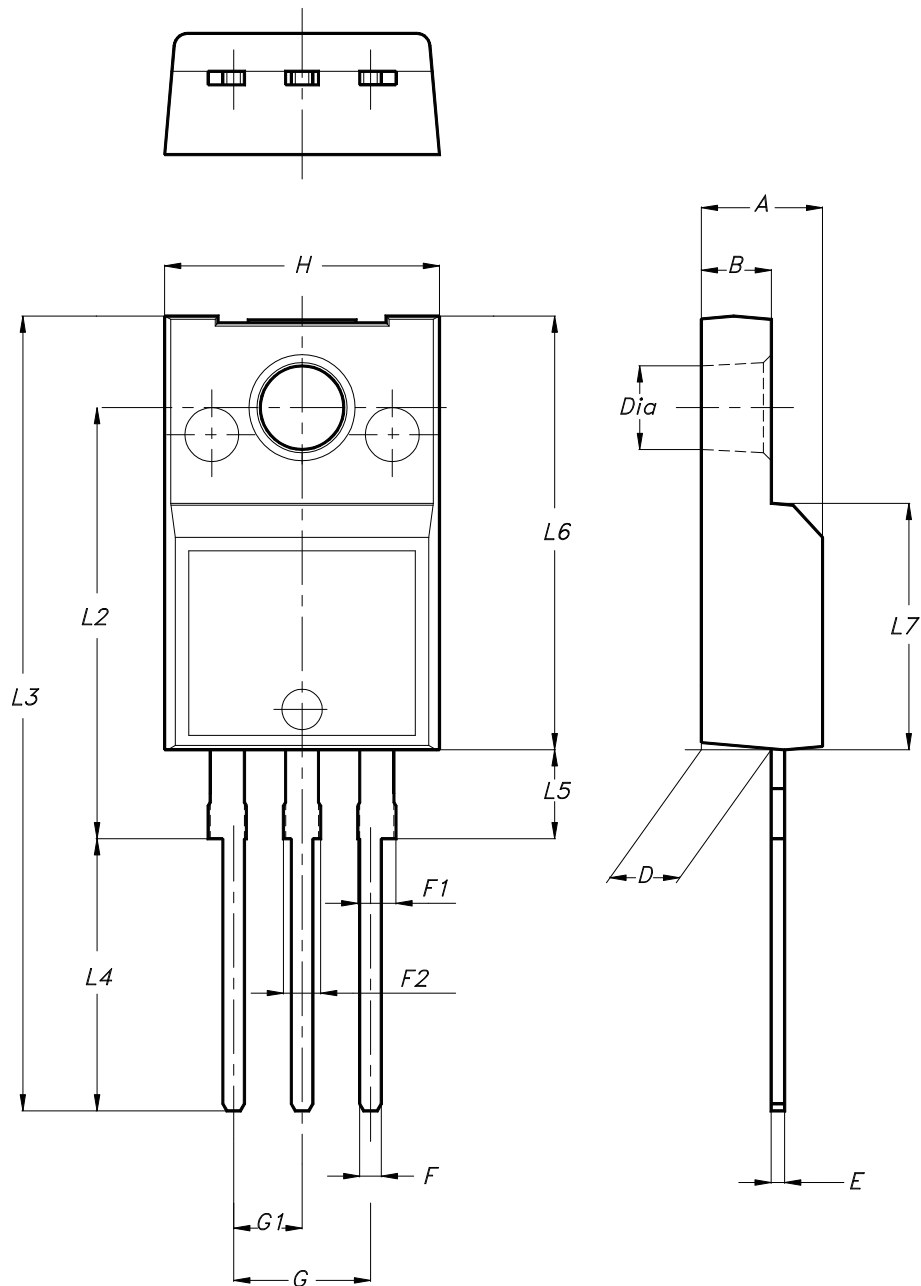
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP package information

Figure 20. TO-220FP package outline



7012510_Rev_13_B

Table 8. TO-220FP package mechanical data

| Dim. | mm | | |
|------|-------|-------|-------|
| | Min. | Typ. | Max. |
| A | 4.40 | | 4.60 |
| B | 2.50 | | 2.70 |
| D | 2.50 | | 2.75 |
| E | 0.45 | | 0.70 |
| F | 0.75 | | 1.00 |
| F1 | 1.15 | | 1.70 |
| F2 | 1.15 | | 1.70 |
| G | 4.95 | | 5.20 |
| G1 | 2.40 | | 2.70 |
| H | 10.00 | | 10.40 |
| L2 | | 16.00 | |
| L3 | 28.60 | | 30.60 |
| L4 | 9.80 | | 10.60 |
| L5 | 2.90 | | 3.60 |
| L6 | 15.90 | | 16.40 |
| L7 | 9.00 | | 9.30 |
| Dia | 3.00 | | 3.20 |

Revision history

Table 9. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 15-May-2020 | 1 | First release. |
| 18-May-2020 | 2 | Updated <i>Features</i> in cover page. |
| 11-Aug-2021 | 3 | Updated Table 1. Absolute maximum ratings. Updated Figure 3. Output characteristics, Figure 4. Transfer characteristics and Figure 6. Static drain-source on-resistance. Minor test changes. |

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