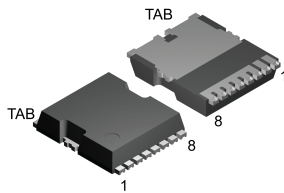
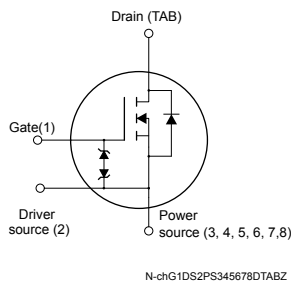


N-channel 600 V, 162 mΩ typ., 17 A, MDmesh M6 Power MOSFET in a TO-LL package



TO-LL type A



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STO24N60M6	600 V	190 mΩ	17 A

- Reduced switching losses
- Lower $R_{DS(on)}$ per area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- LLC converters
- Boost PFC converters

Description

The new MDmesh M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent $R_{DS(on)}$ per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.



Product status link

[STO24N60M6](#)

Product summary

Order code	STO24N60M6
Marking	24N60M6
Package	TO-LL type A
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	17	A
	Drain current (continuous) at $T_C = 100\text{ °C}$	10.7	
$I_{DM}^{(1)}$	Drain current (pulsed)	52.5	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ °C}$	142	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 17\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS}(\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.
3. $V_{DS} \leq 480\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.88	°C/W
R_{thJB}	Thermal resistance, junction-to-board ⁽¹⁾	43	°C/W
	Thermal resistance, junction-to-board ⁽²⁾	22	

1. When mounted on 1 inch² FR-4 pcb, standard footprint 2 Oz copper board.
2. When mounted on 40x40mm FR-4 pcb, 6 cm² 2 Oz copper board.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	3.2	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	250	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}^{(1)}$			100	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 5	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3.25	4.00	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 8.5\text{ A}$		162	190	m Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	960	-	pF
C_{oss}	Output capacitance		-	76	-	pF
C_{rSS}	Reverse transfer capacitance		-	4.5	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$, $V_{GS} = 0\text{ V}$	-	181	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	5	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 17\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	23	-	nC
Q_{gs}	Gate-source charge		-	6.5	-	nC
Q_{gd}	Gate-drain charge		-	11	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 8.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13. Switching times test circuit for resistive load and Figure 18. Switching time waveform)	-	17.7	-	ns
t_r	Rise time		-	32	-	ns
$t_{d(off)}$	Turn-off delay time		-	38.3	-	ns
t_f	Fall time		-	9	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		17	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		52.5	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 17\text{ A}, V_{GS} = 0\text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 17\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$	-	225		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$	-	2.3		μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	20.4		A
t_{rr}	Reverse recovery time	$I_{SD} = 17\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$	-	387		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}, T_J = 150\text{ }^\circ\text{C}$	-	3.85		μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	25.1		A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

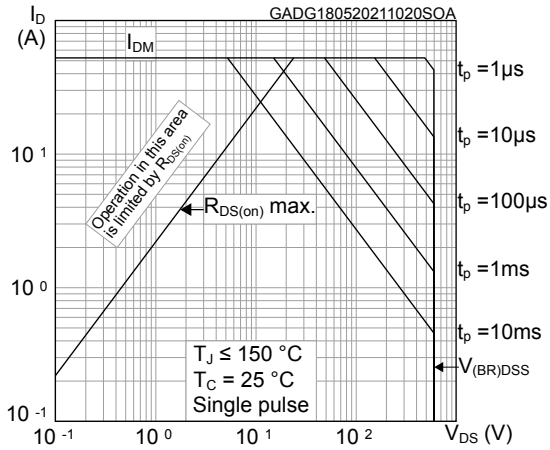


Figure 2. Maximum transient thermal impedance

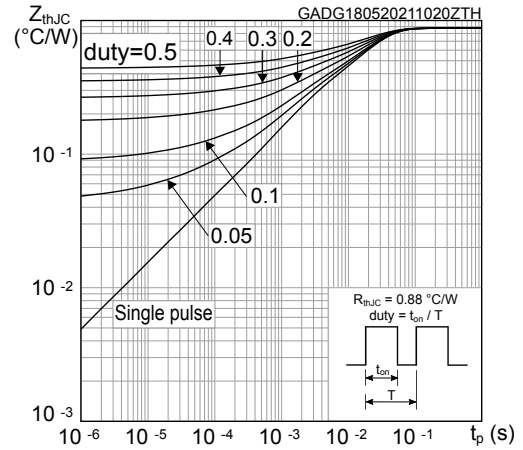


Figure 3. Typical output characteristics

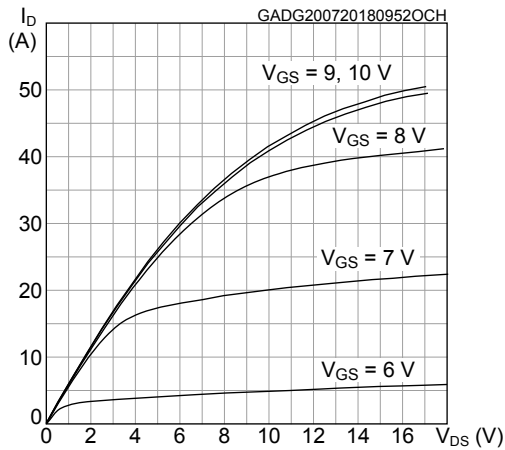


Figure 4. Typical transfer characteristics

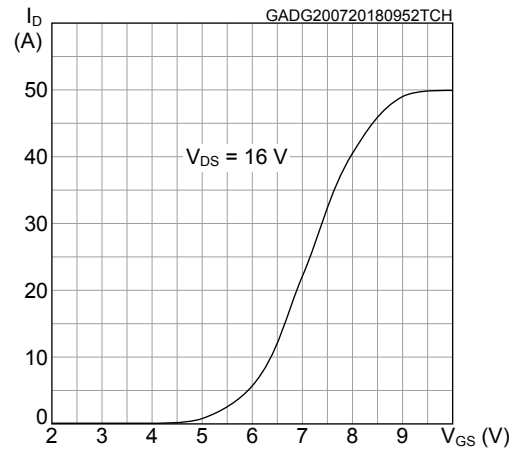


Figure 5. Typical gate charge characteristics

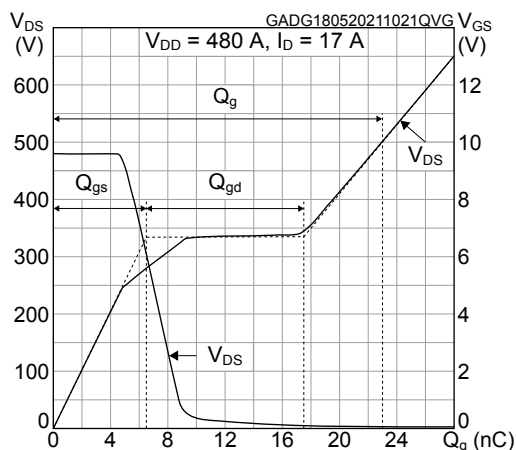


Figure 6. Typical drain-source on-resistance

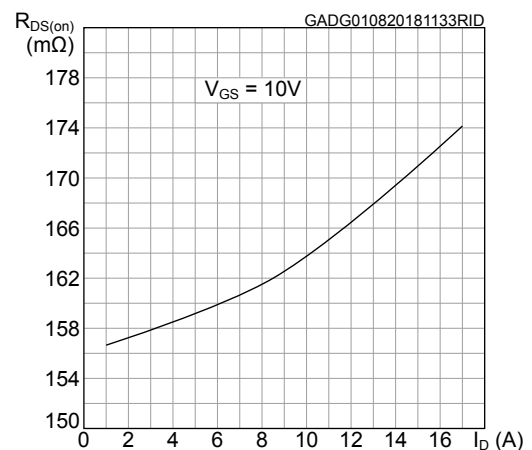


Figure 7. Typical capacitance characteristics

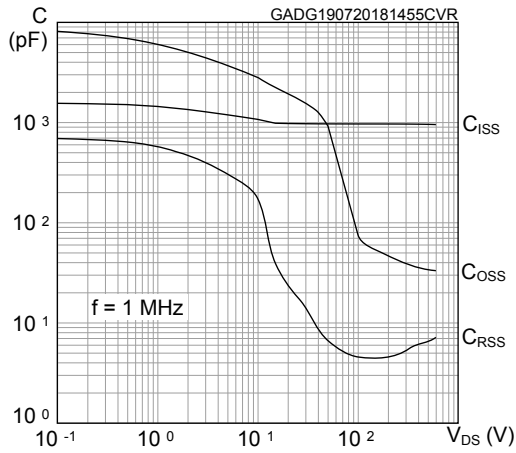


Figure 8. Typical output capacitance stored energy

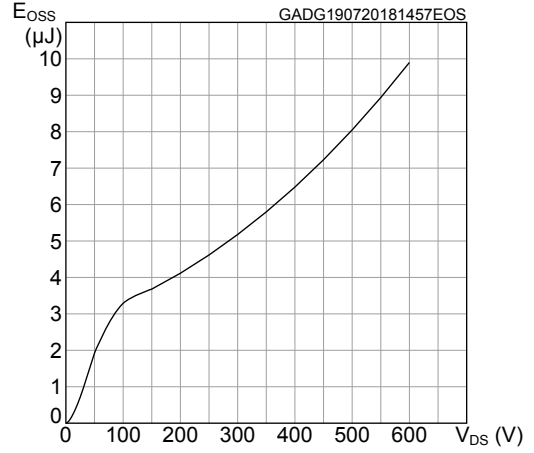


Figure 9. Normalized gate threshold vs temperature

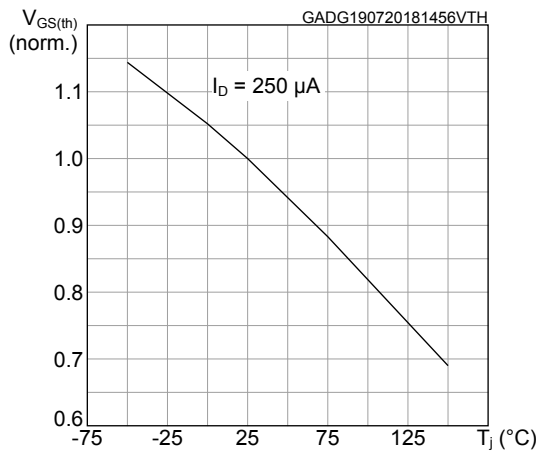


Figure 10. Normalized on-resistance vs temperature

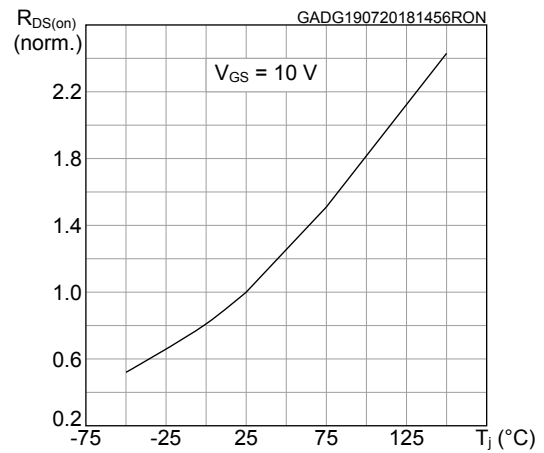


Figure 11. Normalized breakdown voltage vs temperature

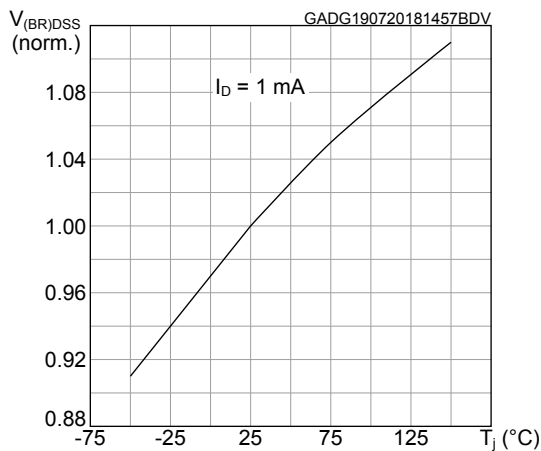
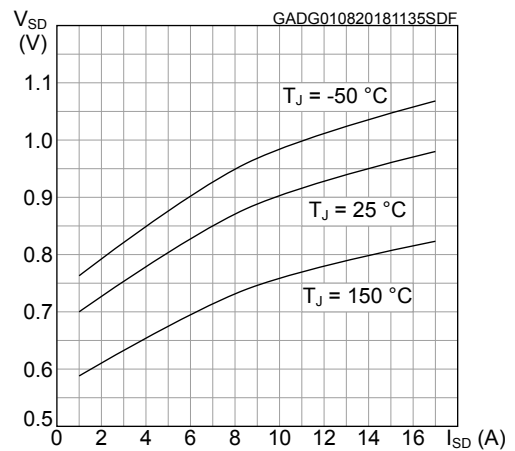
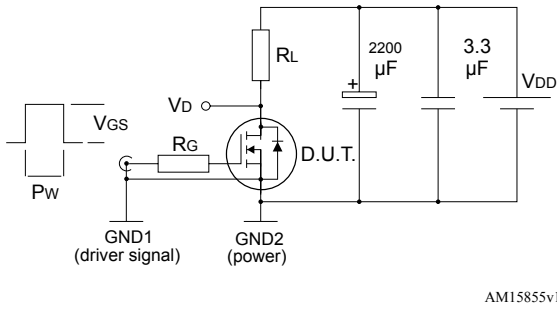
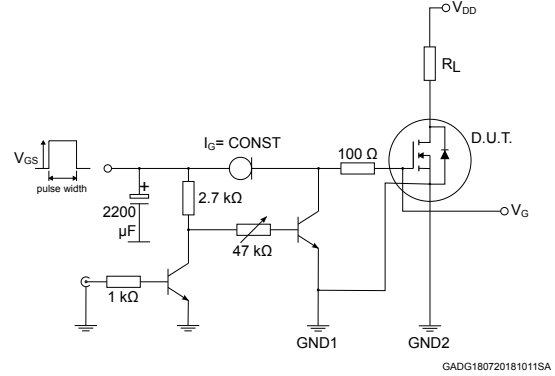
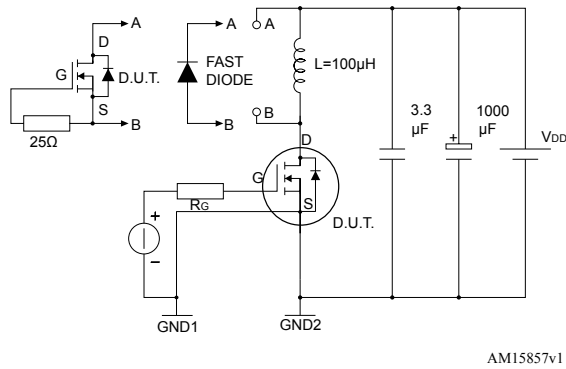
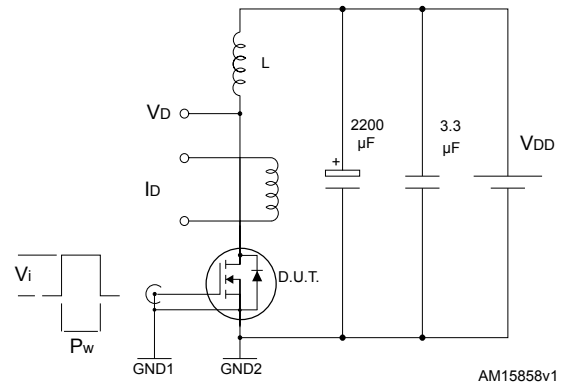
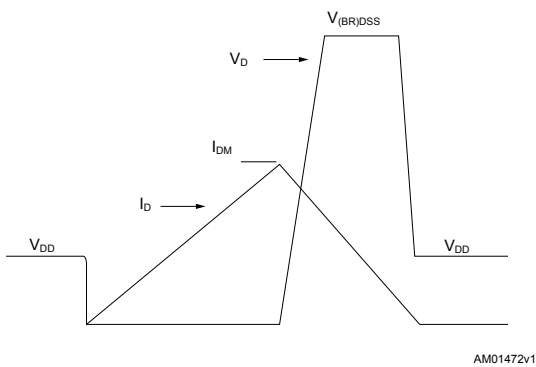
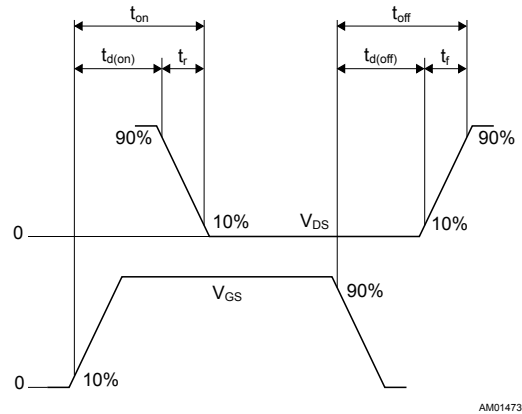


Figure 12. Typical reverse diode forward characteristics



3 Test circuits

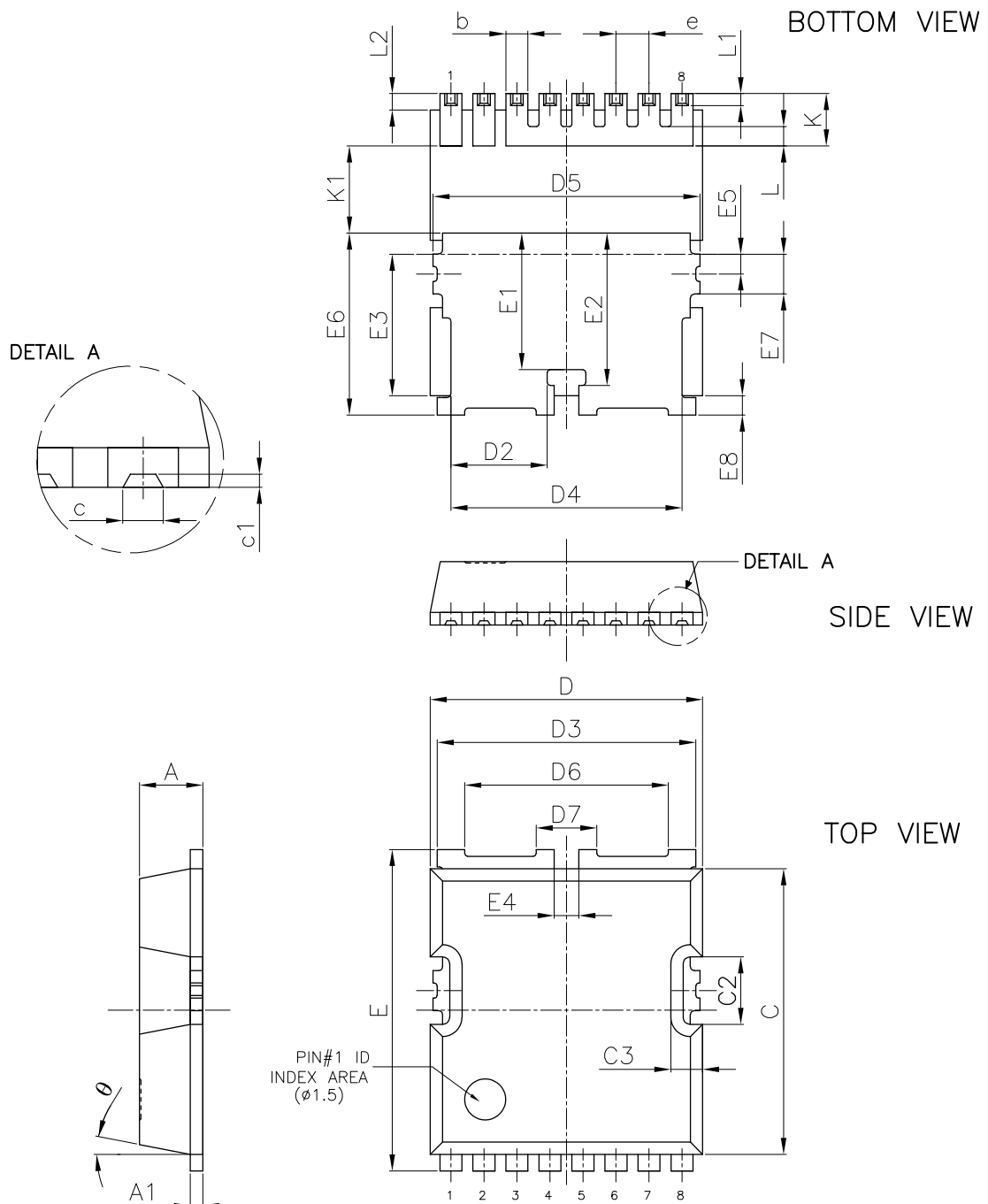
Figure 13. Switching times test circuit for resistive load

Figure 14. Test circuit for gate charge behavior

Figure 15. Test circuit for inductive load switching and diode recovery times

Figure 16. Unclamped inductive load test circuit

Figure 17. Unclamped inductive waveform

Figure 18. Switching time waveform


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-LL type A package information

Figure 19. TO-LL type A package outline

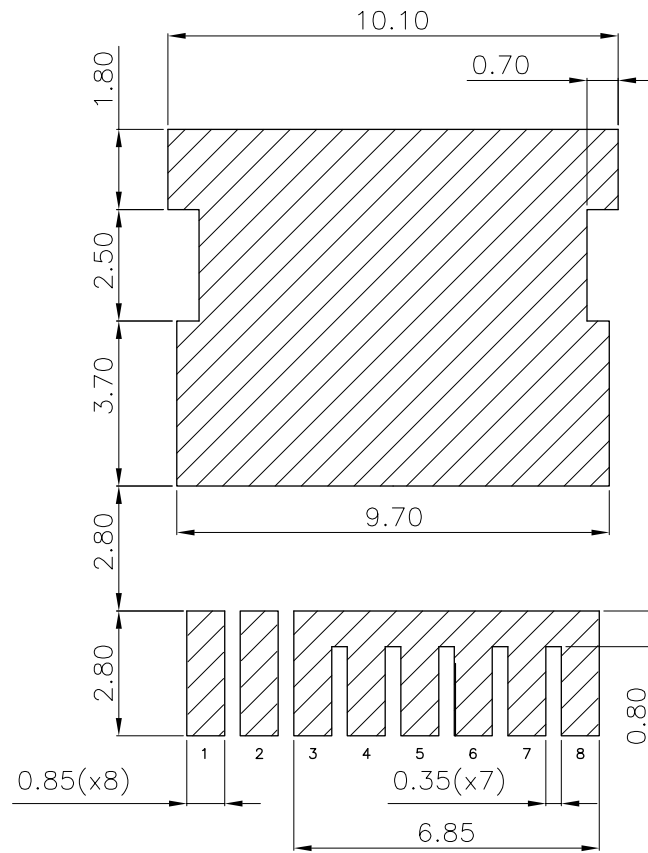


DM00276569_5_type_A

Table 8. TO-LL type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.40
A1	0.40	0.48	0.60
b	0.70	0.80	0.90
c		0.46	
c1		0.15	
C	10.28	10.38	10.48
C2	2.35	2.45	2.55
C3		1.16	
D	9.80	9.90	10.00
D2	3.30	3.50	3.70
D3	9.30	9.40	9.50
D4	8.20	8.40	8.60
D5	9.50	9.70	9.90
D6		7.40	
D7		2.20	
e		1.20	
E	11.48	11.68	11.88
E1		4.96	
E2		5.54	
E3		5.14	
E4		0.90	
E5		0.72	
E6	6.41	6.61	6.81
E7		1.44	
E8	0.50	0.70	0.90
K	1.70	1.90	2.10
K1	2.70		
L		0.70	
L1		0.44	
L2	0.40	0.60	0.80
θ		11°	

Figure 20. TO-LL type A recommended footprint (dimensions are in mm)



DM00276569_5_type_A_FP

4.2 TO-LL packing information

Figure 21. Carrier tape outline and dimensions

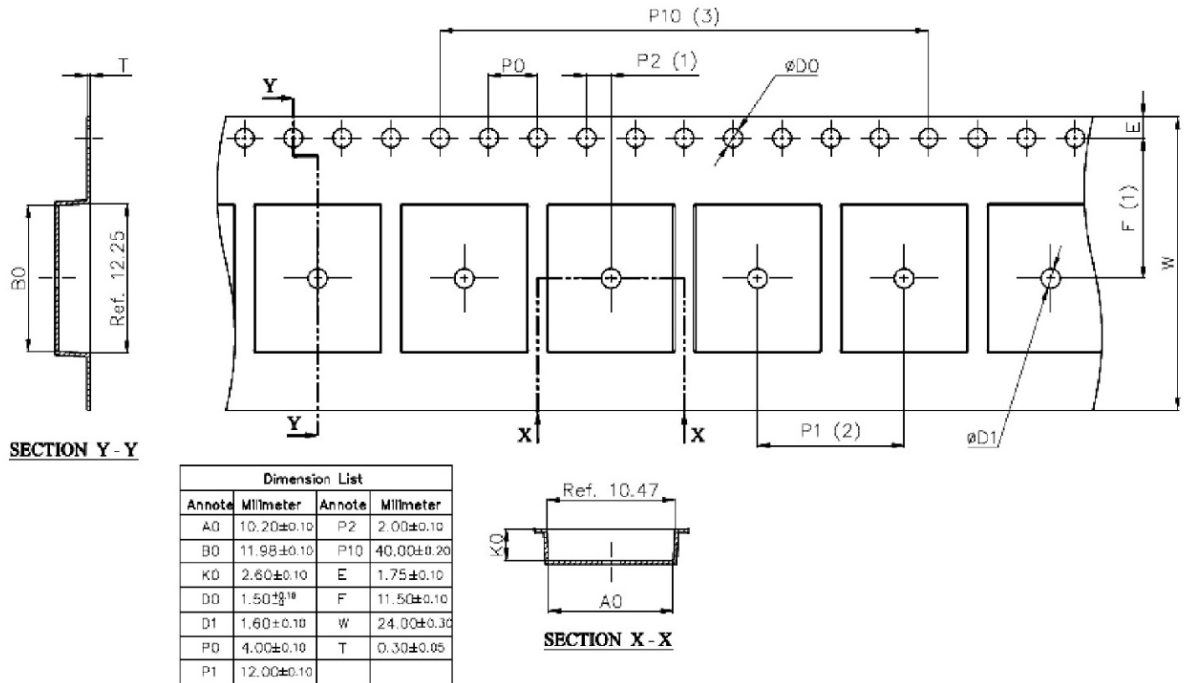


Figure 22. Reel outline and dimensions

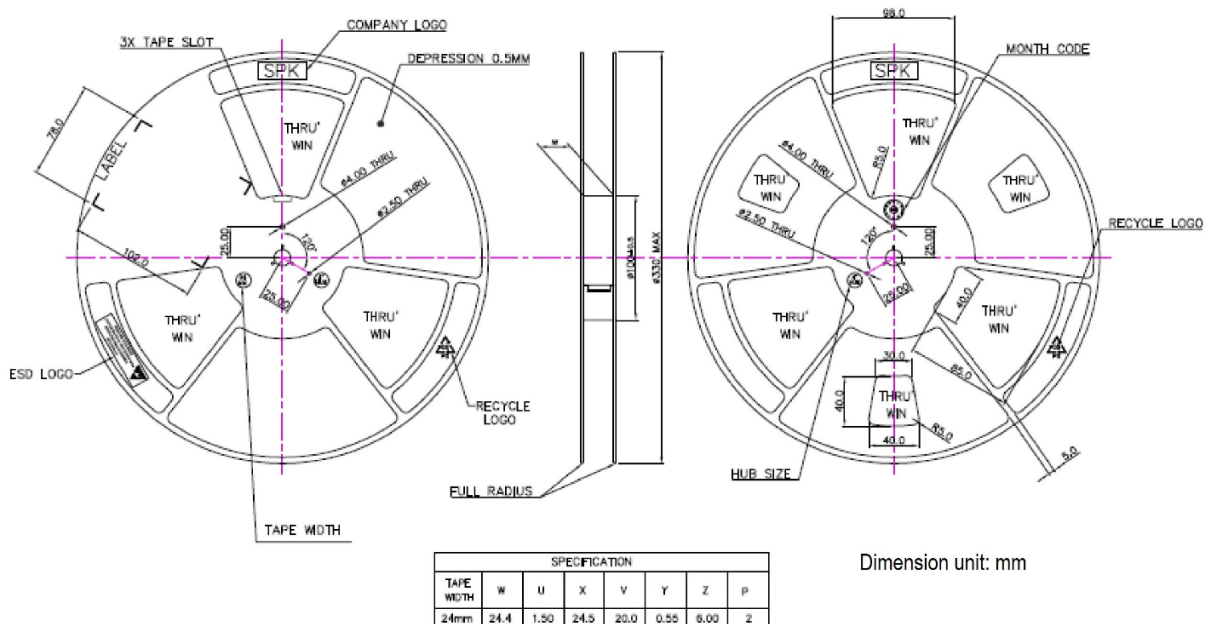
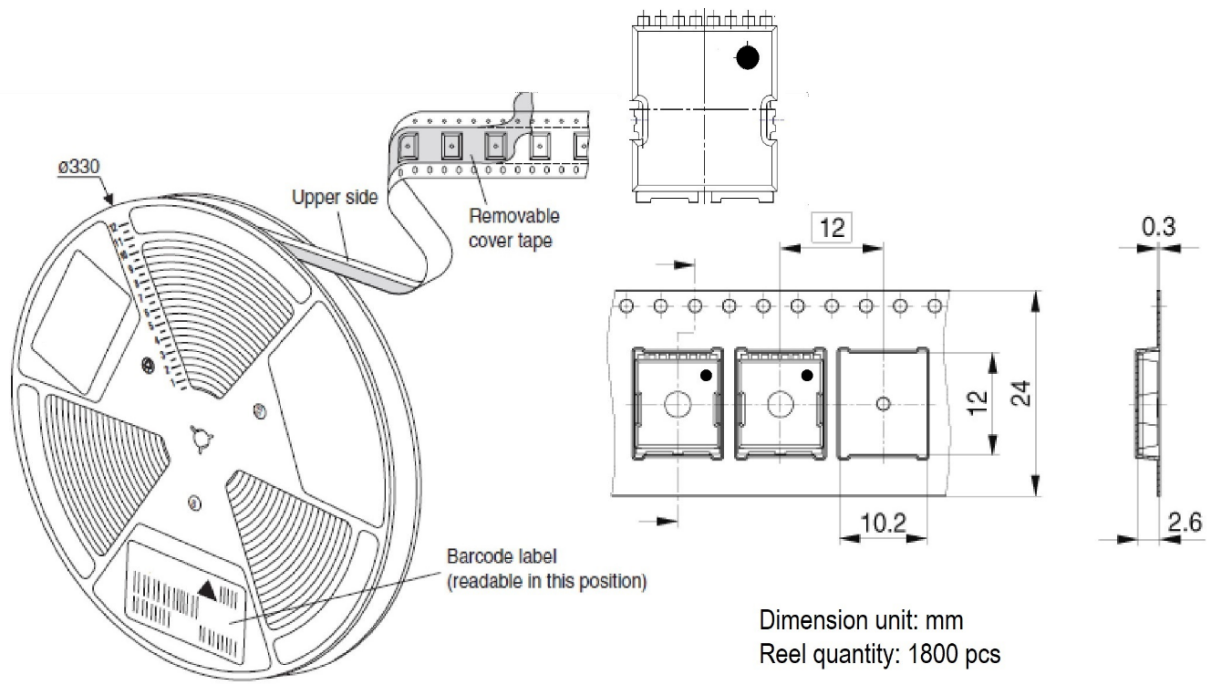


Figure 23. TO-LL orientation in tape pocket



Revision history

Table 9. Document revision history

Date	Version	Changes
20-May-2021	1	First release.

Contents

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2	Electrical characteristics	3
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