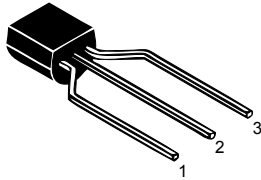
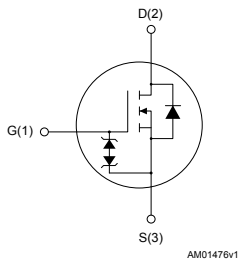


N-channel 600 V, 3.5 Ω typ., 500 mA SuperMESH Power MOSFET in a TO-92 package



TO-92 ammpack



Features

Order codes	V_{DS}	$R_{DS(on)}$ max.	I_D
STQ2Hnk60Zr-AP	600 V	4.8 Ω	500 mA

- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

Applications

- Switching applications

Description

This high-voltage device is a Zener-protected N-channel Power MOSFET developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.



Product status link

[STQ2Hnk60Zr-AP](#)

Product summary

Order code	STQ2Hnk60Zr-AP
Marking	Q2Hnk60Zr
Package	TO-92
Packing	Ampmpack

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	500	mA
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	320	
$I_{DM}^{(1)}$	Drain current (pulsed)	2	A
P_{TOT}	Total power dissipation at $T_L = 25\text{ }^\circ\text{C}$	3	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$, $T_C = 25\text{ }^\circ\text{C}$)	2.5	kV
ESD	Gate-source human body model ($R = 1.5\text{ k}\Omega$, $C = 100\text{ pF}$)	2	kV
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
T_{STG}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_J	Operating junction temperature range		$^\circ\text{C}$

1. Pulse width limited by safe operating area.

2. $I_{SD} \leq 2\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DS}(\text{peak}) \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJL}	Thermal resistance, junction-to-lead	40	$^\circ\text{C}/\text{W}$
R_{thJA}	Thermal resistance, junction-to-ambient	120	$^\circ\text{C}/\text{W}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (t_p limited by T_J max)	2	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$; $V_{DD} = 50\text{ V}$)	120	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}$ ⁽¹⁾			50	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 1\text{ A}$		3.5	4.8	Ω

1. Specified By Design – Not tested in production.

Table 5. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	280		pF
C_{oss}	Output capacitance		-	38		pF
C_{rSS}	Reverse transfer capacitance		-	7		pF
$C_{oss\ eq.}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$, $V_{GS} = 0\text{ V}$	-	30		pF
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 2\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	11	15 ⁽²⁾	nC
Q_{gs}	Gate-source charge		-	2.25		nC
Q_{gd}	Gate-drain charge		-	6		nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

2. Specified By Design – Not tested in production.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 1\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	10	-	ns
t_r	Rise time		-	30	-	ns
$t_{d(off)}$	Turn-off delay time		-	23	-	ns
t_f	Fall time		-	50	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		2	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		8	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 2\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 2\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 20\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	178		ns
Q_{rr}	Reverse recovery charge		-	445		nC
I_{RRM}	Reverse recovery current		-	5		A
t_{rr}	Reverse recovery time	$I_{SD} = 2\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 20\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	200		ns
Q_{rr}	Reverse recovery charge		-	500		nC
I_{RRM}	Reverse recovery current		-	5		A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

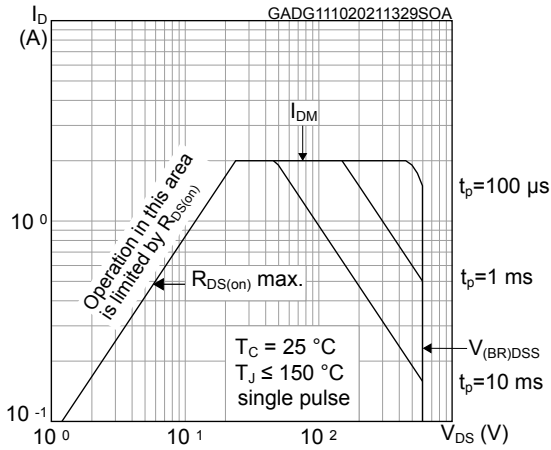


Figure 2. Thermal impedance

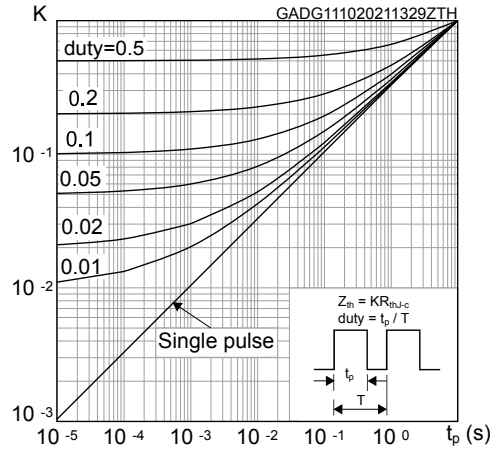


Figure 3. Output characteristics

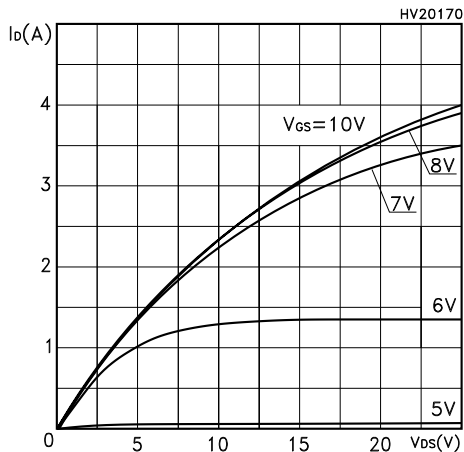


Figure 4. Transfer characteristics

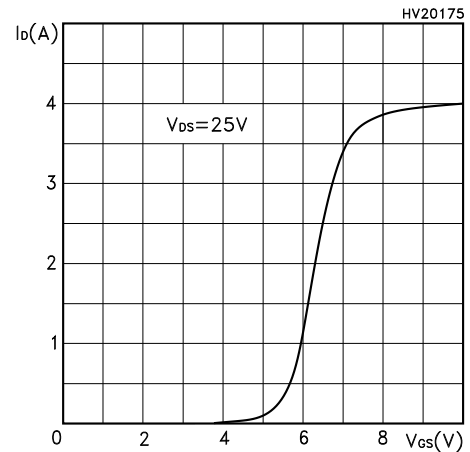


Figure 5. Normalized $V_{(BR)DSS}$ vs temperature

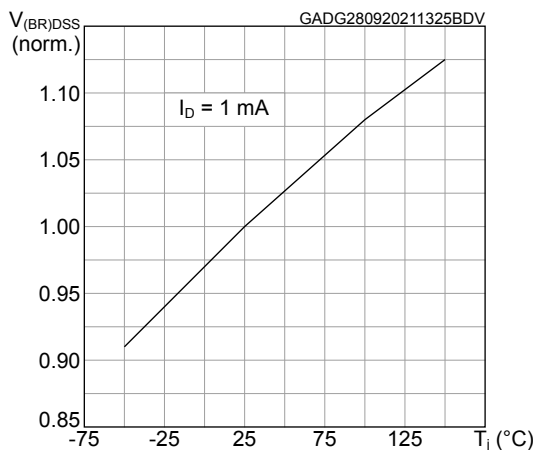


Figure 6. Static drain-source on-resistance

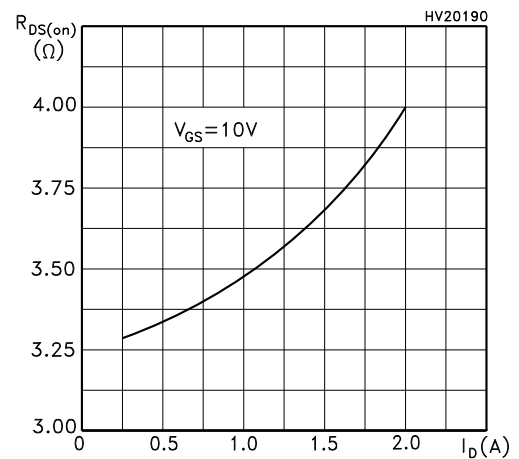


Figure 7. Gate charge vs gate-source voltage

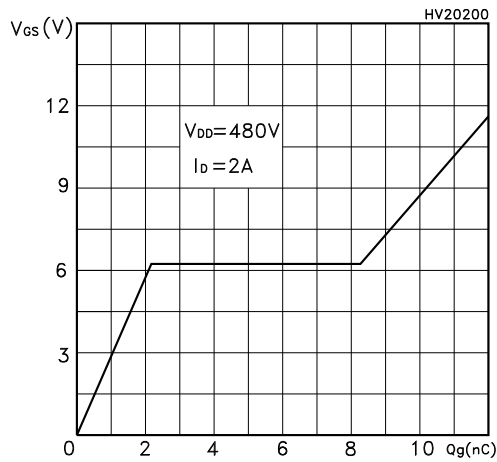


Figure 8. Capacitance variations

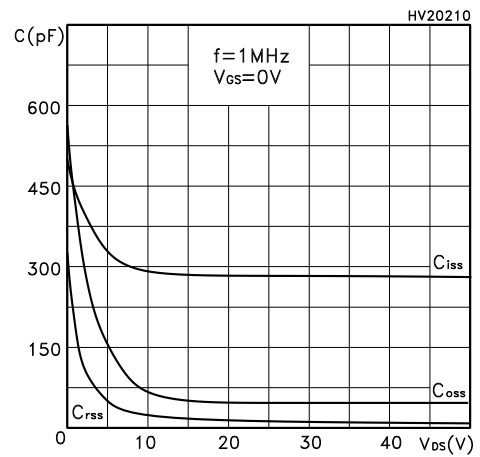


Figure 9. Normalized gate threshold voltage vs temperature

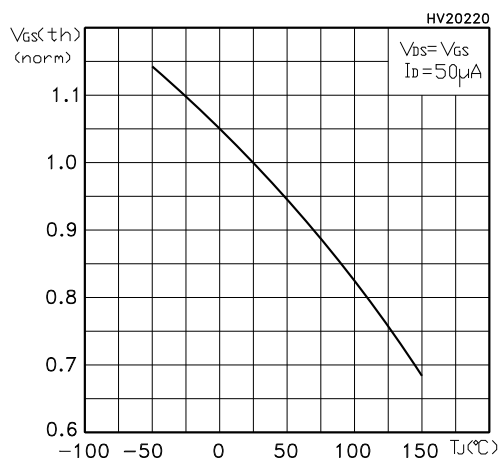


Figure 10. Normalized on-resistance vs temperature

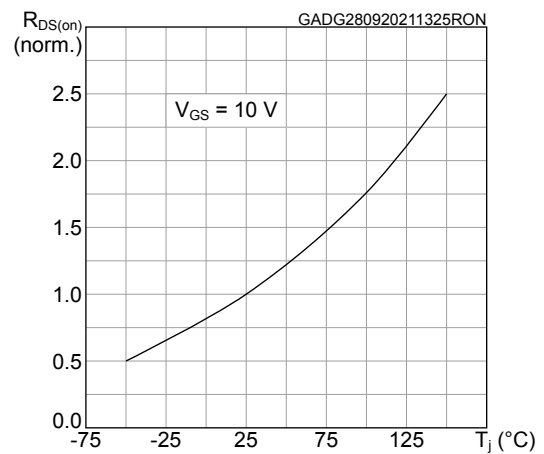


Figure 11. Source-drain diode forward characteristics

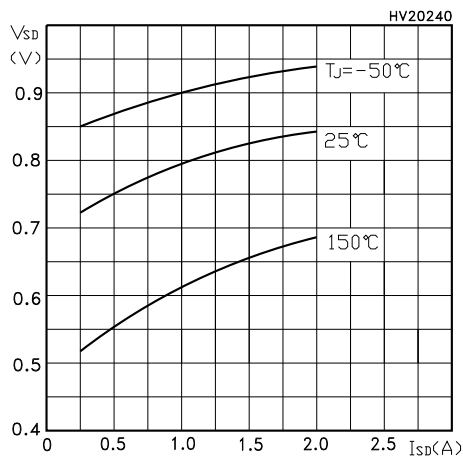
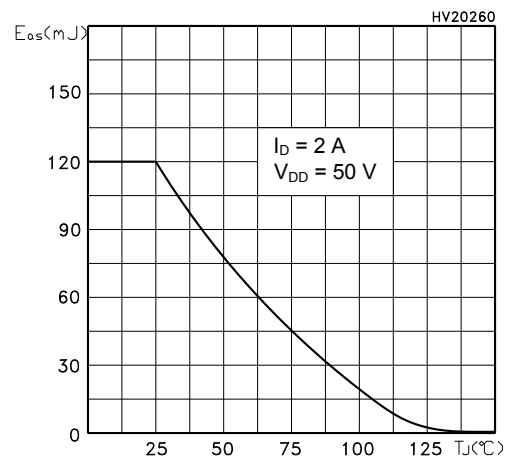
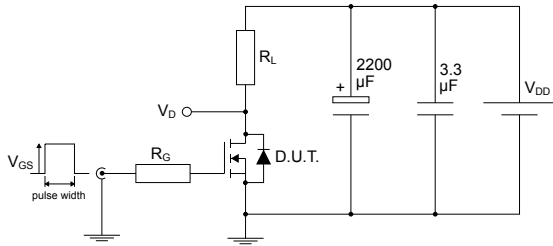


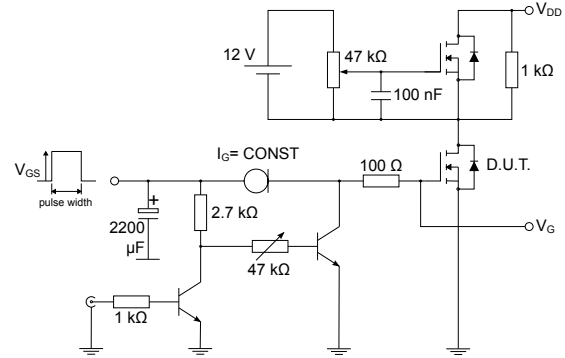
Figure 12. Maximum avalanche energy vs temperature



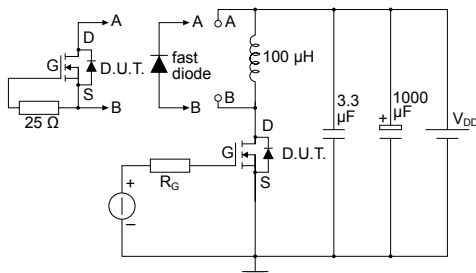
3 Test circuits

Figure 13. Test circuit for resistive load switching times


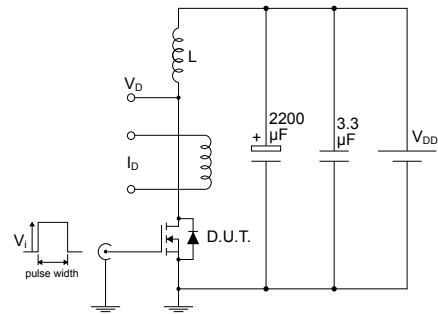
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Figure 14. Test circuit for gate charge behavior


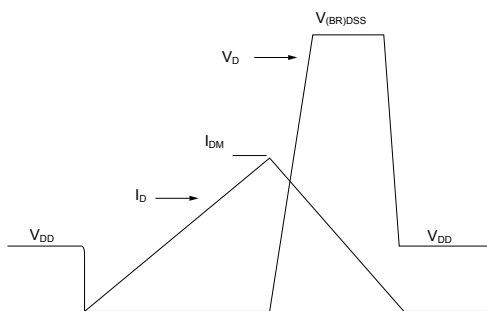
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Figure 15. Test circuit for inductive load switching and diode recovery times


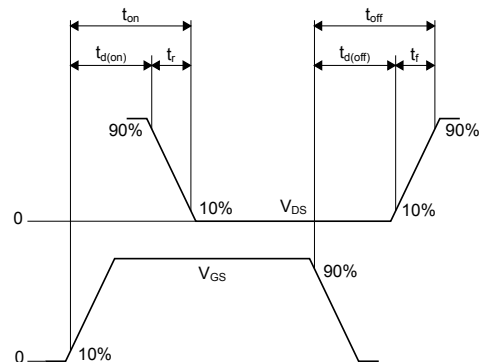
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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


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Figure 18. Switching time waveform


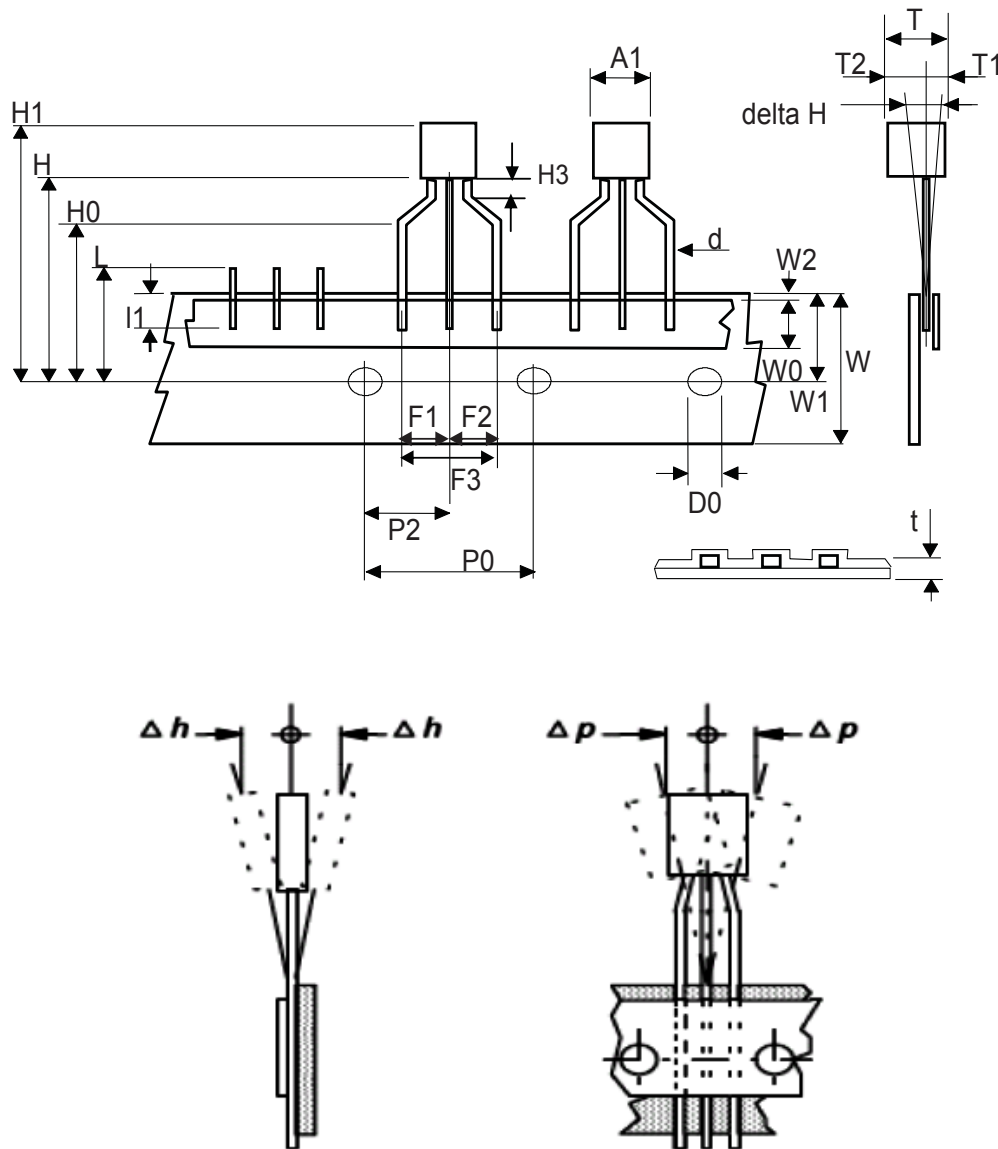
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-92 ammpack package information

Figure 19. TO-92 ammpack package outline



0050910_Rev_22

Table 8. TO-92 ammopack mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A1			4.80
T			3.80
T1			1.60
T2			2.30
d	0.45	0.47	0.48
P0	12.50	12.70	12.90
P2	5.65	6.35	7.05
F1, F2	2.40	2.50	2.94
F3	4.98	5.08	5.48
delta H	-2.00		2.00
W	17.50	18.00	19.00
W0	5.50	6.00	6.50
W1	8.50	9.00	9.25
W2			0.50
H		18.50	21.00
H0	15.50	16.00	18.20
H1		25.00	27.00
H3	0.50	1.00	2.00
D0	3.80	4.00	4.20
t			0.90
L			11.00
I1	3.00		
delta P	-1.00		1.00

Revision history

Table 9. Document revision history

Date	Revision	Changes
12-Oct-2021	1	First release. Part number previously included in datasheet DS3646.

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