SiT1881

Automotive Ultra-Low Power, Low Jitter 32.768kHz Oscillator

PRELIMINARY

Features

- 32.768 kHz
- AEC-Q100 Grade 2
- Frequency stability from ±50 ppm
- Contact SiTime for ±20 ppm option
- Small Oscillator Footprint: 1.32 mm^2
  - 1.2 x 1.1 mm QFN
- Ultra-low power: 490 nA typical @ fout = 32.768 kHz
- Supply voltage: 1.14 V to 1.98 V
- Operating temperature range: from -40°C to +105°C
- Pb-free, RoHS and REACH compliant

Applications

- Automotive Advanced Driver Assistance Systems
- Automotive Infotainment Systems
- Automotive Smart Mirrors
- Industrial Applications

For aerospace and defense applications, SiTime recommends using only Endura™ products.

Block Diagram

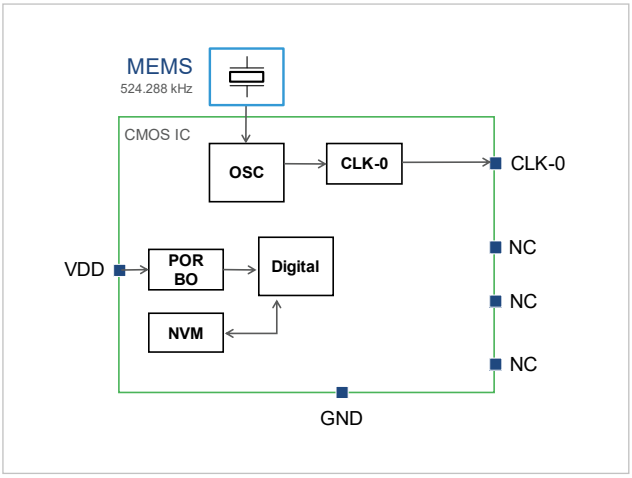


Figure 1. SiT1881 Block Diagram

1.2 x 1.1 mm Package Pinout

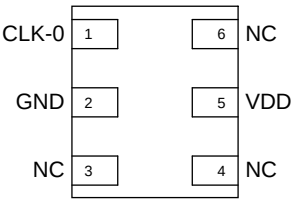
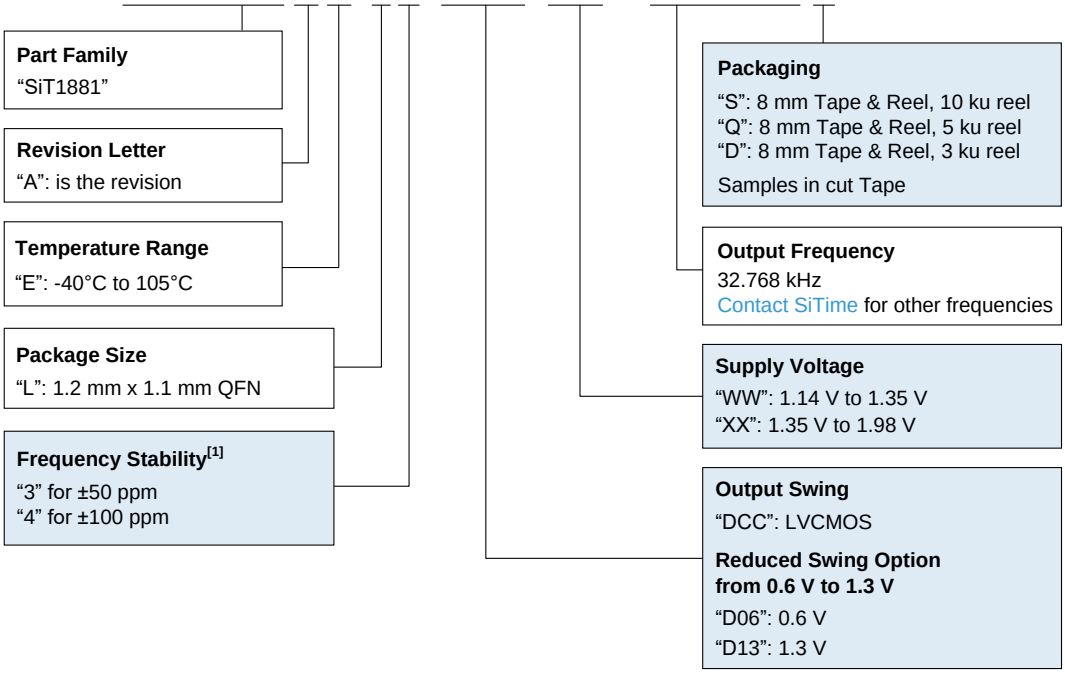


Figure 2. Pin Assignments (Top view)
(Refer to Table 3 for Pin Descriptions)

Ordering Information

SiT1881AE-L**3**-**DCC**-**XX**0-032.768**S**



Note:

1. Contact SiTime for ±20 ppm option.

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Electrical Characteristics

Table 1. Electrical Characteristics

Conditions: Min/Max limits are over temperature, V_{DD} = 1.8 V ±10%, unless otherwise stated.
Typical are at 30°C and V_{DD} = 1.8 V.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency and Stability						
Output Frequency	F_{OUT}		32.768		kHz	Default 32.768 kHz Output. Factory Programmable to other frequencies, where fout=2^n, n = 0 – 18 (default n=15). Contact SiTime for other frequencies
Initial Frequency Tolerance	F_tol	-10	–	+10	ppm	Includes 2x reflow, at 30°C
Frequency Stability[2]	F_stab	-20	–	+20	ppm	Contact SiTime for ±20 ppm option
		-50	–	50		Ordering Code "3": Over temperature, V_{DD}, aging, board-level underfill, and 20% load variation.
		-100	–	100		Ordering Code "4": Over temperature, V_{DD}, aging, board-level underfill, and 20% load variation.
Jitter Performance						
Integrated Phase Jitter	IPJ	–	3	9	ns_{RMS}	F_{OUT} = 32 kHz. Integration bandwidth = 100 Hz to 16 kHz. Inclusive of 50 mV peak-to-peak sinusoidal noise on V_{DD}. Noise frequency 100 Hz to 20 MHz. Contact SiTime for lower jitter performance.
RMS Period Jitter	PJ	–	2.5	8	ns_{RMS}	Cycles = 10,000, f = 32.768 kHz. Per JEDEC standard 65B
Supply Voltage and Current Consumption						
Operating Supply Voltage	V_{DD}	1.14	–	1.365	V	Ordering Code: WW
	V_{DD}	1.35	–	1.98	V	Ordering Code: XX
No Load Supply Current	I_{DD}	–	490	600	nA	Fout = 32.768 kHz, VDD = 1.8 V; -40°C to 85°C
		–	490	800		Fout = 32.768 kHz, VDD = 1.8 V; -40°C to 105°C
Start-up Time at Power-up	t_start	–	–	100	ms	Measured when supply reaches 90% of final V_{DD} to the first output pulse.
Output Characteristics						
Output Rise/Fall Time	t_R, t_F	–	20	40	ns	15 pF load, 20% to 80% of V_{DD} for LVCMOS. 20% to 80% of V_{OH} for Reduced Swing outputs. Factory Programmable Rise/Fall times. Contact SiTime for details.
Output Clock Duty Cycle	DC	45	–	55	%	
LVCMOS Output						
Output Voltage High	VOH	90%	–		V_{DD}	I_{OH} = -1 µA
Output Voltage Low	VOL	–	–	10%	V_{DD}	I_{OL} = 1 µA
Reduced Swing Output						
Output Voltage High	VOH	0.6	–	1.3	V	I_{OH} = -1 µA. Factory Programmable VOH from 0.6 V to 1.3 V @ 0.1 V steps for V_{DD} > V_{OH}+0.6V
Output Voltage Low	VOL	–	–	0.1	V	I_{OL} = 1 µA
Operating Temperature Range						
Operating Temperature Range	Op_Temp	-40	–	+105	°C	Ordering Code (E); ±50 ppm stability over temperature

Note:

2. Tested with Agilent 53132A frequency counter. Measured with ≥100 ms gate time for accurate frequency measurement.

Table 2. Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameters	Test Conditions	Value	Unit
Continuous Power Supply Voltage Range (V_{DD})		-0.5 to 1.98	V
Continuous Maximum Operating Temperature Range		125	°C
Short Duration Maximum Operating Temperature Range	≤ 30 minutes	130	°C
Human Body Model (HBM) ESD Protection	JESD22-A114	2000	V
Charge-Device Model (CDM) ESD Protection	JESD22-C101	500	V
Machine Model (MM) ESD Protection	JESD22-A115	200	V
Latch-up Tolerance	JESD78 Compliant		
Mechanical Shock Resistance	Mil 883, Method 2002	10,000	*g*
Mechanical Vibration Resistance	Mil 883, Method 2007	100	*g*
Max Junction Temperature		130	°C
Storage Temperature		-65 to 150	°C

Table 3. Pin Configuration

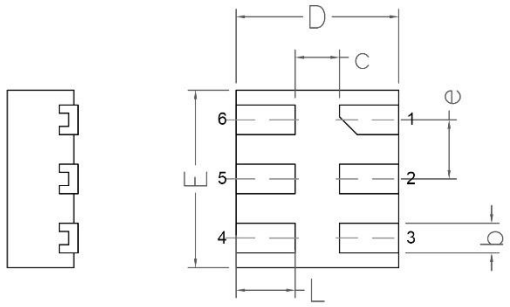
Pin	Symbol	I/O	Functionality
1	CLK-0	Out	Oscillator Clock Output
2	GND	Power Supply Ground	Connect to Ground
3	NC	NC	No Connect
4	NC	NC	No Connect
5	VDD	Power Supply	Device supply voltage. Under normal operating conditions, VDD does not require external bypass/decoupling capacitor(s). SiT1881 includes on-chip VDD filtering.
6	NC	NC	No Connect

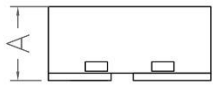
Table 4. Environmental Compliance

Parameter	Condition/Test method
AEC-Q100	**Grade 2**

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)





POD BOTTOM VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.45	0.50	0.55
BODY SIZE	X	D	1.05	1.10	1.15
	Y	E	1.15	1.20	1.25
LEAD WIDTH		b	0.15	0.20	0.25
LEAD LENGTH		L	0.35	0.40	0.45
LEAD PITCH		e	0.35	0.40	0.45
LEAD TO LEAD GAP		c	0.25	0.30	0.35

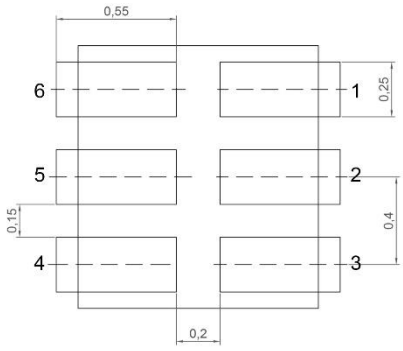
NOTE:

1. ALL DIMENSION IN MM

SiTime

PKG INFO		DRAWING NO.
6L QFN 1.20 x 1.10 x 0.55 mm		POD-088-QFN-06-X1211
		REV
DATE	2021/08/11	A00

Recommended Land Pattern (Unit: mm)



Note: All units in mm.

SiTime	PKG INFO	SPL DRAWING NO.
	6L QFN 1.20 x 1.10 mm	SPL-088-QFN-06-X01211
DATE		REV
2021/08/23		A00

Layout Guidelines

Sample PCB layout is shown in the following figure. It is strongly recommended that the PCB designer observe the following layout guidelines:

- Do not connect any of the pads directly to a copper polygon or a wide PCB trace. This may cause bad solder joints due to non-uniform heating transfer during the assembly process
- Provide short length (>0.5 mm) and thin width (≤0.25 mm) traces to each pad and then to the respective copper polygon or wide trace
- Keep mirror symmetry of the traces X-Y planes. This will prevent the rotation effect during reflow
- Keep high-current and high-speed traces away from the oscillator
    - Route high edge-rate and noisy signals at least 1 mm away from clock-out and pin1 signal traces
    - The use of orthogonal routes is recommended to avoid signal coupling

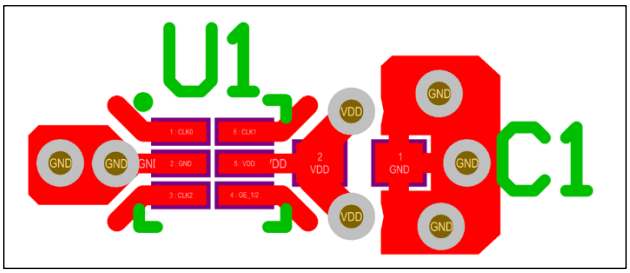


Figure 3. SiT1881 Layout Example

It is recommended to connect VDD and GND pins with polygons or thick wires to corresponding layers of the board. For GND connection it would apply for both device and bypass connections.

- For additional layout recommendations, refer to the Best Design Layout Practices.

Manufacturing Guidelines

The SiT1881 is a precision timing device. Proper PCB solder and cleaning processes must be followed to ensure best performance and long-term reliability.

- For additional manufacturing guidelines and marking/ tape-reel instructions, refer to SiTime Manufacturing Notes.

Revision History

Table 5. Revision History

Version	Release Date	Change Summary
0.1	18-Jun-2021	Advance Datasheet
0.2	20-Jan-2021	Updated Frequency Stability Specification for ±20 ppm over -10°C to 80°C
0.3	17-Feb-2021	Updated Pinout and Package Dimensions
0.4	19-Feb-2021	Corrected Pinout Error in Table 1
0.5	16-Sep-2021	Updated Block Diagram, POD diagram, Ordering table
0.6	5-May-2022	Updated Ordering Code, Updated Current and Jitter Specifications.
0.7	12-Jul-2022	Removed OE functionality
0.8	4-Oct-2022	Updated Disclaimer, updated various electrical specifications
0.95	16-Dec-2022	Supply Voltage and Output Swing changes (Ordering Information and EC table)

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