

## Features

- 32.768 kHz
- AEC-Q100 Grade 2
- Frequency stability from  $\pm 50$  ppm
- [Contact SiTime](#) for  $\pm 20$  ppm option
- Small Oscillator Footprint: 1.32 mm<sup>2</sup>
  - 1.2 x 1.1 mm QFN
- Ultra-low power: 490 nA typical @  $f_{out} = 32.768$  kHz
- Supply voltage: 1.14 V to 1.98 V
- Operating temperature range: from -40°C to +105°C
- Pb-free, RoHS and REACH compliant

## Applications

- Automotive Advanced Driver Assistance Systems
- Automotive Infotainment Systems
- Automotive Smart Mirrors
- Industrial Applications

For aerospace and defense applications, SiTime recommends using only [Endura™ products](#).

## Block Diagram

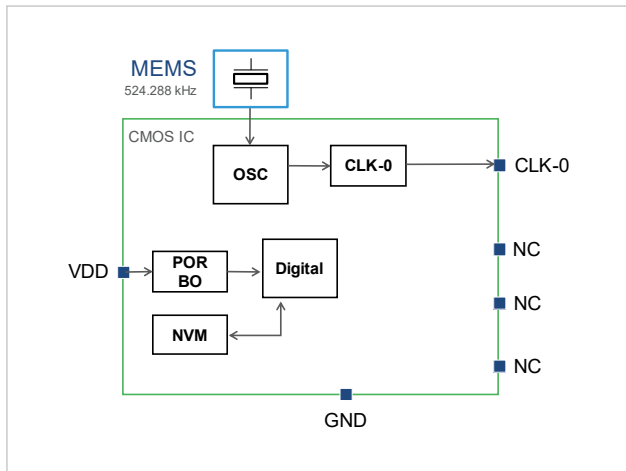


Figure 1. SiT1881 Block Diagram

## 1.2 x 1.1 mm Package Pinout

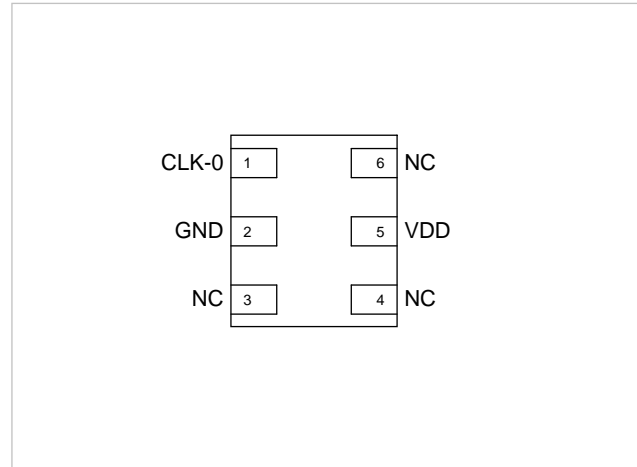
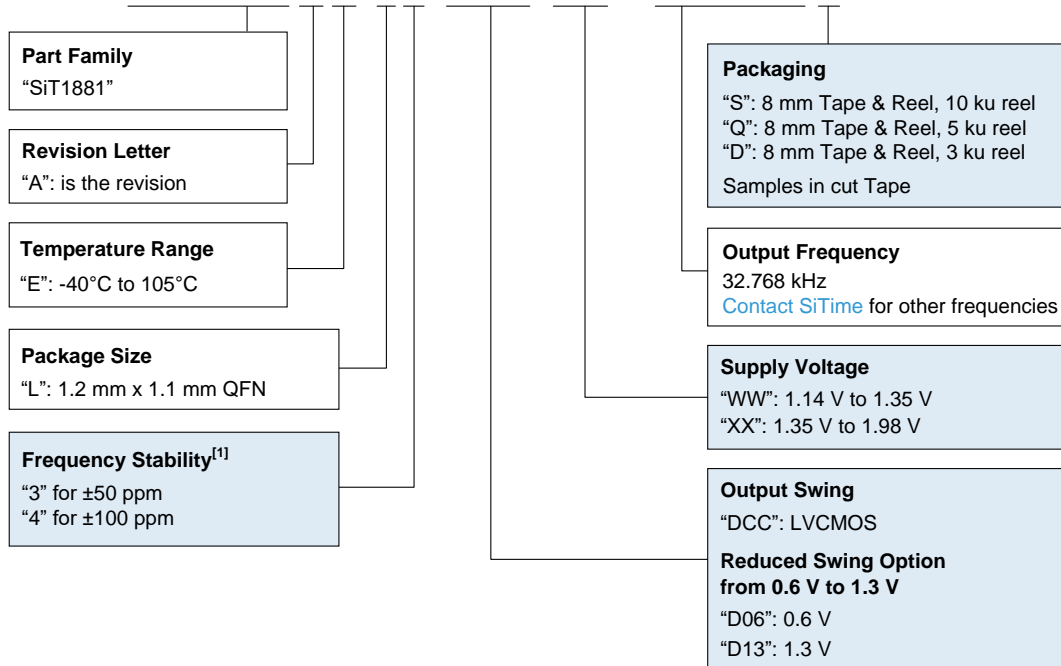


Figure 2. Pin Assignments (Top view)  
(Refer to [Table 3](#) for Pin Descriptions)

## Ordering Information

## SiT1881AE-L3-DCC-XX0-032.768S

**Note:**

1. [Contact SiTime](#) for ±20 ppm option.

---

## Table of Contents

Features.....	1
Applications .....	1
Block Diagram .....	1
1.2 x 1.1 mm Package Pinout.....	1
Ordering Information.....	2
Electrical Characteristics.....	4
Dimensions and Patterns.....	6
Layout Guidelines .....	7
Manufacturing Guidelines .....	7
Revision History.....	8

## SiT1881 Automotive Ultra-Low Power, Low Jitter 32.768kHz Oscillator

## Electrical Characteristics

Table 1. Electrical Characteristics

Conditions: Min/Max limits are over temperature,  $V_{DD} = 1.8 \text{ V} \pm 10\%$ , unless otherwise stated. Typical are at  $30^\circ\text{C}$  and  $V_{DD} = 1.8 \text{ V}$ .

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Frequency and Stability</b>						
Output Frequency	$F_{OUT}$	32.768			kHz	Default 32.768 kHz Output. Factory Programmable to other frequencies, where $f_{out}=2^n$ , $n = 0 - 18$ (default $n=15$ ). <a href="#">Contact SiTime</a> for other frequencies
Initial Frequency Tolerance	$F_{tol}$	-10	–	+10	ppm	Includes 2x reflow, at $30^\circ\text{C}$
Frequency Stability <sup>[2]</sup>	$F_{stab}$	-20	–	+20	ppm	<a href="#">Contact SiTime</a> for $\pm 20$ ppm option
		-50	–	50		Ordering Code "3": Over temperature, $V_{DD}$ , aging, board-level underfill, and 20% load variation.
		-100	–	100		Ordering Code "4": Over temperature, $V_{DD}$ , aging, board-level underfill, and 20% load variation.
<b>Jitter Performance</b>						
Integrated Phase Jitter	IPJ	–	3	9	$\text{ns}_{RMS}$	$F_{OUT} = 32 \text{ kHz}$ . Integration bandwidth = 100 Hz to 16 kHz. Inclusive of 50 mV peak-to-peak sinusoidal noise on $V_{DD}$ . Noise frequency 100 Hz to 20 MHz. <a href="#">Contact SiTime</a> for lower jitter performance.
RMS Period Jitter	PJ	–	2.5	8	$\text{ns}_{RMS}$	Cycles = 10,000, $f = 32.768 \text{ kHz}$ . Per JEDEC standard 65B
<b>Supply Voltage and Current Consumption</b>						
Operating Supply Voltage	$V_{DD}$	1.14	–	1.365	V	Ordering Code: WW
	$V_{DD}$	1.35	–	1.98	V	Ordering Code: XX
No Load Supply Current	$I_{DD}$	–	490	600	nA	$F_{out} = 32.768 \text{ kHz}$ , $V_{DD} = 1.8 \text{ V}$ ; $-40^\circ\text{C}$ to $85^\circ\text{C}$
		–	490	800		$F_{out} = 32.768 \text{ kHz}$ , $V_{DD} = 1.8 \text{ V}$ ; $-40^\circ\text{C}$ to $105^\circ\text{C}$
Start-up Time at Power-up	$t_{start}$	–	–	100	ms	Measured when supply reaches 90% of final $V_{DD}$ to the first output pulse.
<b>Output Characteristics</b>						
Output Rise/Fall Time	$t_r, t_f$	–	20	40	ns	15 pF load, 20% to 80% of $V_{DD}$ for LVCMOS. 20% to 80% of $V_{OH}$ for Reduced Swing outputs. Factory Programmable Rise/Fall times. <a href="#">Contact SiTime</a> for details.
Output Clock Duty Cycle	DC	45	–	55	%	
<b>LVCMOS Output</b>						
Output Voltage High	$V_{OH}$	90%	–		$V_{DD}$	$I_{OH} = -1 \mu\text{A}$
Output Voltage Low	$V_{OL}$	–	–	10%	$V_{DD}$	$I_{OL} = 1 \mu\text{A}$
<b>Reduced Swing Output</b>						
Output Voltage High	$V_{OH}$	0.6	–	1.3	V	$I_{OH} = -1 \mu\text{A}$ . Factory Programmable $V_{OH}$ from 0.6 V to 1.3 V @ 0.1 V steps for $V_{DD} > V_{OH} + 0.6\text{V}$
Output Voltage Low	$V_{OL}$	–	–	0.1	V	$I_{OL} = 1 \mu\text{A}$
<b>Operating Temperature Range</b>						
Operating Temperature Range	Op_Temp	-40	–	+105	$^\circ\text{C}$	Ordering Code (E); $\pm 50$ ppm stability over temperature

## Note:

- Tested with Agilent 53132A frequency counter. Measured with  $\geq 100$  ms gate time for accurate frequency measurement.

**SiT1881** Automotive Ultra-Low Power, Low Jitter 32.768kHz Oscillator

**Table 2. Absolute Maximum Ratings**

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameters	Test Conditions	Value	Unit
Continuous Power Supply Voltage Range ( $V_{DD}$ )		-0.5 to 1.98	V
Continuous Maximum Operating Temperature Range		125	°C
Short Duration Maximum Operating Temperature Range	≤ 30 minutes	130	°C
Human Body Model (HBM) ESD Protection	JESD22-A114	2000	V
Charge-Device Model (CDM) ESD Protection	JESD22-C101	500	V
Machine Model (MM) ESD Protection	JESD22-A115	200	V
Latch-up Tolerance	JESD78 Compliant		
Mechanical Shock Resistance	Mil 883, Method 2002	10,000	<i>g</i>
Mechanical Vibration Resistance	Mil 883, Method 2007	100	<i>g</i>
Max Junction Temperature		130	°C
Storage Temperature		-65 to 150	°C

**Table 3. Pin Configuration**

Pin	Symbol	I/O	Functionality
1	CLK-0	Out	Oscillator Clock Output
2	GND	Power Supply Ground	Connect to Ground
3	NC	NC	No Connect
4	NC	NC	No Connect
5	VDD	Power Supply	Device supply voltage. Under normal operating conditions, VDD does not require external bypass/decoupling capacitor(s). SiT1881 includes on-chip VDD filtering.
6	NC	NC	No Connect

**Table 4. Environmental Compliance**

Parameter	Condition/Test method
AEC-Q100	Grade 2

### Dimensions and Patterns

**Package Size – Dimensions (Unit: mm)**

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.45	0.50	0.55
BODY SIZE	X	D	1.05	1.10	1.15
	Y	E	1.15	1.20	1.25
LEAD WIDTH		b	0.15	0.20	0.25
LEAD LENGTH		L	0.35	0.40	0.45
LEAD PITCH		e	0.35	0.40	0.45
LEAD TO LEAD GAP		c	0.25	0.30	0.35
NOTE:					
1. ALL DIMENSION IN MM					
PKG INFO		DRAWING NO.			
6L QFN 1.20 x 1.10 x 0.55 mm		POD-088-QFN-06-X1211			
DATE		REV			
2021/08/11		A00			

POD BOTTOM VIEW

**Recommended Land Pattern (Unit: mm)**

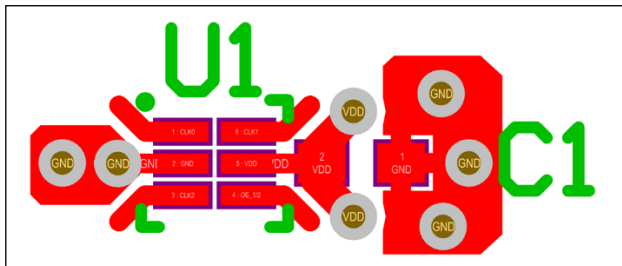
Note: All units in mm.

		PKG INFO	SPL DRAWING NO.
		6L QFN 1.20 x 1.10 mm	SPL-088-QFN-06-X01211
		DATE	REV
2021/08/23		A00	

## Layout Guidelines

Sample PCB layout is shown in the following figure. It is strongly recommended that the PCB designer observe the following layout guidelines:

- Do not connect any of the pads directly to a copper polygon or a wide PCB trace. This may cause bad solder joints due to non-uniform heating transfer during the assembly process
- Provide short length (>0.5 mm) and thin width ( $\leq 0.25$  mm) traces to each pad and then to the respective copper polygon or wide trace
- Keep mirror symmetry of the traces X-Y planes. This will prevent the rotation effect during reflow
- Keep high-current and high-speed traces away from the oscillator
  - Route high edge-rate and noisy signals at least 1 mm away from clock-out and pin1 signal traces
  - The use of orthogonal routes is recommended to avoid signal coupling



**Figure 3. SiT1881 Layout Example**

It is recommended to connect VDD and GND pins with polygons or thick wires to corresponding layers of the board. For GND connection it would apply for both device and bypass connections.

- For additional layout recommendations, refer to the [Best Design Layout Practices](#).

## Manufacturing Guidelines

The SiT1881 is a precision timing device. Proper PCB solder and cleaning processes must be followed to ensure best performance and long-term reliability.

- For additional manufacturing guidelines and marking/tape-reel instructions, refer to [SiTime Manufacturing Notes](#).

## Revision History

**Table 5. Revision History**

Version	Release Date	Change Summary
0.1	18-Jun-2021	Advance Datasheet
0.2	20-Jan-2021	Updated Frequency Stability Specification for $\pm 20$ ppm over $-10^{\circ}\text{C}$ to $80^{\circ}\text{C}$
0.3	17-Feb-2021	Updated Pinout and Package Dimensions
0.4	19-Feb-2021	Corrected Pinout Error in Table 1
0.5	16-Sep-2021	Updated Block Diagram, POD diagram, Ordering table
0.6	5-May-2022	Updated Ordering Code, Updated Current and Jitter Specifications.
0.7	12-Jul-2022	Removed OE functionality
0.8	4-Oct-2022	Updated Disclaimer, updated various electrical specifications
0.95	16-Dec-2022	Supply Voltage and Output Swing changes (Ordering Information and EC table)

**SiTime Corporation**, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | **Phone:** +1-408-328-4400 | **Fax:** +1-408-328-4439

© SiTime Corporation 2021-2022. The information contained herein is subject to change at any time without notice. SiTime assumes no responsibility or liability for any loss, damage or defect of a Product which is caused in whole or in part by (i) use of any circuitry other than which is embodied in a SiTime product, (ii) misuse or abuse including static discharge, neglect or accident, (iii) unauthorized modification or repairs which have been soldered or altered during assembly and are not capable of being tested by SiTime under its normal test conditions, or (iv) improper installation, storage, handling, warehousing or transportation, or (v) being subjected to unusual physical, thermal, or electrical stress.

**Disclaimer:** SiTime makes no warranty of any kind, express or implied, with regard to this material, and specifically disclaims any and all express or implied warranties, either in fact or by operation of law, statutory or otherwise, including the implied warranties of merchantability and fitness for use or a particular purpose, and any implied warranty arising from course of dealing or usage of trade, as well as any common-law duties relating to accuracy or lack of negligence, with respect to this material, any SiTime product and any product documentation. This product is not suitable or intended to be used in a life support application or component, to operate nuclear facilities, in military or aerospace applications, or in other mission critical applications where human life may be involved or at stake. All sales are made conditioned upon compliance with the critical uses policy set forth below.

#### CRITICAL USE EXCLUSION POLICY

BUYER AGREES NOT TO USE THIS PRODUCT FOR ANY APPLICATION OR IN ANY COMPONENTS: USED IN LIFE SUPPORT DEVICES, TO OPERATE NUCLEAR FACILITIES, FOR MILITARY OR AEROSPACE USE, OR IN OTHER MISSION-CRITICAL APPLICATIONS OR COMPONENTS WHERE HUMAN LIFE OR PROPERTY MAY BE AT STAKE.

For aerospace and defense applications, SiTime recommends using only [Endura™ ruggedized products](#).

SiTime owns all rights, title and interest to the intellectual property related to SiTime's products, including any software, firmware, copyright, patent, or trademark. The sale of SiTime products does not convey or imply any license under patent or other rights. SiTime retains the copyright and trademark rights in all documents, catalogs and plans supplied pursuant to or ancillary to the sale of products or services by SiTime. Unless otherwise agreed to in writing by SiTime, any reproduction, modification, translation, compilation, or representation of this material shall be strictly prohibited.