SiT5346 1 MHz – 60 MHz, ±0.1 to ±0.25 ppm, Endura™ Series Precision Super-TCXO

Description

The SiT5346 is a ruggedized ±100 ppb precision MEMS Super-TCXO with a maximum acceleration sensitivity of 0.009 ppb/g or 0.1 ppb/g. Fully compliant to Telcordia GR-1244-CORE Stratum 3 oscillator specifications, and engineered for best dynamic performance, the SiT5346 is ideal for high reliability defense, space, avionics, guidance, precision GNSS and communications applications.

Leveraging SiTime's unique DualMEMS® temperature sensing and TurboCompensation® technologies, the SiT5346 delivers the best dynamic performance for timing stability in the presence of environmental stressors such as air flow, temperature perturbation, vibration, shock, and electromagnetic interference. This device also integrates multiple on-chip regulators to filter power supply noise, eliminating the need for a dedicated external LDO.

The SiT5346 offers three device configurations that can be ordered using Ordering Codes for:

1) TCXO with non-pullable output frequency,
2) VCTCXO allowing voltage control of output frequency,
3) DCTCXO enabling digital control of output frequency using an I²C interface, pullable to 5 ppt (parts per trillion) resolution.

The SiT5346 can be factory programmed for any combination of frequency, stability, voltage, and pull range. Programmability enables designers to optimize clock configurations while eliminating long lead times and customization costs associated with quartz devices where each frequency is custom built.

Refer to Manufacturing Guideline for proper reflow profile and PCB cleaning recommendations to ensure best performance.

Features

- Any frequency from 1 MHz to 60 MHz in 1 Hz steps
- Factory programmable options for short lead time
- Best dynamic stability under airflow, thermal shock
  - 0.009 ppb/g or 0.1 ppb/g acceleration sensitivity
  - ±100 ppb stability across temperature
  - ±1 ppb/°C typical frequency slope (ΔF/ΔT)
  - 1.5e-11 ADEV at 10 second averaging time
- -40°C to +105°C operating temperature
- No activity dips or micro jumps
- Resistant to shock, vibration and board bending
- On-chip regulators eliminate the need for external LDOs
- Digital frequency pulling (DCTCXO) via I²C
  - Digital control of output frequency and pull range
  - Up to ±3200 ppm pull range
  - Frequency pull resolution down to 5 ppt
- 2.5 V, 2.8 V, 3.0 V and 3.3 V supply voltage
- LVCMOS or clipped sinewave output
- RoHS and REACH compliant
- Pb-free, Halogen-free, Antimony-free

Applications

TempFlat MEMS

- Ballistics, missiles, munitions
- Military portable radios
- Ruggedized communications networks
- Precision GNSS systems
- SATCOM
- Transponders
- Military, defense, space, avionics systems

Block Diagram

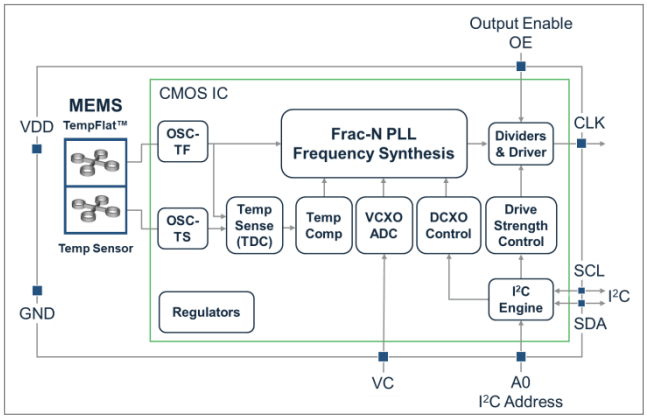


Figure 1. SiT5346 Block Diagram

5.0 mm x 3.2 mm Package Pinout

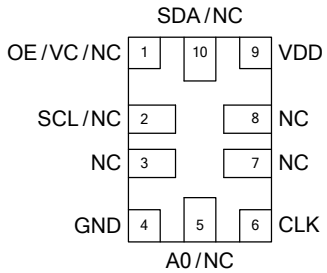
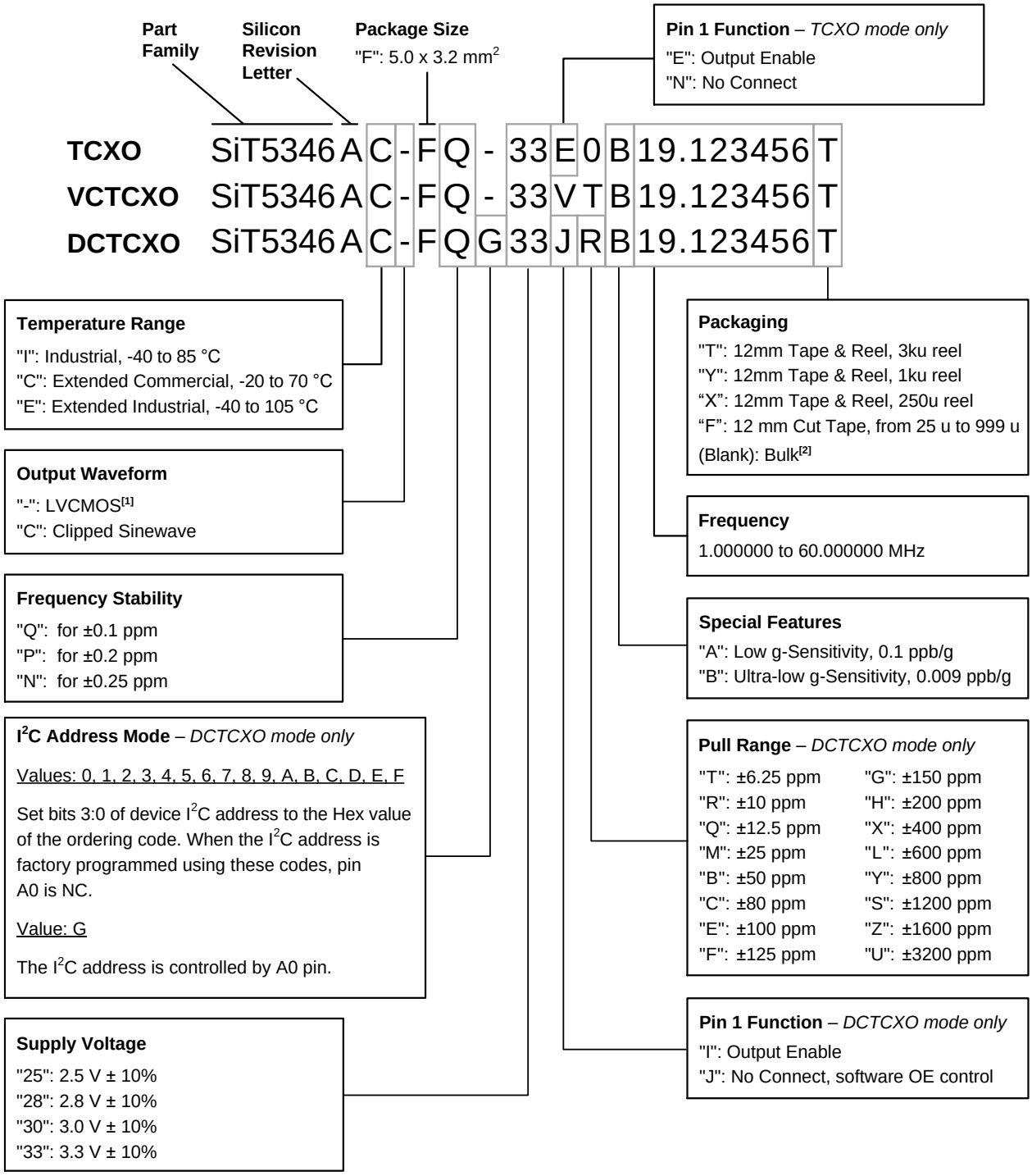


Figure 2. Pin Assignments (Top view)
(Refer to Table 13 for Pin Descriptions)

Ordering Information

The part number guide illustrated below is for reference only. To customize and build an exact part number, use the SiTime Part Number Generator. To validate the part number, use the SiTime Part Number Decoder.



Notes:

1. "-" corresponds to the default rise/fall time for LVCMOS output as specified in Table 1 (Electrical Characteristics). Contact SiTime for other rise/fall time options for best EMI or driving multiple loads. For differential outputs, contact SiTime.
2. Bulk is available for sampling only (up to 24 u).

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Electrical Characteristics

All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at 25°C and 3.3 V Vdd.

Table 1. Output Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Coverage						
Nominal Output Frequency Range	F_nom	1	–	60	MHz	
Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial, ambient temperature
		-40	–	+85	°C	Industrial, ambient temperature
		-40	–	+105	°C	Extended Industrial, ambient temperature
Rugged Characteristics						
Acceleration (g) sensitivity, Gamma Vector	F_g	–	0.004	0.009	ppb/g	Ultra-low sensitivity grade; total gamma over 3 axes; 15 Hz to 2 kHz; MIL-PRF-55310, computed per section 4.8.18.3.1
		–	–	0.1	ppb/g	Low sensitivity grade; total gamma over 3 axes; 15 Hz to 2 kHz; MIL-PRF-55310, computed per section 4.8.18.3.1
Frequency Stability – Stratum 3+ Grade						
Frequency Stability over Temperature	F_stab	–	–	±0.1	ppm	Referenced to (max frequency + min frequency)/2 over the rated temperature range, in TCXO, DCTCXO, or VCTCXO (VCTCXO with ±6.25 ppm pull range, Vc=Vdd/2)
Initial Tolerance	F_init	–	–	±0.3	ppm	Initial frequency at 25°C at 48 hours after 2 reflows
Supply Voltage Sensitivity	F_Vdd	–	±0.5	±2.5	ppb	Vdd ±5%
Output Load Sensitivity	F_load	–	±0.05	±0.4	ppb	LVCMOS output, 15 pF ±10%. Clipped sinewave output, 10 kΩ || 10 pF ±10%
Frequency vs. Temperature Slope	ΔF/ΔT	–	±0.9	±2	ppb/°C	0.5°C/min temperature ramp rate, -20 to 85°C
		–	±1	±3.5	ppb/°C	0.5°C/min temperature ramp rate, -40 to -20°C
		–	±0.9	±3.3	ppb/°C	0.5°C/min temperature ramp rate, 85 to 105°C
Dynamic Frequency Change during Temperature Ramp	F_dynamic	–	±0.008	±0.02	ppb/s	0.5°C/min temperature ramp rate, -20 to 85°C
		–	±0.01	±0.03	ppb/s	0.5°C/min temperature ramp rate, -40 to -20°C
		–	±0.008	±0.028	ppb/s	0.5°C/min temperature ramp rate, 85 to 105°C
24-hour holdover stability	F_24_Hold	–	–	±0.15	ppm	Inclusive of frequency variation due to temperature, ±10% supply variation, ±1.5 pF load variation and 24-hour aging
Hysteresis Over Temperature	F_hys	–	±25	±42	ppb	-40 to 105°C, 0.5°C/min ramp rate, defined as ±ΔF/2 as shown in Figure 19, contact SiTime for lower hysteresis
		–	±15	±27	ppb	-40 to 85°C, 0.5°C/min ramp rate, defined as ±ΔF/2 as shown in Figure 19, contact SiTime for lower hysteresis
		–	±10	±20	ppb	-20 to 70°C, 0.5°C/min ramp rate, defined as ±ΔF/2 as shown in Figure 19, contact SiTime for lower hysteresis
One-Day Aging	F_1d	–	±0.5	±2.0	ppb	At 85°C, after 30-days of continued operation. Aging is measured with respect to day 31.
One-Year Aging	F_1y	–	±57	±230	ppb	At 85°C, after 2-days of continued operation. Aging is measured with respect to day 3.
5-Year Aging	F_5y	–	±73	±320	ppb	
10-Year Aging	F_10y	–	±80	±360	ppb	
20-Year Aging	F_20y	–	±87	±400	ppb	
Allan deviation	ADEV	–	1.5e-11	–	–	10 second averaging time[3]

Table 1. Output Characteristics (continued)

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Stability – Stratum 3 Grade						
Frequency Stability over Temperature	F_stab	–	–	±0.2	ppm	Referenced to (max frequency + min frequency)/2 over the rated temperature range. Vc=Vdd/2 for VCTCXO
		–	–	±0.25	ppm	
Initial Tolerance	F_init	–	–	±1	ppm	Initial frequency at 25°C at 48 hours after 2 reflows
Supply Voltage Sensitivity	F_Vdd	–	±3.0	±6.5	ppb	Vdd ±5%
Output Load Sensitivity	F_load	–	±0.3	±1.1	ppb	LVCMOS output, 15 pF ±10%. Clipped sinewave output, 10 kΩ || 10 pF ±10%
Frequency vs. Temperature Slope	ΔF/ΔT	–	±6.4	±10	ppb/°C	-40 to 105°C
Dynamic Frequency Change during Temperature Ramp	F_dynamic	–	±0.05	±0.08	ppb/s	0.5°C/min temperature ramp rate
24-hour holdover stability	F_24_Hold	–	–	±0.28	ppm	Inclusive of frequency variation due to temperature, ±10% supply variation, ±1.5 pF load variation and 24-hour aging
One-Day Aging	F_1d	–	±3	±5	ppb	At 25°C, after 30-days of continued operation. Aging is measured with respect to day 31
One-Year Aging	F_1y	–	±1	–	ppm	At 25°C, after 2-days of continued operation. Aging is measured with respect to day 3
20-Year Aging	F_20y	–	±2	–	ppm	
20-Year Total Stability	F_tot_20y	–	–	±4.6	ppm	Complies with Stratum 3 per GR-1244-CORE. Actual performance is better
LVCMOS Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Rise/Fall Time	Tr, Tf	0.8	1.2	1.9	ns	10% - 90% Vdd
Output Voltage High	VOH	90%	–	–	Vdd	IOH = +3 mA
Output Voltage Low	VOL	–	–	10%	Vdd	IOL = -3 mA
Output Impedance	Z_out_c	–	17	–	Ohms	Impedance looking into output buffer, Vdd = 3.3 V
		–	17	–	Ohms	Impedance looking into output buffer, Vdd = 3.0 V
		–	18	–	Ohms	Impedance looking into output buffer, Vdd = 2.8 V
		–	19	–	Ohms	Impedance looking into output buffer, Vdd = 2.5 V
Clipped Sinewave Output Characteristics						
Output Voltage Swing	V_out	0.8	–	1.2	V	Clipped sinewave output, 10 kΩ || 10 pF ±10%
Rise/Fall Time	Tr, Tf	–	3.5	4.6	ns	20% - 80% Vdd, F_nom = 19.2 MHz
Start-up Characteristics						
Start-up Time	T_start	–	2.5	3.5	ms	Time to first pulse, measured from the time Vdd reaches 90% of its final value. Vdd ramp time = 100 µs from 0 V to Vdd
Output Enable Time	T_oe	–	–	680	ns	F_nom = 10 MHz. See Timing Diagrams section below
Time to Rated Frequency Stability	T_stability	–	5	45	ms	Time to first accurate pulse within rated stability, measured from the time Vdd reaches 90% of its final value. Vdd ramp time = 100 µs

Note:

3. Measured 2 hours after startup in a temperature chamber with a constant temperature in still air.

Table 2. DC Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage						
Supply Voltage	Vdd	2.25	2.5	2.75	V	Contact SiTime for 2.25 V to 3.63 V continuous supply voltage support
		2.52	2.8	3.08	V	
		2.7	3.0	3.3	V	
		2.97	3.3	3.63	V	
Current Consumption						
Current Consumption	Idd	–	44	53	mA	F_nom = 19.2 MHz, No Load, TCXO and DCTCXO modes
		–	48	57	mA	F_nom = 19.2 MHz, No Load, VCTCXO mode
OE Disable Current	I_od	–	43	51	mA	OE = GND, output weakly pulled down. TCXO, DCTCXO
		–	47	55	mA	OE = GND, output weakly pulled down. VCTCXO mode

Table 3. Input Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Characteristics – OE Pin						
Input Impedance	Z_in	75	–	–	kΩ	Internal pull up to Vdd
Input High Voltage	VIH	70%	–	–	Vdd	
Input Low Voltage	VIL	–	–	30%	Vdd	
Frequency Tuning Range – Voltage Control or I²C mode						
Pull Range	PR	±6.25	–	–	ppm	VCTCXO mode. Contact SiTime for ±12.5 and ±25 ppm
		±6.25 ±10 ±12.5 ±25 ±50 ±80 ±100 ±125 ±150 ±200 ±400 ±600 ±800 ±1200 ±1600 ±3200	–	–	ppm	DCTCXO mode
Absolute Pull Range[3]	APR	±5.31	–	–	ppm	±0.1 ppm F_stab, DCTCXO, VCTCXO for PR = ±6.25 ppm
		±3.05	–	–	ppm	±0.2 ppm F_stab, DCTCXO, VCTCXO for PR = ±6.25 ppm
		±3.00	–	–	ppm	±0.25 ppm F_stab, DCTCXO, VCTCXO for PR = ±6.25 ppm
Upper Control Voltage	VC_U	90%	–	–	Vdd	VCTCXO mode
Lower Control Voltage	VC_L	–	–	10%	Vdd	VCTCXO mode
Control Voltage Input Impedance	VC_z	8	–	–	MΩ	VCTCXO mode
Control Voltage Input Bandwidth	VC_bw	–	10	–	kHz	VCTCXO mode. Contact SiTime for other bandwidth options
Frequency Control Polarity	F_pol	Positive				VCTCXO mode
Pull Range Linearity	PR_lin	–	0.5	1.0	%	VCTCXO mode
I²C Interface Characteristics, 200 Ohm, 550 pF (Max I²C Bus Load)						
Bus Speed	F_I2C	≤ 400			kHz	-40 to 105°C
		≤ 1000			kHz	-40 to 85°C
Input Voltage Low	VIL_I2C	–	–	30%	Vdd	DCTCXO mode
Input Voltage High	VIH_I2C	70%	–	–	Vdd	DCTCXO mode
Output Voltage Low	VOL_I2C	–	–	0.4	V	DCTCXO mode
Input Leakage current	I_L	0.5	–	24	µA	0.1 V_{DD}< VOUT < 0.9 V_{DD}. Includes typical leakage current from 200 kΩ pull resister to VDD. DCTCXO mode
Input Capacitance	C_{IN}	–	–	5	pF	DCTCXO mode

Note:

4. APR = PR – initial tolerance – 20-year aging – frequency stability over temperature. Refer to Table 17 for APR with respect to other pull range options.

Table 4. Jitter & Phase Noise – LVCMOS, -40°C to 85°C

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Jitter						
RMS Phase Jitter (random)	T_phj	–	0.31	0.48	ps	F_nom = 10 MHz, Integration bandwidth = 12 kHz to 5 MHz
		–	0.31	0.48	ps	F_nom = 50 MHz, Integration bandwidth = 12 kHz to 20 MHz
RMS Period Jitter	T_jitt_per	–	0.8	1.1	ps	F_nom = 10 MHz, population 10 k
Peak Cycle-to-Cycle Jitter	T_jitt_cc	–	6	9	ps	F_nom = 10 MHz, population 1 k, measured as absolute value
Phase Noise						
1 Hz offset		–	-80	-74	dBc/Hz	F_nom = 10 MHz TCXO and DCTCXO modes, and VCTCXO mode with ±6.25 ppm pull range
10 Hz offset		–	-108	-102	dBc/Hz	
100 Hz offset		–	-127	-123	dBc/Hz	
1 kHz offset		–	-148	-145	dBc/Hz	
10 kHz offset		–	-154	-151	dBc/Hz	
100 kHz offset		–	-154	-150	dBc/Hz	
1 MHz offset		–	-167	-163	dBc/Hz	
5 MHz offset		–	-168	-164	dBc/Hz	
Spurious	T_spur	–	-112	-105	dBc	F_nom = 10 MHz, 1 kHz to 5 MHz offsets

Table 5. Jitter & Phase Noise – Clipped Sinewave, -40°C to 85°C

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Jitter						
RMS Phase Jitter (random)	T_phj	–	0.31	0.45	ps	F_nom = 19.2 MHz, Integration bandwidth = 12 kHz to 5 MHz
		–	0.31	0.48	ps	F_nom = 60 MHz, Integration bandwidth = 12 kHz to 20 MHz
Phase Noise						
1 Hz offset		–	-74	-68	dBc/Hz	F_nom = 19.2 MHz TCXO and DCTCXO modes, and VCTCXO mode with ±6.25 ppm pull range
10 Hz offset		–	-102	-97	dBc/Hz	
100 Hz offset		–	-121	-117	dBc/Hz	
1 kHz offset		–	-142	-140	dBc/Hz	
10 kHz offset		–	-148	-146	dBc/Hz	
100 kHz offset		–	-149	-145	dBc/Hz	
1 MHz offset		–	-162	-158	dBc/Hz	
5 MHz offset		–	-164	-159	dBc/Hz	
Spurious	T_spur	–	-109	-104	dBc	F_nom = 19.2 MHz, 1 kHz to 5 MHz offsets

Table 6. Jitter & Phase Noise – LVCMOS, -40°C to 105°C

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Jitter						
RMS Phase Jitter (random)	T_phj	–	0.31	0.48	ps	F_nom = 10 MHz, Integration bandwidth = 12 kHz to 5 MHz
		–	0.31	0.50	ps	F_nom = 50 MHz, Integration bandwidth = 12 kHz to 20 MHz
RMS Period Jitter	T_jitt_per	–	0.8	1.1	ps	F_nom = 10 MHz, population 10 k
Peak Cycle-to-Cycle Jitter	T_jitt_cc	–	6	9	ps	F_nom = 10 MHz, population 1 k, measured as absolute value
Phase Noise						
1 Hz offset		–	-80	-74	dBc/Hz	F_nom = 10 MHz TCXO and DCTCXO modes, and VCTCXO mode with ±6.25 ppm pull range
10 Hz offset		–	-108	-102	dBc/Hz	
100 Hz offset		–	-127	-123	dBc/Hz	
1 kHz offset		–	-148	-145	dBc/Hz	
10 kHz offset		–	-154	-151	dBc/Hz	
100 kHz offset		–	-154	-150	dBc/Hz	
1 MHz offset		–	-167	-162	dBc/Hz	
5 MHz offset		–	-168	-163	dBc/Hz	
Spurious	T_spur	–	-112	-101	dBc	F_nom = 10 MHz, 1 kHz to 5 MHz offsets, Vdd = 2.5 V
		–	-112	-106	dBc	F_nom = 10 MHz, 1 kHz to 5 MHz offsets, Vdd = 2.8 V, 3.0 V, 3.3 V

Table 7. Jitter & Phase Noise – Clipped Sinewave, -40°C to 105°C

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Jitter						
RMS Phase Jitter (random)	T_phj	–	0.31	0.46	ps	F_nom = 19.2 MHz, Integration bandwidth = 12 kHz to 5 MHz
		–	0.31	0.50	ps	F_nom = 60 MHz, Integration bandwidth = 12 kHz to 20 MHz
Phase Noise						
1 Hz offset		–	-74	-68	dBc/Hz	F_nom = 19.2 MHz TCXO and DCTCXO modes, and VCTCXO mode with ±6.25 ppm pull range
10 Hz offset		–	-102	-97	dBc/Hz	
100 Hz offset		–	-121	-117	dBc/Hz	
1 kHz offset		–	-142	-140	dBc/Hz	
10 kHz offset		–	-148	-146	dBc/Hz	
100 kHz offset		–	-149	-145	dBc/Hz	
1 MHz offset		–	-162	-158	dBc/Hz	
5 MHz offset		–	-164	-159	dBc/Hz	
Spurious	T_spur	–	-109	-103	dBc	F_nom = 19.2 MHz, 1 kHz to 5 MHz offsets

Table 8. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Conditions	Value	Unit
Storage Temperature		-65 to 125	°C
Continuous Power Supply Voltage Range (Vdd)		-0.5 to 4	V
Human Body Model (HBM) ESD Protection	JESD22-A114	2000	V
Soldering Temperature (follow standard Pb-free soldering guidelines)		260	°C
Junction Temperature[5]		130	°C
Input Voltage, Maximum	Any input pin	Vdd + 0.3	V
Input Voltage, Minimum	Any input pin	-0.3	V

Note:
5. Exceeding this temperature for an extended period of time may damage the device.

Table 9. Thermal Considerations[6]

Package	θJA[7] (°C/W)	θJC, Bottom (°C/W)
Ceramic 5.0 mm x 3.2 mm	54	15

Note:
6. Measured in still air. Refer to JESD51 for θ_{JA} and θ_{JC} definitions.
7. Devices soldered on a JESD51 2s2p compliant board.

Table 10. Maximum Operating Junction Temperature[8]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	**80°C**
85°C	**95°C**
105°C	**115°C**

Note:
8. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 11. Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	**MIL-STD-883F, Method 2002**	**30000**	*g*
Mechanical Vibration Resistance	**MIL-STD-883F, Method 2007**	**70**	*g*
Temperature Cycle	**JESD22, Method A104**	–	–
Solderability	**MIL-STD-883F, Method 2003**	–	–
Moisture Sensitivity Level	**MSL1 @260°C**	–	–

Device Configurations and Pin-outs

Table 12. Device Configurations

Configuration	Pin 1	Pin 5	I²C Programmable Parameters
TCXO	OE/NC	NC	–
VCTCXO	VC	NC	–
DCTCXO	OE/NC	A0/NC	Frequency Pull Range, Frequency Pull Value, Output Enable control

Pin-out Top Views

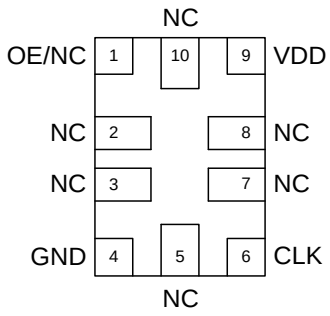


Figure 3. TCXO

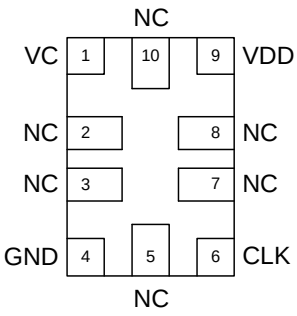


Figure 4. VCTCXO

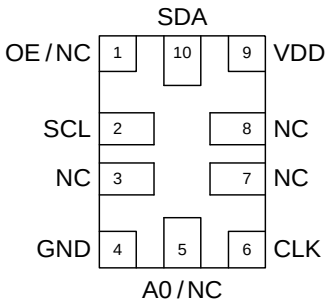


Figure 5. DCTCXO

Table 13. Pin Description

Pin	Symbol	I/O	Internal Pull-up/Pull Down Resistor	Function
1	OE/NC/VC	OE – Input	100 kΩ Pull-Up	H[9]: specified frequency output L: output is high impedance. Only output driver is disabled
		NC[11] – No Connect	–	H or L or Open: No effect on output frequency or other device functions
		VC – Input	–	Control Voltage in VCTCXO Mode
2	SCL / NC[11]	SCL – Input	200 kΩ Pull-Up	I²C serial clock input
		No Connect		H or L or Open: No effect on output frequency or other device functions
3	NC[11]	No Connect	–	H or L or Open: No effect on output frequency or other device functions
4	GND	Power	–	Connect to ground
5	A0 / NC[11]	A0 – Input	100 kΩ Pull-Up	Device I²C address when the address selection mode is via the A0 pin. This pin is NC when the I²C device address is specified in the ordering code. A0 Logic Level — I²C Address 0 — 1100010 1 — 1101010
		NC – No Connect	–	H or L or Open: No effect on output frequency or other device functions.
6	CLK	Output	–	LVCMOS, or clipped sinewave oscillator output
7	NC[11]	No Connect	–	H or L or Open: No effect on output frequency or other device functions
8	NC[11]	No Connect	–	H or L or Open: No effect on output frequency or other device functions
9	VDD	Power	–	Connect to power supply[1010]
10	SDA / NC[11]	SDA – Input/Output	200 kΩ Pull Up	I²C Serial Data
		NC – No Connect	–	H or L or Open: No effect on output frequency or other device functions

Notes:

9. In OE mode for noisy environments, a pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven. If pin 1 needs to be left floating, use the NC option.
10. A 0.1 µF capacitor in parallel with a 10 µF capacitor are required between VDD and GND. The 0.1 µF capacitor is recommended to place close to the device, and place the 10 µF capacitor less than 2 inches away.
11. All NC pins can be left floating and do not need to be soldered down.

Test Circuit Diagrams for LVCMOS and Clipped Sinewave Outputs

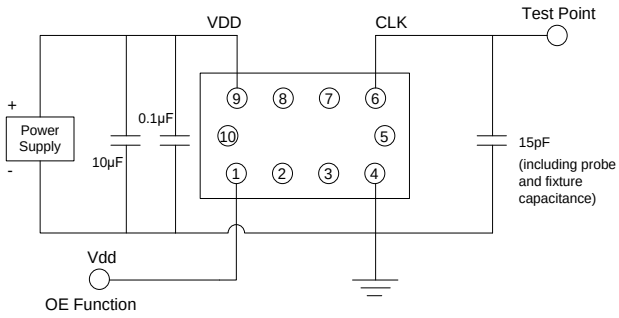


Figure 6. LVCMOS Test Circuit (OE Function)

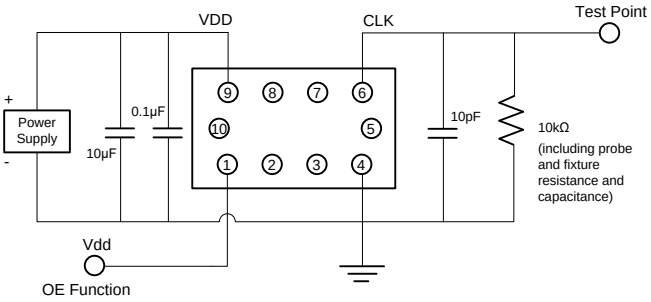


Figure 7. Clipped Sinewave Test Circuit (OE Function) for AC and DC Measurements

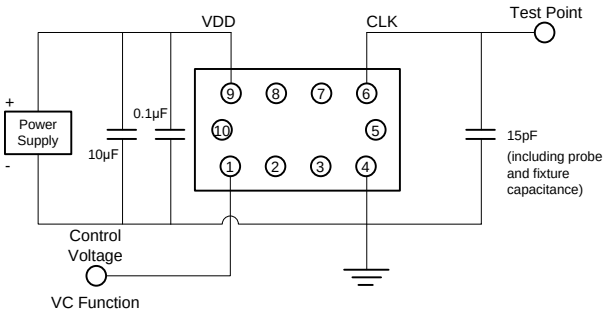


Figure 8. LVCMOS Test Circuit (VC Function)

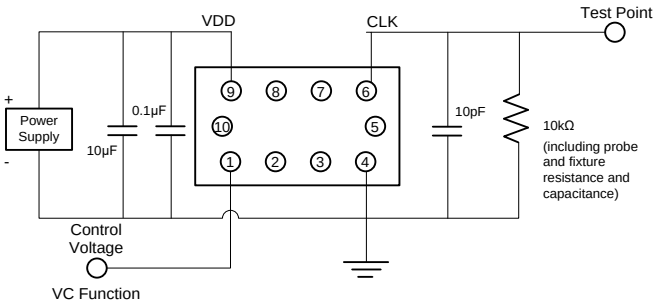


Figure 9. Clipped Sinewave Test Circuit (VC Function) for AC and DC Measurements

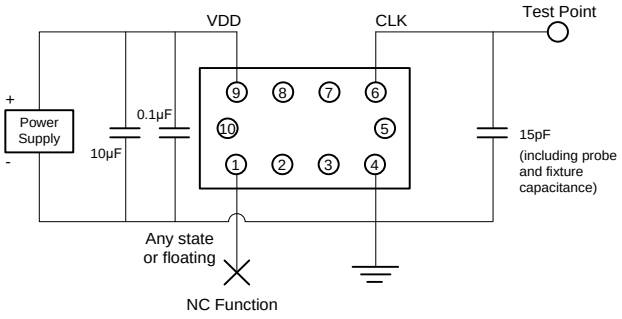


Figure 10. LVCMOS Test Circuit (NC Function)

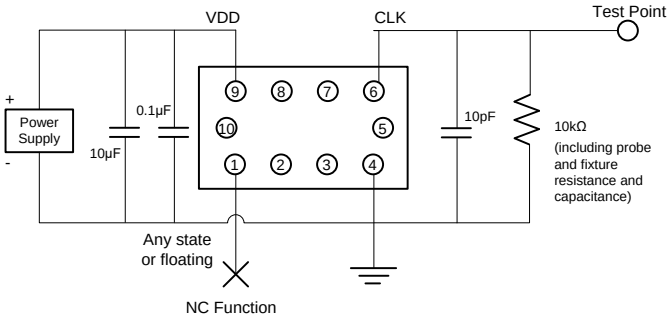


Figure 11. Clipped Sinewave Test Circuit (NC Function) for AC and DC Measurements

Test Circuit Diagrams for LVCMOS and Clipped Sinewave Outputs (continued)

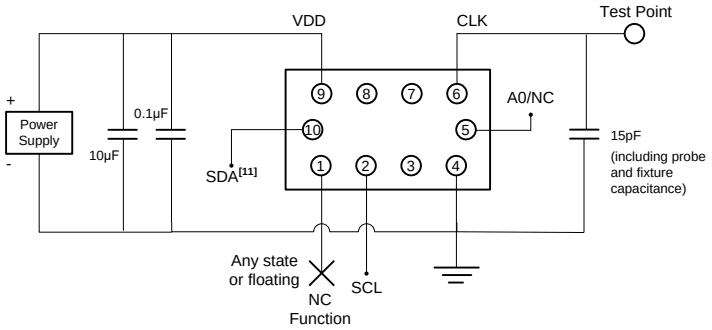


Figure 12. LVCMOS Test Circuit (I²C Control), DCTCXO mode for AC and DC Measurements

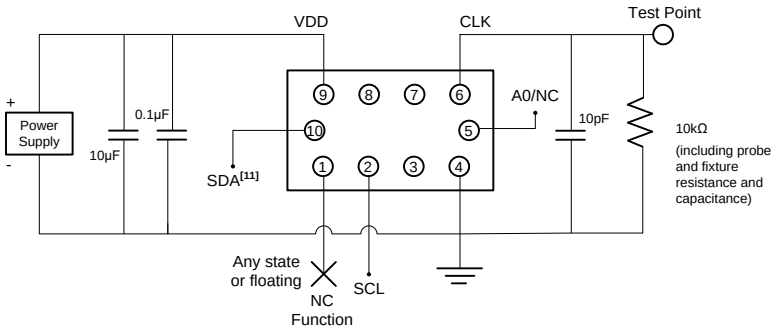


Figure 13. Clipped Sinewave Test Circuit (I²C Control), DCTCXO mode for AC and DC Measurements

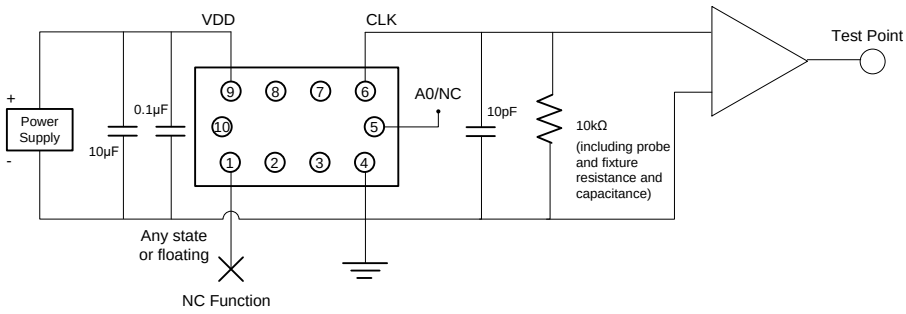


Figure 14. Clipped Sinewave Test Circuit for Phase Noise Measurements, Applies to All Configurations (NC Function shown for example only)

Note:
12. SDA is open-drain and may require pull-up resistor if not present in I²C test setup.

Waveforms

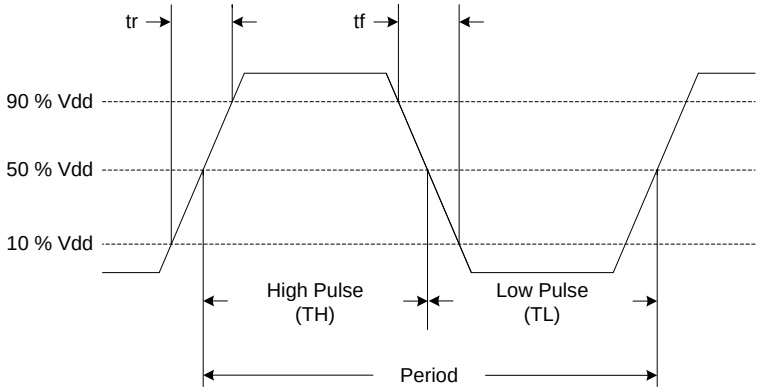


Figure 15. LVCMOS Waveform Diagram[13]

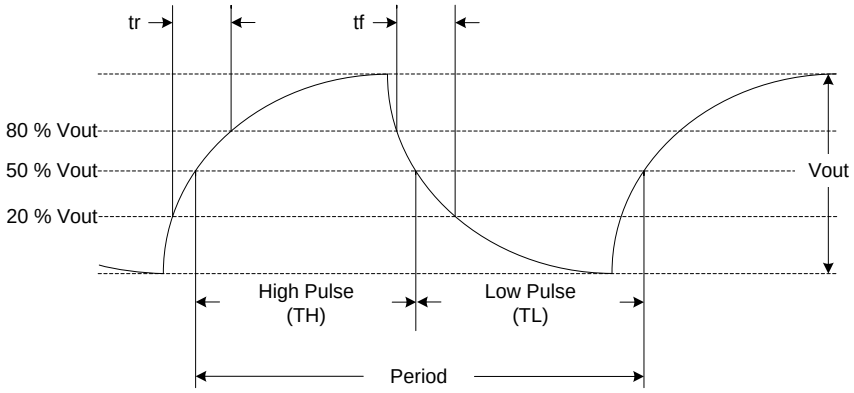
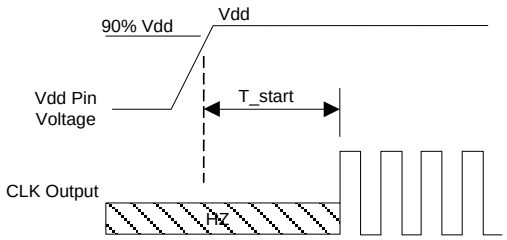


Figure 16. Clipped Sinewave Waveform Diagram[13]

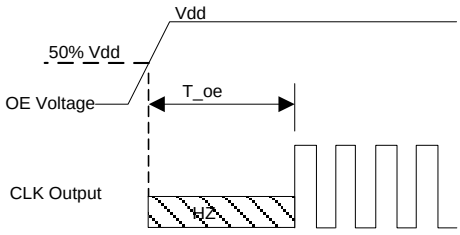
Note:
13. Duty Cycle is computed as Duty Cycle = TH/Period.

Timing Diagrams



T_start: Time to start from power-off

Figure 17. Startup Timing



T_oe: Time to re-enable the clock output

Figure 18. OE Enable Timing (OE Mode Only)

Stability Diagrams

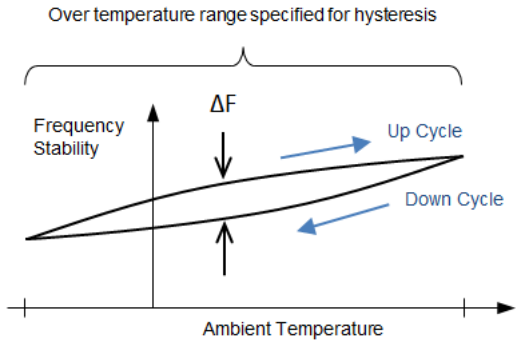


Figure 19. Illustration of hysteresis, where ΔF is max frequency difference between up and down cycles across temperature

Typical Performance Plots

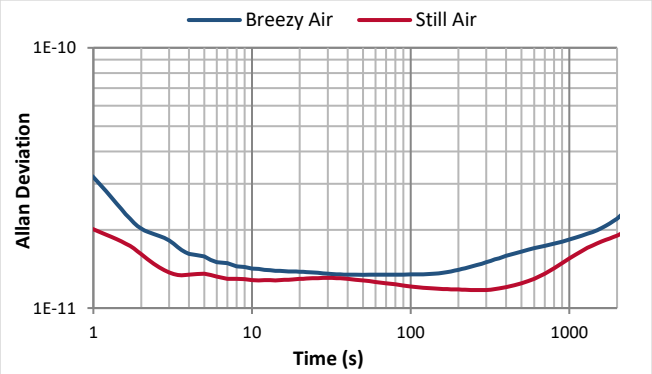


Figure 20. ADEV (±0.1 ppm) [14]

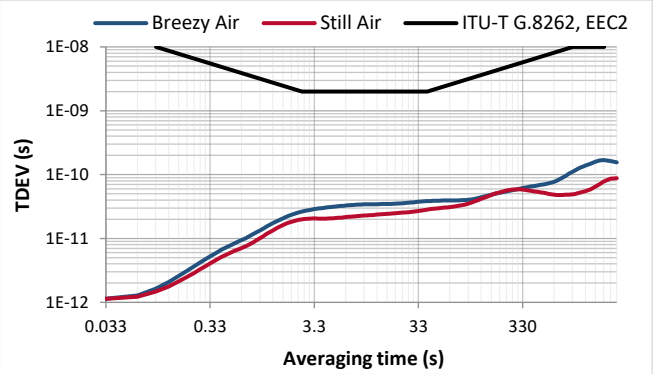


Figure 21. TDEV (0.1 Hz loop bandwidth, ±0.1 ppm) [14]

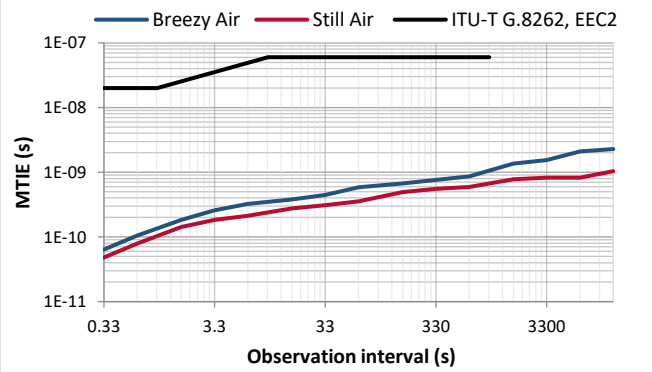


Figure 22. MTIE (0.1 Hz loop bandwidth, ±0.1 ppm) [14]

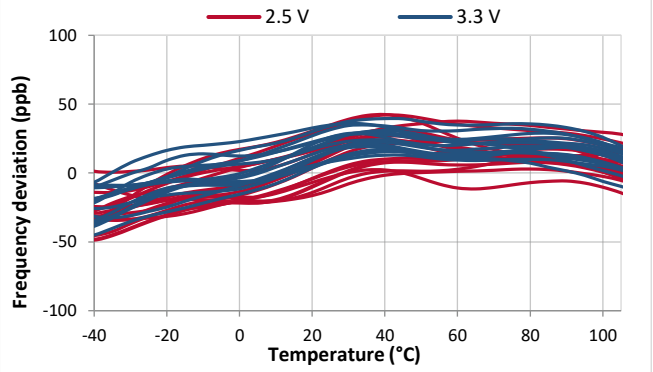


Figure 23. Frequency vs Temperature (±0.1 ppm), 105°C

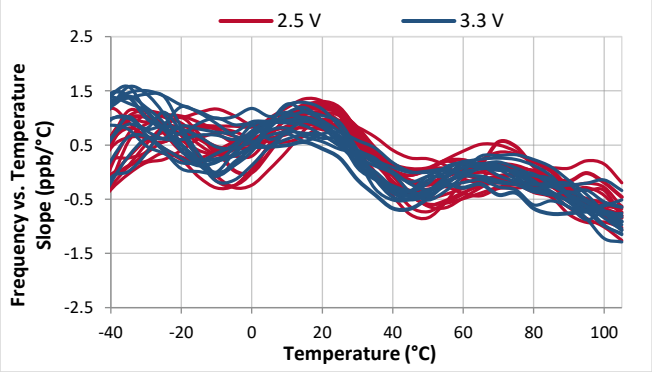


Figure 24. Freq. vs. Temp. Slope (ΔF/ΔT), ±0.1 ppm device

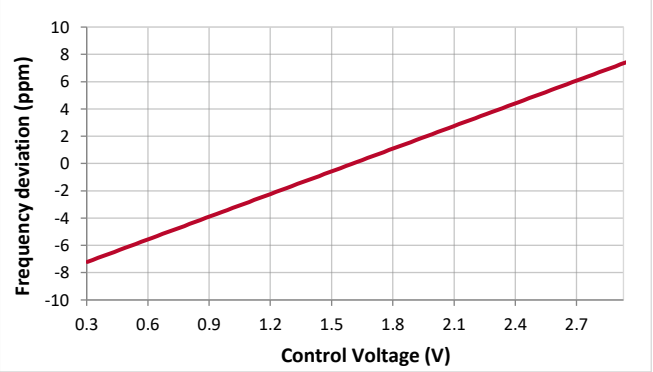


Figure 25. VCTCXO frequency pull characteristic

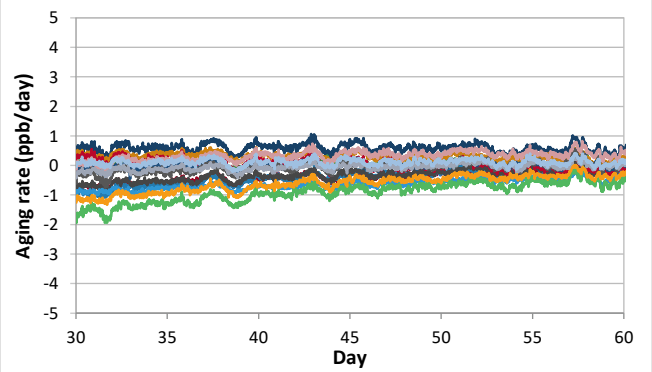


Figure 26. 1-day aging rate after 30 days, 0.1 ppm device

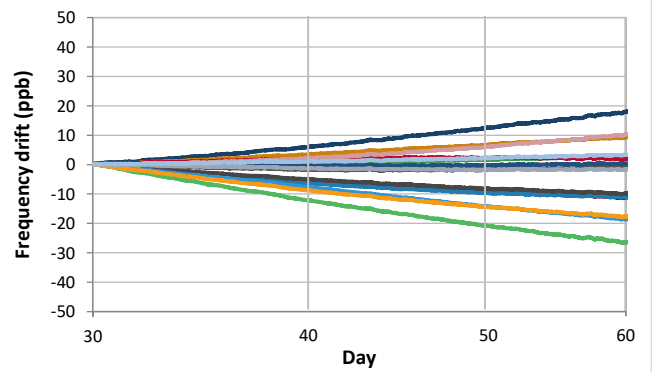


Figure 27. Frequency drift after 30 days [15]

Typical Performance Plots (continued)

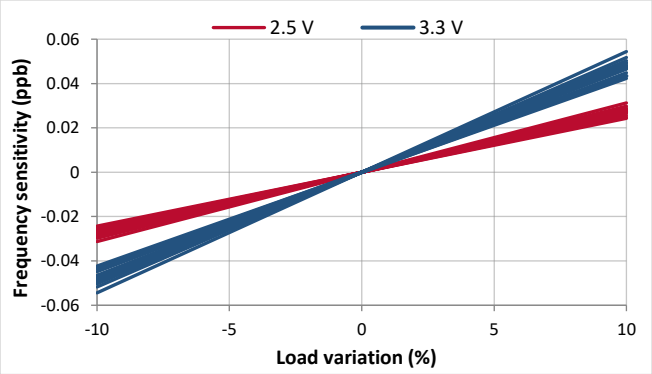


Figure 28. Load sensitivity (±0.1 ppm)

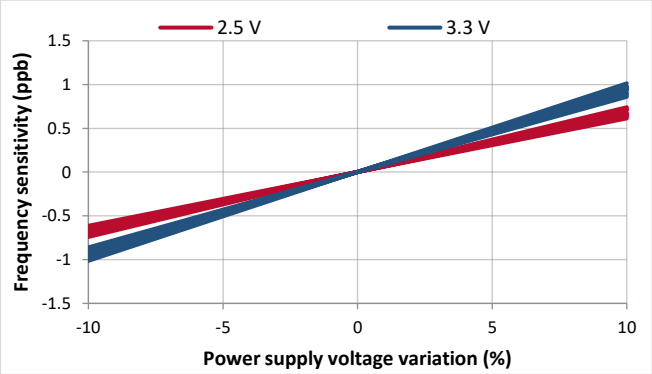


Figure 29. VDD sensitivity (±0.1 ppm)

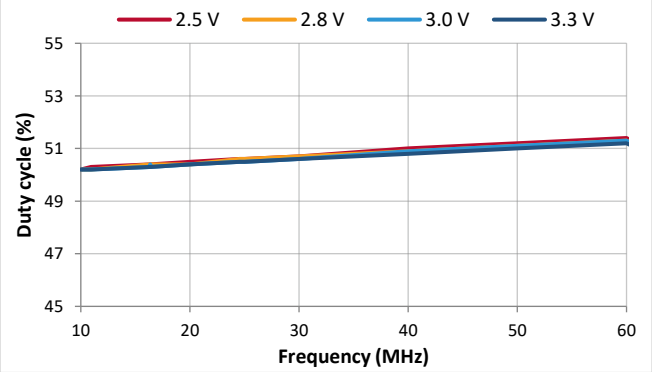


Figure 30. Duty Cycle (LVCMOS)

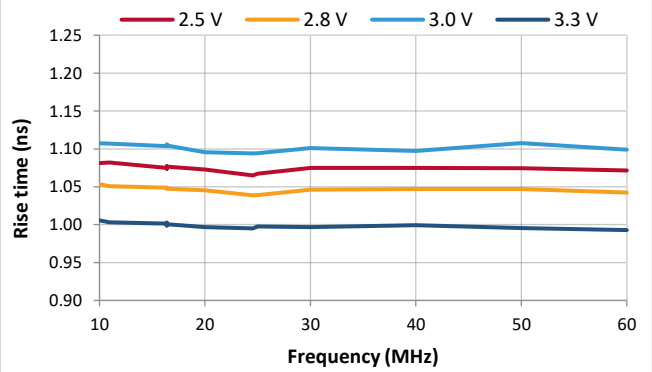


Figure 31. Rise Time (LVCMOS)

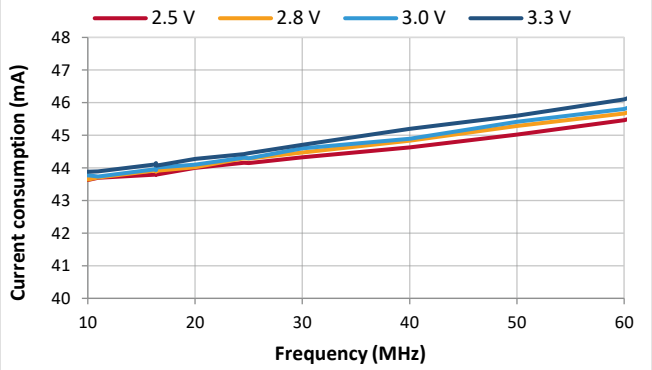


Figure 32. IDD TCXO (LVCMOS)

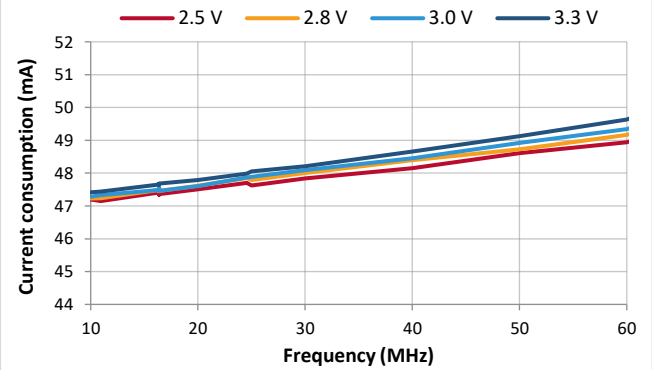


Figure 33. IDD VCTCXO (LVCMOS)

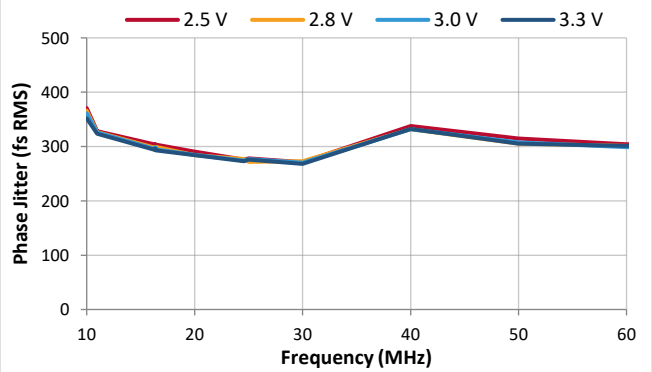


Figure 34. RMS Phase Jitter, DCTCXO, TCXO (LVCMOS)

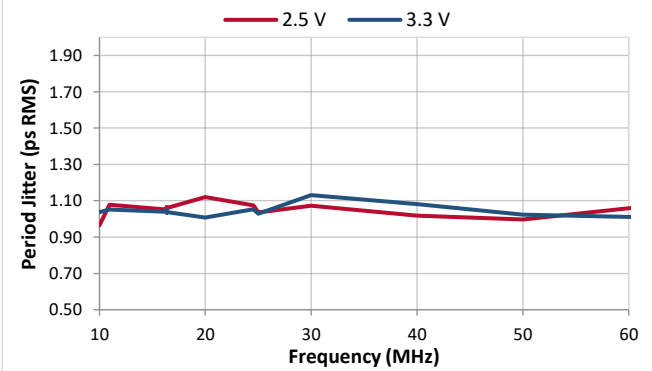


Figure 35. RMS Period Jitter (LVCMOS)

Typical Performance Plots (continued)

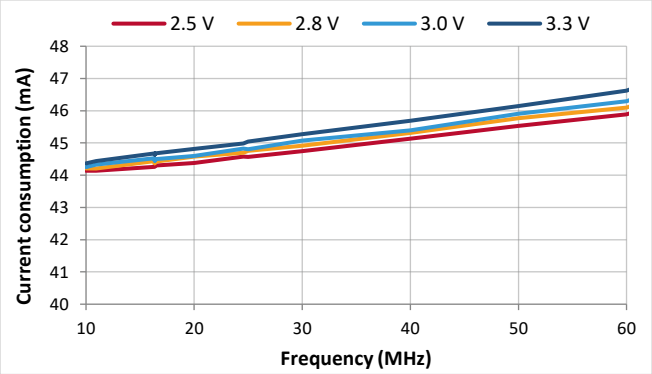


Figure 36. IDD DCTCXO (LVCMOS)

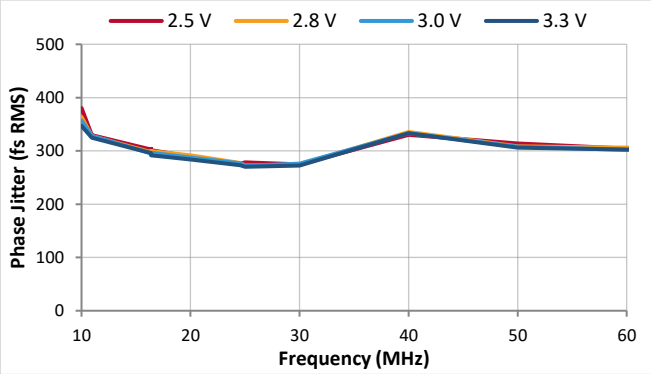


Figure 37. RMS Phase Jitter, VCTCXO (LVCMOS)

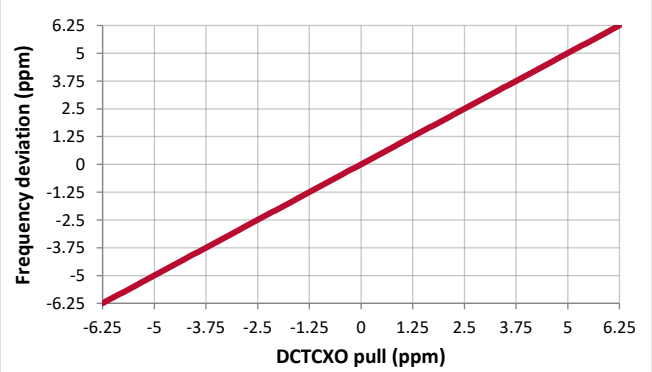


Figure 38. DCTCXO frequency pull characteristic

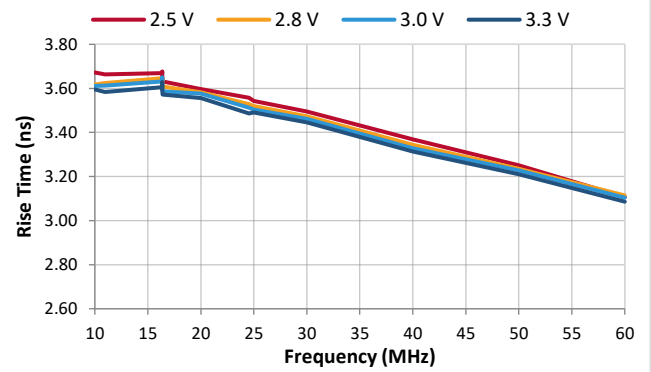


Figure 39. Rise Time (Clipped Sinewave)

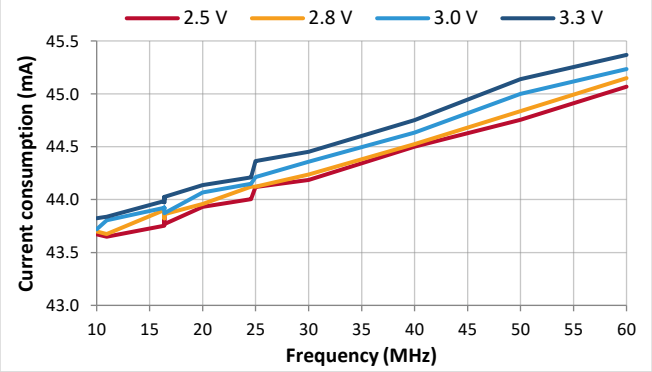


Figure 40. IDD TCXO (Clipped Sinewave)

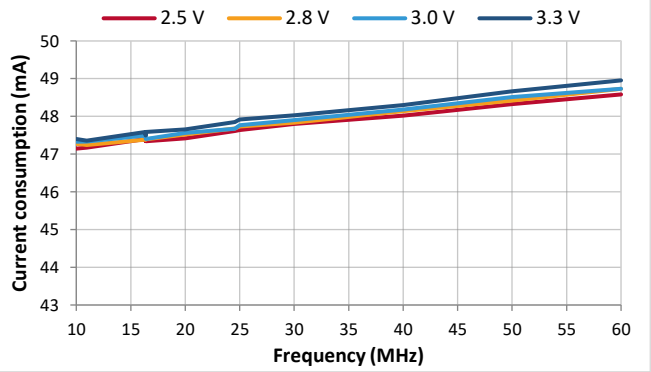


Figure 41. IDD VCTCXO (Clipped Sinewave)

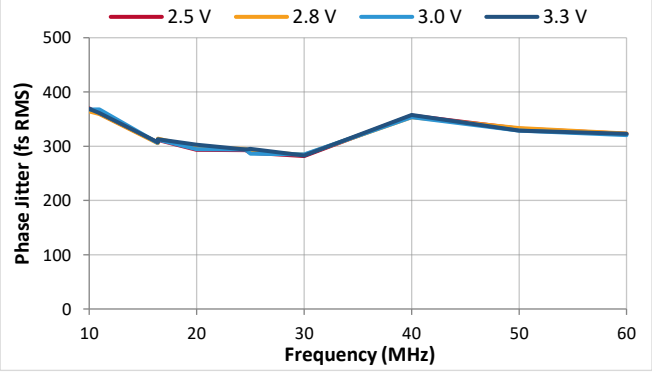


Figure 42. RMS Phase Jitter, DCTCXO, TCXO (Clip Sine)

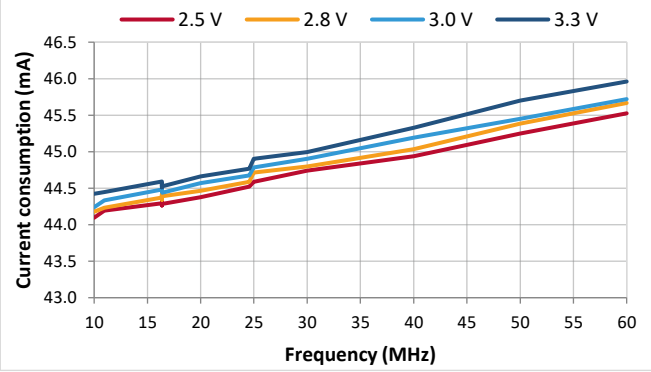


Figure 43. IDD DCTCXO (Clipped Sinewave)

Typical Performance Plots (continued)

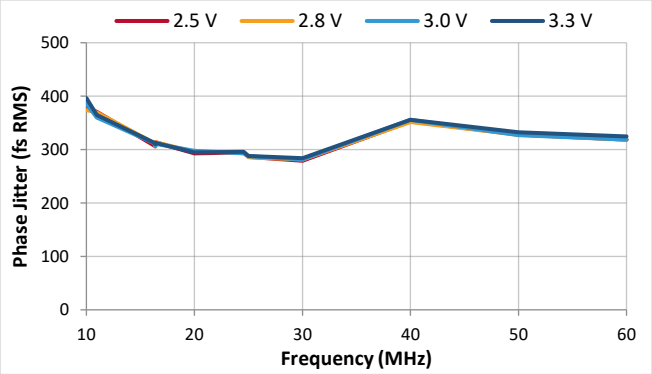


Figure 44. RMS Phase Jitter, VCTCXO (Clipped Sine)

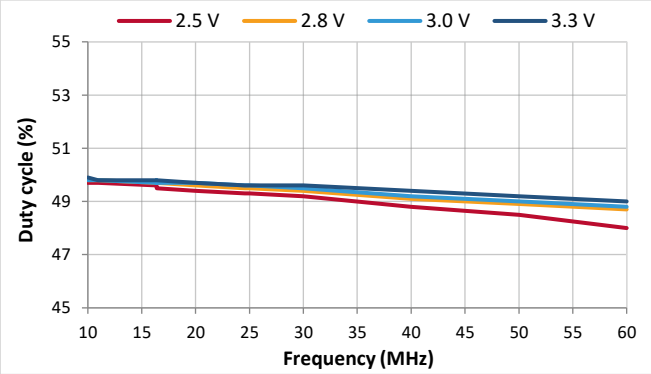


Figure 45. Duty Cycle (Clipped Sinewave)

Note:

14. Measured 24 hours after start up in a temperature chamber with constant temperature.
15. Plotted with respect to the frequency measurement at the end of the 30th day.

Architecture Overview

Based on SiTime's innovative Elite Platform®, the SiT5346 delivers exceptional dynamic performance, i.e. resilience to environmental stressors such as shock, vibration, and fast temperature transients. Underpinning the Elite Platform are SiTime's unique DualMEMS temperature sensing architecture and TurboCompensation™ technologies.

DualMEMS is a noiseless temperature compensation scheme. It consists of two MEMS resonators fabricated on the same die substrate. The TempFlat® MEMS resonator is designed with a flat frequency characteristic over temperature whereas the temperature sensing resonator is by design sensitive to temperature changes. The ratio of frequencies between these two resonators provides an accurate reading of the resonator temperature with 20 µK resolution.

By placing the two MEMS resonators (TempFlat MEMS® and temperature sensing resonator) on the same die, this temperature sensing scheme eliminates any thermal lag and gradients between resonator and temperature sensor, thereby overcoming an inherent weakness of legacy quartz TCXOs.

The DualMEMS temperature sensor drives a state-of-the-art CMOS temperature compensation circuit. The TurboCompensation design, with >100 Hz compensation bandwidth, achieves a dynamic frequency stability that is far superior to any quartz TCXO. The digital temperature compensation enables additional optimization of frequency stability and frequency slope over temperature within any chosen temperature range for a given system design.

The Elite Platform also incorporates a high resolution, low noise frequency synthesizer along with the industry standard I^2C bus. This unique combination enables system designers to digitally control the output frequency in steps as low as 5 ppt and over a wide range up to ±3200 ppm.

For more information regarding the Elite Platform and its benefits please visit:

- SiTime's breakthroughs section
- TechPaper: DualMEMS Temperature Sensing Technology
- TechPaper: DualMEMS Resonator TDC

Functional Overview

The SiT5346 is designed for maximum flexibility with an array of factory programmable options, enabling system designers to configure this precision device for optimal performance in a given application.

Frequency Stability

The SiT5346 comes in three factory-trimmed stability grades that are optimized for different applications. Both Stratum 3+ and Stratum 3 devices are compliant with Stratum 3 stability of ±4.6 ppm over 20 years.

Table 14. Stability Grades vs. Ordering Codes

Grade	Frequency Slope (ΔF/ΔT)	Frequency Stability Over Temperature	Ordering Code
Stratum 3+	±3.5 ppb/°C	±0.1 ppm	Q
Stratum 3	±10 ppb/°C	±0.2 ppm	P
		±0.25 ppm	N

- Stratum 3+ grade with ΔF/ΔT of ±3.5 ppb/°C is engineered to provide significantly better performance than legacy quartz TCXOs in time and phase synchronization applications such as IEEE1588, small cells, and 5G C-RAN (cloud RAN).
- Stratum 3 grade is designed to replace classic Stratum 3 TCXOs in applications such as SyncE with better dynamic performance and shorter lead time.

Output Frequency and Format

The SiT5346 can be factory programmed for an output frequency without sacrificing lead time or incurring an upfront customization cost typically associated with custom-frequency quartz TCXOs.

The device supports both LVCMOS and clipped sinewave output. Ordering codes for the output format are shown below:

Table 15. Output Formats vs. Ordering Codes

Output Format	Ordering Code
LVCMOS	"-"
Clipped Sinewave	"C"

Output Frequency Tuning

In addition to the non-pullable TCXO, the SiT5346 can also support output frequency tuning through either an analog control voltage (VCTCXO), or I^2C interface (DCTCXO). The I^2C interface enables 16 factory programmed pull-range options from ±6.25 ppm to ±3200 ppm. The pull range can also be reprogrammed via I^2C to any supported pull-range value.

Refer to Device Configuration section for details.

Pin 1 Configuration (OE, VC, or NC)

Pin 1 of the SiT5346 can be factory programmed to support three modes: Output Enable (OE), Voltage Control (VC), or No Connect (NC).

Table 16. Pin Configuration Options

Pin 1 Configuration	Operating Mode	Output
OE	TCXO/DCTCXO	Active or High-Z
NC	TCXO/DCTCXO	Active
VC	VCTCXO	Active

When pin 1 is configured as OE pin, the device output is guaranteed to operate in one of the following two states:

- Clock output with the frequency specified in the part number when Pin 1 is pulled to logic high
- Hi-Z mode with weak pull down when pin 1 is pulled to logic low.

When pin 1 is configured as NC, the device is guaranteed to output the frequency specified in the part number at all times, regardless of the logic level on pin 1.

In the VCTCXO configuration, the user can fine-tune the output frequency from the nominal frequency specified in the part number by varying the pin 1 voltage. The guaranteed allowable variation of the output frequency is specified as pull range. A VCTCXO part number must contain a valid pull-range ordering code.

Device Configurations

The SiT5346 supports 3 device configurations – TCXO, VCTCXO, and DCTCXO. The TCXO and VCTCXO options are directly compatible with the quartz TCXO and VCTCXO. The DCTCXO configuration provides performance enhancement by eliminating VCTCXO's sensitivity to control voltage noise with an I^2C digital interface for frequency tuning.

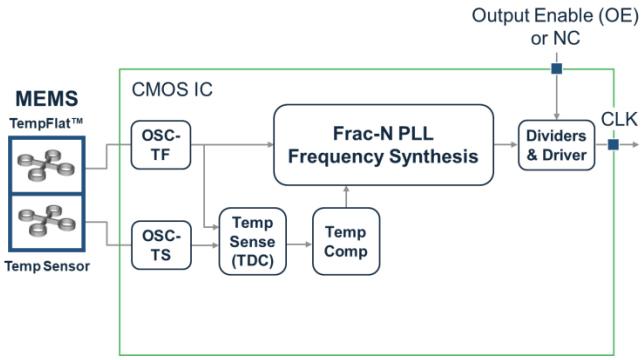


Figure 46. Block Diagram – TCXO

TCXO Configuration

The TCXO generates a fixed frequency output, as shown in Figure 46. The frequency is specified by the user in the frequency field of the device ordering code and then factory programmed. Other factory programmable options include supply voltage, output types (LVCMOS or clipped sinewave), and pin 1 functionality (OE or NC).

Refer to the Ordering Information section at the end of the datasheet for a list of all ordering options.

VCTCXO Configuration

A VCTCXO, shown in Figure 47, is a frequency control device whose output frequency is an approximately linear function of control voltage applied to the voltage control pin. VCTCXOs have a number of use cases including the VCO portion of a jitter attenuation/jitter cleaner PLL Loop.

The SiT5346 achieves a 10x better pull range linearity of <0.5% via a high-resolution fractional PLL and low-noise precision analog-to-digital converter. By contrast, quartz-based VCTCXOs change output frequency by varying the capacitive load of a crystal resonator using varactor diodes, which results in linearity of 5% to 105%.

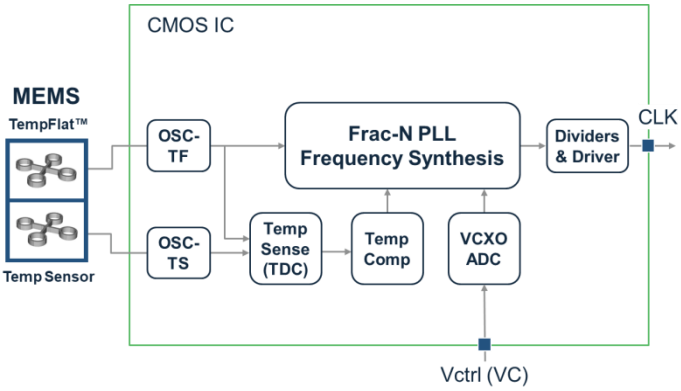


Figure 47. Block Diagram – VCTCXO

Note that the output frequency of the VCTCXO is proportional to the analog control voltage applied to pin 1. Because this control signal is analog and directly controls the output frequency, care must be taken to minimize noise on this pin.

The nominal output frequency is factory programmed per the customer's request to 6 digits of precision and is defined as the output frequency when the control voltage equals Vdd/2. The maximum output frequency variation from this nominal value is set by the pull range, which is also factory programmed to the customer's desired value and specified by the ordering code. The Ordering Information section shows all ordering options and associated ordering codes.

Refer to VCTCXO-Specific Design Considerations for more information on critical VCTCXO parameters including pull range linearity, absolute pull range, control voltage bandwidth, and K_V.

DCTCXO Configuration

The SiT5346 offers digital control of the output frequency, as shown in Figure 48. The output frequency is controlled by writing frequency control words over the I²C interface.

There are several advantages of DCTCXOs relative to VCTCXOs:

1) Frequency control resolution as low as 5 ppt. This high resolution minimizes accumulated time error in synchronization applications.
2) Lower system cost – A VCTCXO may need a Digital to Analog Converter (DAC) to drive the control voltage input. In a DCTCXO, the frequency control is achieved digitally by register writes to the control registers via I²C, thereby eliminating the need for a DAC.
3) Better noise immunity – The analog signal used to drive the voltage control pin of a VCTCXO can be sensitive to noise, and the trace over which the signal is routed can be susceptible to noise coupling from the system. The DCTCXO does not suffer from analog noise coupling since the frequency control is performed digitally through I²C.
4) No frequency-pull non-linearity – The frequency pulling is achieved via fractional feedback divider of the PLL, eliminating any pull non-linearity concerns typical of quartz-based VCTCXOs. This improves dynamic performance in closed-loop applications.
5) Programmable wide pull range – The DCTCXO pulling mechanism is via the fractional feedback divider and is therefore not constrained by resonator pullability as in quartz-based solutions. The SiT5346 offers 16 frequency pull-range options from ±6.25 ppm to ±3200 ppm, providing system designers great flexibility.

Refer to DCTCXO-Specific Design Considerations for more information on critical DCTCXO parameters including pull range, absolute pull range, frequency output, and I²C control registers.

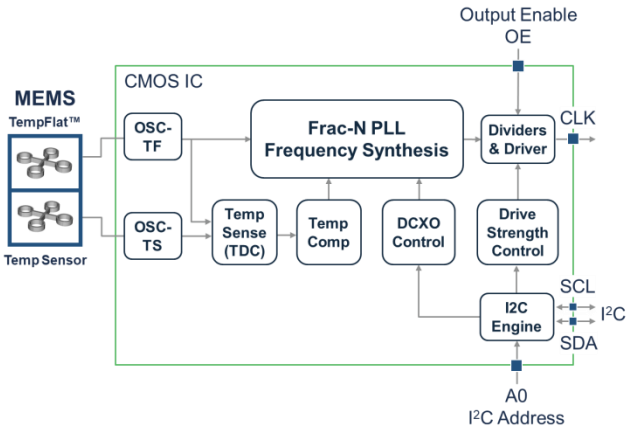


Figure 48. Block Diagram

VCTCXO-Specific Design Considerations

Linearity

In any VCTCXO, there will be some deviation of the frequency-voltage (FV) characteristic from an ideal straight line. Linearity is the ratio of this maximum deviation to the total pull range, expressed as a percentage. Figure 49 below shows the typical pull linearity of a SiTime VCTCXO. The linearity is excellent (1% maximum) relative to most quartz offerings because the frequency pulling is achieved with a PLL rather than varactor diodes.

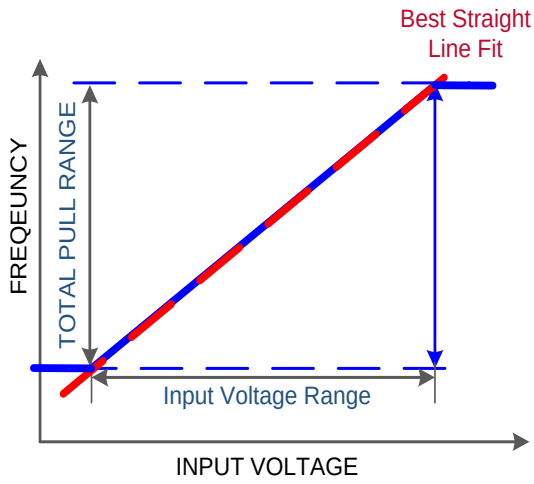


Figure 49. Typical SiTime VCTCXO Linearity

Control Voltage Bandwidth

Control voltage bandwidth, sometimes called “modulation rate” or “modulation bandwidth”, indicates how fast a VCO can respond to voltage changes at its input. The ratio of the output frequency variation to the input voltage variation, previously denoted by K_V, has a low-pass characteristic in most VCTCXOs. The control voltage bandwidth equals the modulating frequency where the output frequency deviation equals 0.707 (e.g. -3 dB) of its DC value, for DC inputs swept in the same voltage range.

For example, a part with a ±6.25 ppm pull range and a 0-3V control voltage can be regarded as having an average KV of 4.17 ppm/V (12.5 ppm/3V = 4.17 ppm/V). Applying an input of 1.5 V DC ± 0.5 V (1.0 V to 2.0 V) causes an output frequency change of 4.17 ppm (±2.08 ppm). If the control voltage bandwidth is specified as 10 kHz, the peak-to-peak value of the output frequency change will be reduced to 4.33 ppm/√2 or 2.95 ppm, as the frequency of the control voltage change is increased to 10 kHz.

FV Characteristic Slope K_V

The slope of the FV characteristic is a critical design parameter in many low bandwidth PLL applications. The slope is the derivative of the FV characteristic – the deviation of frequency divided by the control voltage change needed to produce that frequency deviation, over a small voltage span, as shown below:

$$K_V = \frac{\Delta f_{out}}{\Delta V_{in}}$$

It is typically expressed in kHz/Volt, MHz/Volt, ppm/Volt, or similar units. This slope is usually called “K_V” based on terminology used in PLL designs.

The extreme linear characteristic of the SiTime SiT5346 VCTCXO family means that there is very little K_V variation across the whole input voltage range (typically <1%), significantly reducing the design burden on the PLL designer. Figure 50 below illustrates the typical K_V variation.

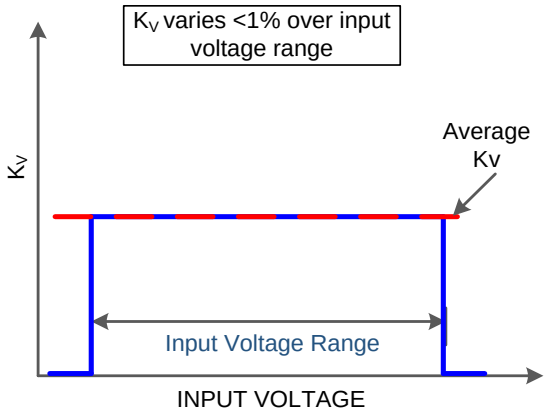


Figure 50. Typical SiTime K_V Variation

Pull Range, Absolute Pull Range

Pull range (PR) is the amount of frequency deviation that will result from changing the control voltage over its maximum range under nominal conditions.

Absolute pull range (APR) is the guaranteed controllable frequency range over all environmental and aging conditions. Effectively, it is the amount of pull range remaining after taking into account frequency stability, tolerances over variables such as temperature, power supply voltage, and aging, i.e.:

$$APR = PR - F_{stability} - F_{aging}$$

where $F_{stability}$ is the device frequency stability due to initial tolerance and variations on temperature, power supply, and load.

Figure 51 shows a typical SiTime VCTCXO FV characteristic. The FV characteristic varies with conditions, so that the frequency output at a given input voltage can vary by as much as the specified frequency stability of the VCTCXO. For such VCTCXOs, the frequency stability and APR are independent of each other. This allows very wide range of pull options without compromising frequency stability.

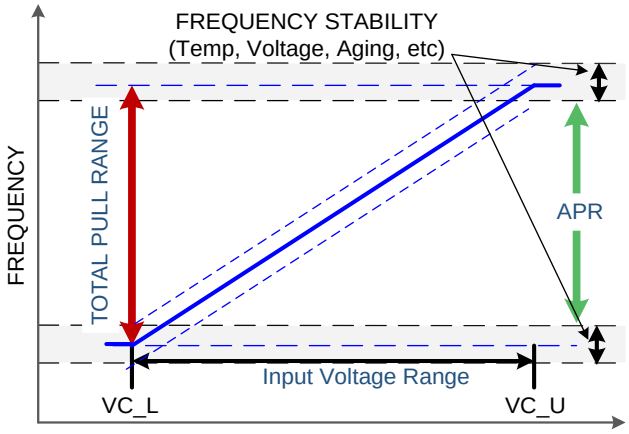


Figure 51. Typical SiTime VCTCXO FV Characteristic

The upper and lower control voltages are the specified limits of the input voltage range as shown in Figure 51 above. Applying voltages beyond the upper and lower voltages do not result in noticeable changes of output frequency. In other words, the FV characteristic of the VCTCXO saturates beyond these voltages. Figures 1 and 2 show these voltages as Lower Control Voltage (VC_L) and Upper Control Voltage (VC_U).

Table 17 below shows the pull range and corresponding APR values for each of the frequency vs. temperature ordering options.

Table 17. VCTCXO Pull Range, APR Options[16] Typical unless specified otherwise. Pull range (PR) is ±6.25 ppm.

Pull Range Ordering Code	Device Option(s)	APR ppm ±0.1 ppm option ±0.54 ppm 20-year aging	APR ppm ±0.2 ppm option ±2 ppm 20-year aging	APR ppm ±0.25 ppm option ±2 ppm 20-year aging
T	VCTCXO	±5.31	±3.05	±3.00

Notes:
16. APR includes initial tolerance, frequency stability vs. temperature, and the indicated 20-year aging.

DCTCXO-Specific Design Considerations

Pull Range and Absolute Pull Range

Pull range and absolute pull range are described in the previous section. Table 18 below shows the pull range and corresponding APR values for each of the frequency vs. temperature ordering options.

Table 18. APR Options[17]

Pull Range Ordering Code	Pull Range ppm	APR ppm ±0.1 ppm option ±0.54 ppm 20-year aging	APR ppm ±0.2 ppm option ±2 ppm 20-year aging	APR ppm ±0.25 ppm option ±2 ppm 20-year aging
T	±6.25	±5.31	±3.05	±3.00
R	±10	±9.06	±6.80	±6.75
Q	±12.5	±11.56	±9.3	±9.25
M	±25	±24.06	±21.8	±21.75
B	±50	±49. 06	±46.8	±46.75
C	±80	±79. 06	±76.8	±76.75
E	±100	±99. 06	±96.8	±96.75
F	±125	±124. 06	±121.8	±121.75
G	±150	±149. 06	±146.8	±146.75
H	±200	±199. 06	±196.8	±196.75
X	±400	±399. 06	±396.8	±396.75
L	±600	±599. 06	±596.8	±596.75
Y	±800	±799. 06	±796.8	±796.75
S	±1200	±1199. 06	±1196.8	±1196.75
Z	±1600	±1599. 06	±1596.8	±1596.75
U	±3200	±3199. 06	±3196.8	±3196.75

Notes:
17. APR includes initial tolerance, frequency stability vs. temperature, and the indicated 20-year aging.

Output Frequency

The device powers up at the nominal operating frequency and pull range specified by the ordering code. After power-up both pull range and output frequency can be controlled via I^2C writes to the respective control registers. The maximum output frequency change is constrained by the pull range limits.

The pull range is specified by the value loaded in the digital pull-range control register. The 16 pull range choices are specified in the control register and range from ±6.25 ppm to ±3200 ppm.

Table 19 below shows the frequency resolution versus pull range programmed value

Table 19. Frequency Resolution versus Pull Range

Programmed Pull Range	Frequency Resolution
±6.25 ppm	$5x10^{-12}$
±10 ppm	$5x10^{-12}$
±12.5 ppm	$5x10^{-12}$
±25 ppm	$5x10^{-12}$
±50 ppm	$5x10^{-12}$
±80 ppm	$5x10^{-12}$
±100 ppm	$5x10^{-12}$
±120 ppm	$5x10^{-12}$
±150 ppm	$5x10^{-12}$
±200 ppm	$5x10^{-12}$
±400 ppm	$1x10^{-11}$
±600 ppm	$1.4x10^{-11}$
±800 ppm	$2.1x10^{-11}$
±1200 ppm	$3.2x10^{-11}$
±1600 ppm	$4.7x10^{-11}$
±3200 ppm	$9.4x10^{-11}$

The ppm frequency offset is specified by the 26 bit DCXO frequency control register in two's complement format as described in the I^2C Register Descriptions. The power up default value is 00000000000000000000000000b which sets the output frequency at its nominal value (0 ppm). To change the output frequency, a frequency control word is written to 0x00[15:0] (Least Significant Word) and 0x01[9:0] (Most Significant Word). The LSW value should be written first followed by the MSW value; the frequency change is initiated after the MSW value is written.

Bits	25:24	23:20	19:16	15:12	11:8	7:4	3:0
Value (Hex)	01	1111	1111	1111	1111	1111	1111
Dec. Value	2^{25} -1 = 33,554,431						

Bits	25:24	23:20	19:16	15:12	11:8	7:4	3:0
Value (Hex)	00	0000	0000	0000	0000	0000	0000
Dec. Value	0						

Bits	25:24	23:20	19:16	15:12	11:8	7:4	3:0
Value (Hex)	10	0000	0000	0000	0000	0000	0000
Dec. Value	-(2^{25}) = -33,554,432						

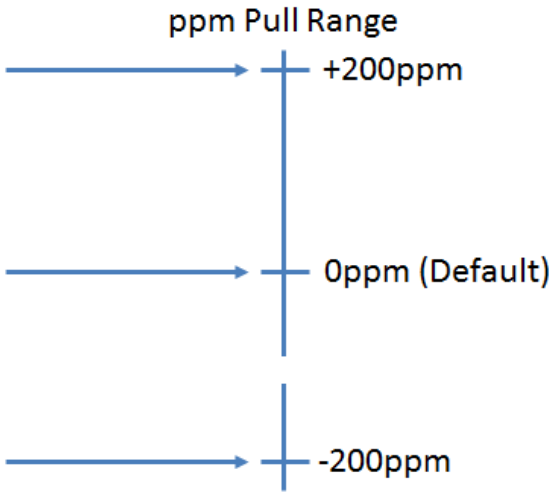


Figure 52. Pull Range and Frequency Control Word

Figure 52 shows how the two's complement signed value of the frequency control word sets the output frequency within the ppm pull range set by 0x02:[3:0]. This example shows use of the ±200 ppm pull range. Therefore, to set the desired output frequency, one just needs to calculate the fraction of full scale value ppm, convert to two's complement binary, and then write these values to the frequency control registers.

The following formula generates the control word value:

Control word value = RND((2^{25}-1) × ppm shift from nominal/pull range), where RND is the rounding function which rounds the number to the nearest whole number. Two examples follow, assuming a ±200 ppm pull range:

Example 1:

- Default Output Frequency = 19.2 MHz
- Desired Output Frequency = 19.201728 MHz (+90 ppm)

2^{25}-1 corresponds to +200 ppm, and the fractional value required for +90 ppm can be calculated as follows.

- 90 ppm / 200 ppm × (2^{25}-1) = 15,099,493.95.

Rounding to the nearest whole number yields 15,099,494 and converting to two's complement gives a binary value of 111001100110011001100110, or E66666 in hex.

Example 2:

- Default Output Frequency = 10 MHz
- Desired Output Frequency = 9.9995 MHz (-50 ppm)

Following the formula shown above,

- (-50 ppm / 200 ppm) × (2^{25}) = -8,388,608.

Converting this to two's complement binary results in 111000000000000000000000000, or 3800000 in hex.

To summarize, the procedure for calculating the frequency control word associated with a given ppm offset is as follows:

1) Calculate the fraction of the half-pull range needed. For example, if the total pull range is set for ±100 ppm and a +20 ppm shift from the nominal frequency is needed, this fraction is 20 ppm/100 ppm = 0.2
2) Multiply this fraction by the full-half scale word value, 2^{25}-1 = 33,554,431, round to the nearest whole number, and convert the result to two's complement binary. Following the +20 ppm example, this value is 0.2 × 33,554,431 = 6,710,886.2 and rounded to 6,710,886.
3) Write the two's complement binary value starting with the Least Significant Word (LSW) 0x00[16:0], followed by the Most Significant Word (MSW), 0x01[9:0]. If the user desires that the output remains enabled while changing the frequency, a 1 must also be written to the OE control bit 0x01[10] if the device has software OE Control Enabled.

It is important to note that the maximum Digital Control update rate is 38 kHz regardless of I^2C bus speed.

I²C Control Registers

The SiT5346 enables control of frequency pull range, frequency pull value, and Output Enable via I²C writes to the control registers. Table 20 below shows the register map summary, and detailed register descriptions follow.

Table 20. Register Map Summary

Address	Bits	Access	Description
0x00	[15:0]	RW	DIGITAL FREQUENCY CONTROL LEAST SIGNIFICANT WORD (LSW)
0x01	[15:11]	R	NOT USED
	[10]	RW	OE Control. This bit is only active if the output enable function is under software control. If the device is configured for hardware control using the OE pin, writing to this bit has no effect.
	[9:0]	RW	DIGITAL FREQUENCY CONTROL MOST SIGNIFICANT WORD (MSW)
0x02	[15:4]	R	NOT USED
	[3:0]	RW	DIGITAL PULL RANGE CONTROL

Register Descriptions

Register Address: 0x00. Digital Frequency Control Least Significant Word (LSW)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	DIGITAL FREQUENCY CONTROL LEAST SIGNIFICANT WORD (LSW)[15:0]															

Bits	Name	Access	Description
15:0	DIGITAL FREQUENCY CONTROL LEAST SIGNIFICANT WORD	RW	Bits [15:0] are the lower 16 bits of the 26 bit FrequencyControlWord and are the Least Significant Word (LSW). The upper 10 bits are in regsiter 0x01[9:0] and are the Most Significant Word (MSW). The lower 16 bits together with the upper 10 bits specify a 26-bit frequency control word. This power-up default values of all 26 bits are 0 which sets the output frequency at its nominal value. After power-up, the system can write to these two registers to pull the frequency across the pull range. The register values are two's complement to support positive and negative control values. The LSW value should be written before the MSW value because the frequency change is initiated when the new values are loaded into the MSW. More details and examples are discussed in the previous section.

Register Address: 0x01. OE Control, Digital Frequency Control Most Significant Word (MSW)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	NOT USED					OE	DCXO FREQUENCY CONTROL[9:0] MSW									

Bits	Name	Access	Description
15:11	NOT USED	R	Bits [15:10] are read only and return all 0's when read. Writing to these bits has no effect.
10	OE Control	RW	Output Enable Software Control. Allows the user to enable and disable the output driver via I^2C. 0 = Output Disabled (Default) 1 = Output Enabled This bit is only active if the Output Enable function is under software control. If the device is configured for hardware control using the OE pin, writing to this bit has no effect.
9:0	DIGITAL FREQUENCY CONTROL MOST SIGNIFICANT WORD (MSW)	RW	Bits [9:0] are the upper 10 bits of the 26 bit FrequencyControlWord and are the Most Significant Word (MSW). The lower 16 bits are in register 0x00[15:0] and are the Least Significant Word (LSW). These lower 16 bits together with the upper 10 bits specify a 26-bit frequency control word. This power-up default values of all 26 bits are 0 which sets the output frequency at its nominal value. After power-up, the system can write to these two registers to pull the frequency across the pull range. The register values are two's complement to support positive and negative control values. The LSW value should be written before the MSW value because the frequency change is initiated when the new values are loaded into the MSW. More details and examples are discussed in the previous section.

Register Address: 0x02. DIGITAL PULL RANGE CONTROL[18]

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X
Name	NONE												DIGITAL PULL RANGE CONTROL			

Notes:
18. Default values are factory set but can be over-written after power-up.

Bits	Name	Access	Description
15:4	NONE	R	Bits [15:4] are read only and return all 0's when read. Writing to these bits has no effect.
3:0	DIGITAL PULL RANGE CONTROL	RW	Sets the digital pull range of the DCXO. The table below shows the available pull range values and associated bit settings. The default value is factory programmed. **Bit** **3 2 1 0** 0 0 0 0: ±6.25 ppm 0 0 0 1: ±10 ppm 0 0 1 0: ±12.5 ppm 0 0 1 1: ±25 ppm 0 1 0 0: ±50 ppm 0 1 0 1: ±80 ppm 0 1 1 0: ±100 ppm 0 1 1 1: ±125 ppm 1 0 0 0: ±150 ppm 1 0 0 1: ±200 ppm 1 0 1 0: ±400 ppm 1 0 1 1: ±600 ppm 1 1 0 0: ±800 ppm 1 1 0 1: ±1200 ppm 1 1 1 0: ±1600 ppm 1 1 1 1: ±3200 ppm

Serial Interface Configuration Description

The SiT5346 includes an I²C interface to access registers that control the DCTCXO frequency pull range, and frequency pull value. The SiT5346 I²C slave-only interface supports clock speeds up to 1 Mbit/s. The SiT5346 I²C module is based on the I²C specification, UM1024 (Rev.6 April 4, 2014 of NXP Semiconductor).

Serial Signal Format

The SDA line must be stable during the high period of the SCL. SDA transitions are allowed only during SCL low level for data communication. Only one transition is allowed during the low SCL state to communicate one bit of data. Figure 53 shows the detailed timing diagram.

An idle I²C bus state occurs when both SCL and SDA are not being driven by any master and are therefore in a logic HI state due to the pull up resistors. Every transaction begins with a START (S) signal and ends with a STOP (P) signal. A START condition is defined by a high to low transition on the SDA while SCL is high. A STOP condition is defined by a low to high transition on the SDA while SCL is high. START and STOP conditions are always generated by the master. This slave module also supports repeated START (Sr) condition which is same as START condition instead of STOP condition (the blue-color line shows repeated START in Figure 54).

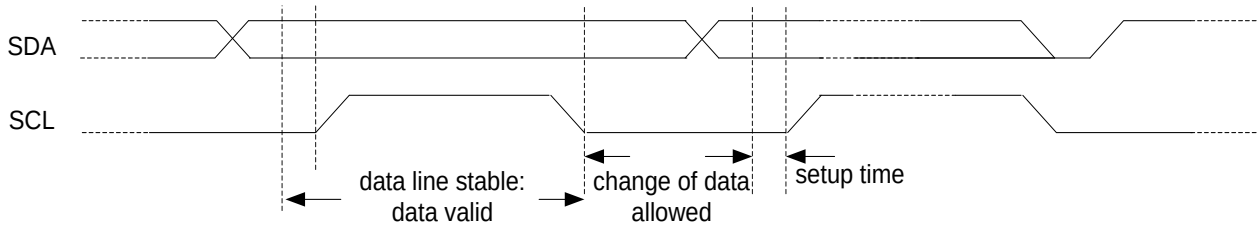


Figure 53. Data and clock timing relation in I²C bus

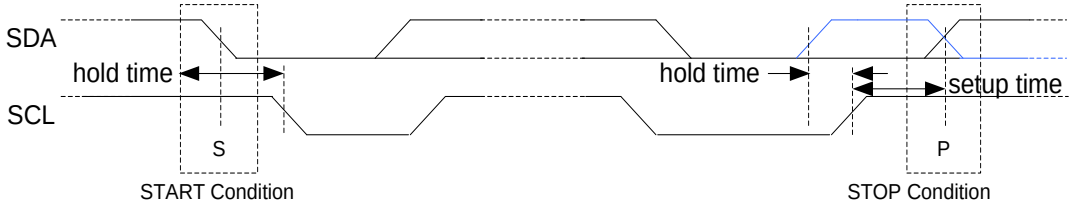


Figure 54. START and STOP (or repeated START, blue line) condition

Parallel Signal Format

Every data byte is 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Data is transferred with the MSB (Most Significant Bit) first. The detailed data transfer format is shown in Figure 56 below.

The acknowledge bit must occur after every byte transfer and it allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. The acknowledge signal is defined as follows: the transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line low and it remains stable low during the high period of this clock pulse. Setup and hold times must also be taken into account. When SDA remains high during this ninth clock pulse, this is defined as the Not-Acknowledge signal (NACK). The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer. The only condition that leads to the generation of NACK from the SiT5346 is when the transmitted address does not match the slave address. When the master is reading data from the SiT5346, the SiT5346 expects the ACK from the master at the end of received data, so that the slave releases the SDA line and the master can generate the STOP or repeated START. If there is a NACK signal at the end of the data, then the SiT5346 tries to send the next data. If the first bit of the next data is “0”, then the SiT5346 holds the SDA line to “0”, thereby blocking the master from generating a STOP/(re)START signal.

Parallel Data Format

This I^2C slave module supports 7-bit device addressing format. The 8^{th} bit is a read/write bit and “1” indicates a read transaction and a “0” indicates a write transaction. The register addresses are 8-bits long with an address range of 0 to 255 (00h to FFh). Auto address incrementing is supported which allows data to be transferred to contiguous addresses without the need to write each address beyond the first address. Since the maximum register address value is 255, the address will roll from 255 back to 0 when auto address incrementing is used. Obviously, auto address incrementing should only be used for writing to contiguous addresses. The data format is 16-bit (two bytes) with the most significant byte being transferred first. For a read operation, the starting register address must be written first. If that is omitted, reading will start from the last address in the auto-increment counter of the device, which has a startup default of 0x00.

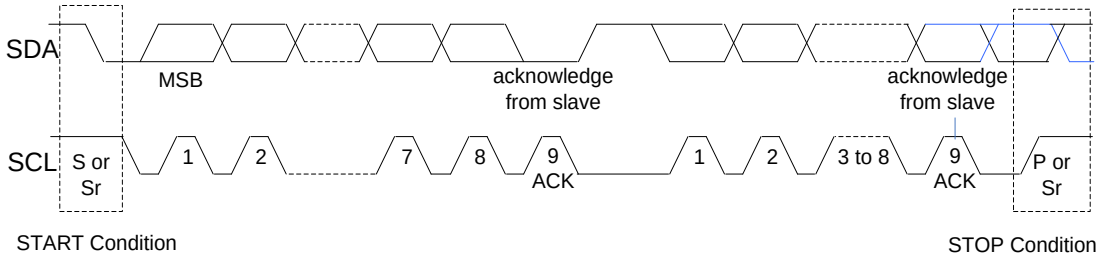


Figure 55. Parallel signaling format

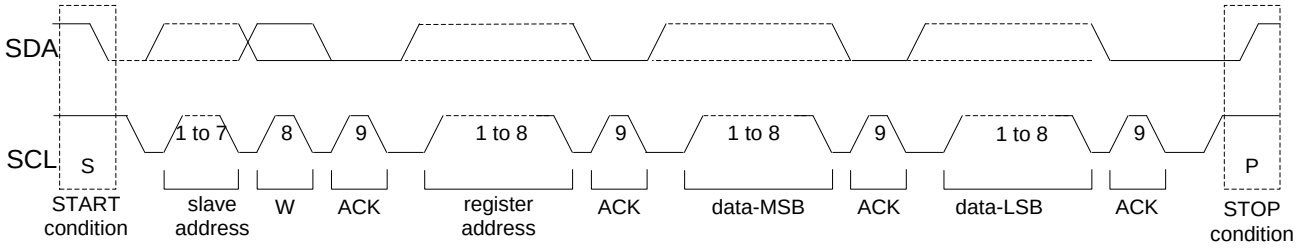


Figure 56. Parallel data byte format, write operation

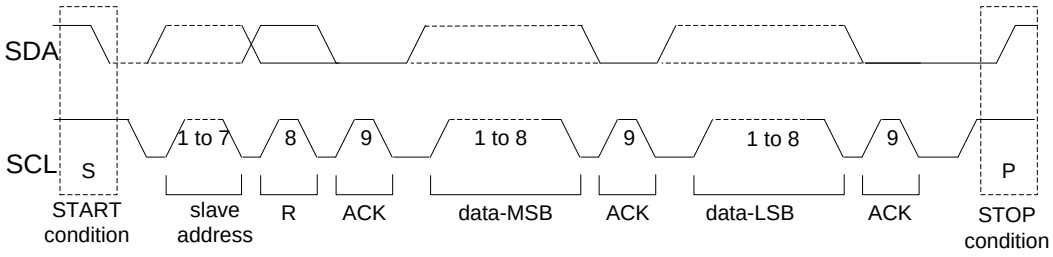


Figure 57. Parallel data byte format, read operation

Figure 58 below shows the I²C sequence for writing the 4-byte control word using auto address incrementing.

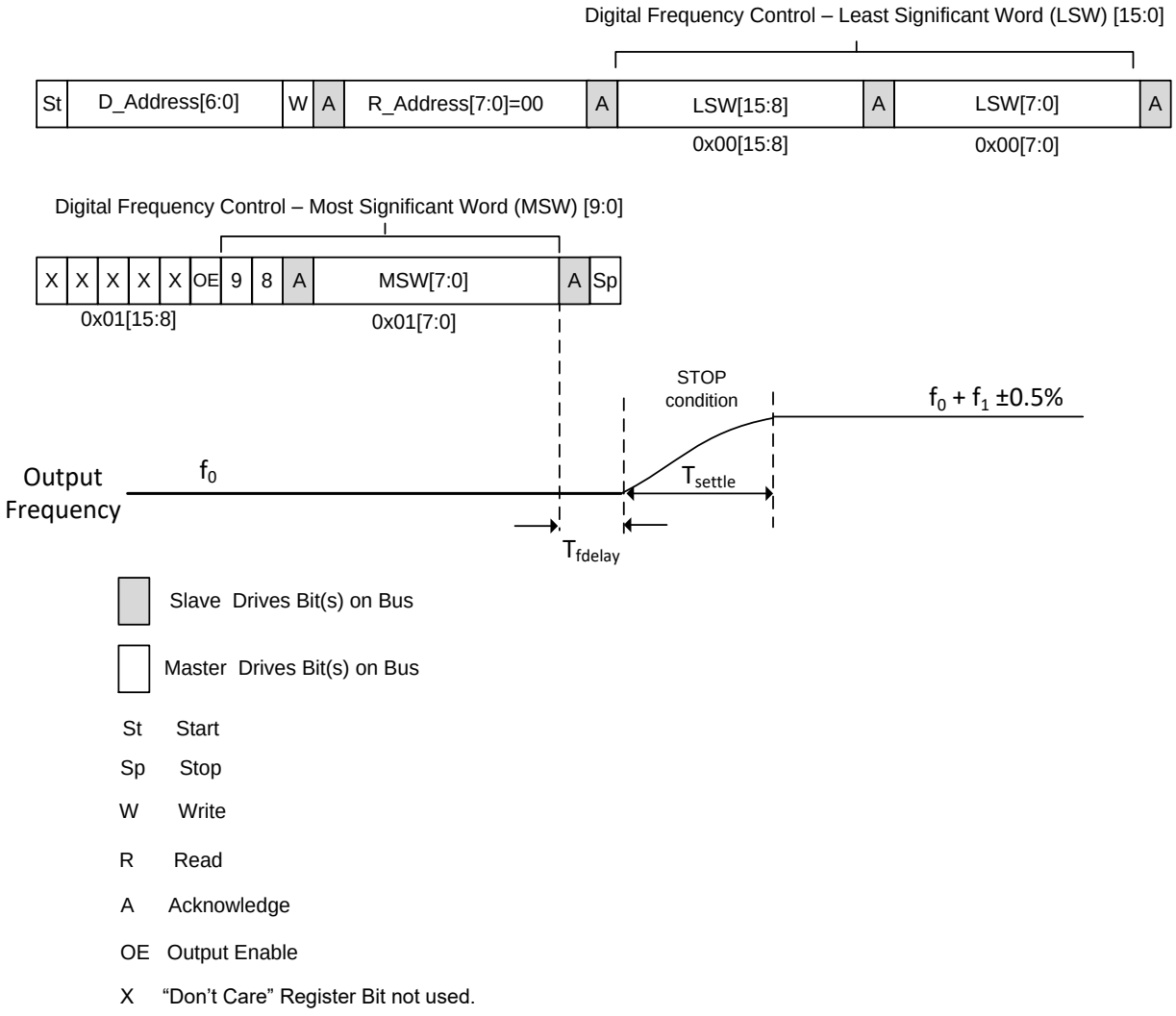


Figure 58. Writing the Frequency Control Word

Table 21. DCTCXO Delay and Settling Time

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Frequency Change Delay	T_{fdelay}	–	103	140	µs	Time from end of 0x01 reg MSW to start of frequency pull, as shown in Figure 58
Frequency Settling Time	T_{settle}	–	16.5	20	µs	Time to settle to 0.5% of frequency offset, as shown in Figure 58

I²C Timing Specification

The below timing diagram and table illustrate the timing relationships for both master and slave.

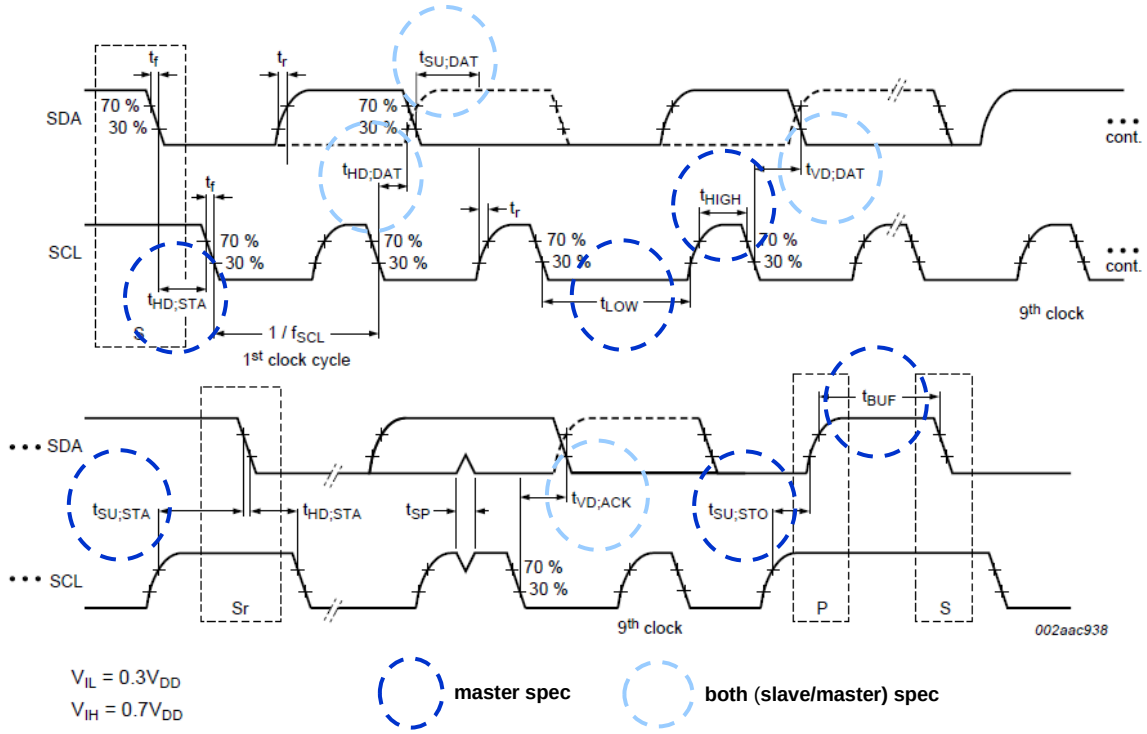


Figure 59. I²C Timing Diagram

Table 22. I²C Timing Requirements

Parameter	Speed Mode	Value	Unit
t_{SETUP}	FM+ (1 MHz)	> 50	nsec
	FM (400 KHz)	> 100	nsec
	SM (100 KHz)	> 250	nsec
t_{HOLD}	FM+ (1 MHz)	> 0	nsec
	FM (400 KHz)	> 0	nsec
	SM (100 KHz)	> 0	nsec
$t_{VD:AWK}$	FM+	> 450	nsec
	FM (400 KHz)	> 900	nsec
	SM (100 KHz)	> 3450	nsec
$t_{VD:DAT}$		NA (s-awk + s-data)/(m-awk/s-data)	

I²C Device Address Modes

There are two I²C address modes:

1) Factory Programmed Mode. The lower 4 bits of the 7-bit device address are set by ordering code as shown in Table 23 below. There are 16 factory programmed addresses available. In this mode, pin 5 is NC and the A0 I²C address pin control function is not available.

2) A0 Pin Control. This mode allows the user to select between two I²C Device addresses as shown in Table 24.

Table 23. Factory Programmed I²C Address Control[19]

I²C Address Ordering Code	Device I²C Address
0	1100000
1	1100001
2	1100010
3	1100011
4	1100100
5	1100101
6	1100110
7	1100111
8	1101000
9	1101001
A	1101010
B	1101011
C	1101100
D	1101101
E	1101110
F	1101111

Notes:
19. Table 23 is only valid for the DCTCXO device option which supports I²C Control.

Table 24. Pin Selectable I²C Address Control[20]

A0 Pin 5	I²C Address
0	1100010
1	1101010

Notes:
20. Table 24 is only valid for the DCTCXO device option which supports I²C control and A0 Device Address Control Pin.

Schematic Example

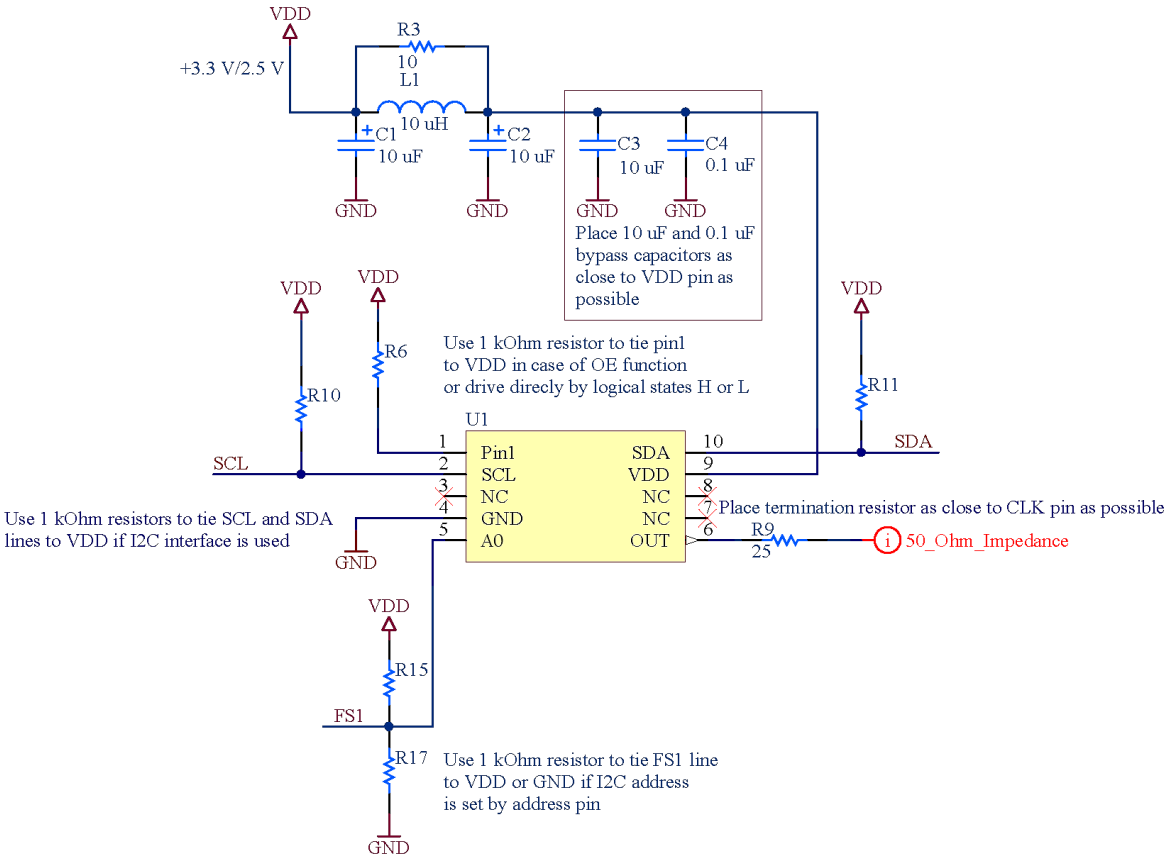
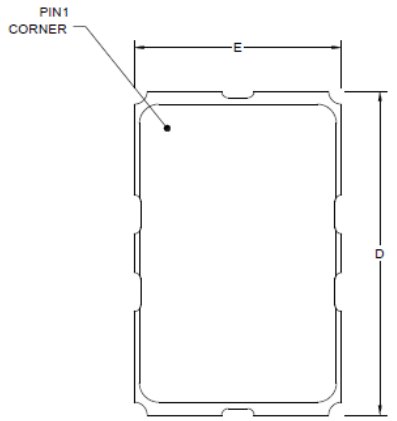


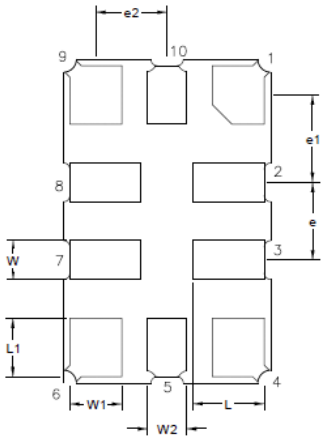
Figure 60. DCTCXO schematic example

Dimensions and Patterns

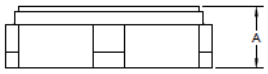
Package Size – Dimensions (Unit: mm)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

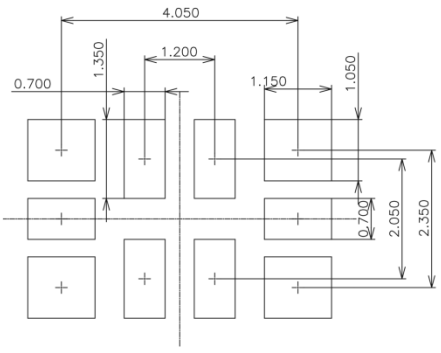
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.840	0.950	1.060
BODY SIZE	X	D	4.850	5.000	5.150
	Y	E	3.050	3.200	3.350
LEAD PITCH		e	1.070	1.200	1.330
		e1	1.220	1.350	1.480
		e2	0.970	1.100	1.230
LEAD LENGTH		L	0.970	1.100	1.230
		L1	0.770	0.900	1.030
LEAD WIDTH		W	0.470	0.600	0.730
		W1	0.670	0.800	0.930
		W2	0.470	0.600	0.730

NOTES

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
2. All dimensions are in millimeters.

Package Outline	
10L CQFN	POD-CQFN-010-E05032-036
5.000 x 3.200 x 0.950	
2018/10/11 Rev A02	

Recommended Land Pattern (Unit: mm)



Solder Print Layout	
10L Ceramic	SPL-001-RevA
5.0 x 3.2 x 0.95	
2017/06/20	

Layout Guidelines

- The SiT5346 uses internal regulators to minimize the impact of power supply noise. For further reduction of noise, it is essential to use two bypass capacitors (0.1 µF and 10 µF). Place the 0.1 µF capacitor as close to the VDD pin as possible, typically within 1 mm to 2 mm. Place the 10 µF capacitor within 2 inches of the device VDD and VSS pins.
- It is also recommended to connect all NC pins to the ground plane and place multiple vias under the GND pin for maximum heat dissipation.
- For additional layout recommendations, refer to the Best Design Layout Practices.

Manufacturing Guidelines

The SiT5346 Super-TCXOs are precision timing devices. **Proper PCB solder and cleaning processes** must be followed to ensure best performance and long-term reliability.

- **No Ultrasonic or Megasonic Cleaning:** Do not subject the SiT5346 to an ultrasonic or megasonic cleaning environment. Otherwise, permanent damage or long-term reliability issues to the device may result.
- **No external cover.** Unlike legacy quartz TCXOs, the SiT5346 is engineered to operate reliably, without performance degradation in the presence of ambient disturbers such as airflow and sudden temperature changes. Therefore, the use of an external cover typically required by quartz TCXOs is not needed.
- **Reflow profile:** For mounting these devices to the PCB, IPC/JEDEC J-STD-020 compliant reflow profile must be used. Device performance is not guaranteed if soldered manually or with a non-compliant reflow profile.
- **PCB cleaning:** After the surface mount (SMT)/reflow process, solder flux residues may be present on the PCB and around the pads of the device. Excess residual solder flux may lead to problems such as pad corrosion, elevated leakage currents, increased frequency aging, or other performance degradation. For optimal device performance and long-term reliability, thorough cleaning to remove all the residual flux and drying of the PCB is required as shortly after the reflow process as possible. Water soluble flux is recommended. In addition, it is highly recommended to avoid the use of any “no clean” flux. However, if the reflow process necessitates the use of “no clean” flux, then utmost care should be taken to remove all residual flux between SiTime device and the PCB. Note that ultrasonic PCB cleaning should not be used with SiTime oscillators.
- For additional manufacturing guidelines and marking/ tape-reel instructions, refer to SiTime Manufacturing Notes.

Additional Information

Table 25. Additional Information

Document	Description	Download Link
ECCN #: EAR99	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.	—
HTS Classification Code: 8542.39.0000	A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods.	—
Evaluation Boards	SiT6722EB Evaluation Board User Manual	https://www.sitime.com/support/user-guides
Demo Board	SiT6702DB Demo Board User Manual	https://www.sitime.com/support/user-guides
Time Machine II	MEMS oscillator programmer	http://www.sitime.com/support/time-machine-oscillator-programmer
Time Master Web-based Configurator	Web tool to establish proper programming	https://www.sitime.com/time-master-web-based-configurator
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	https://www.sitime.com/support/resource-library/manufacturing-notes-sitime-products
Qualification Reports	RoHS report, reliability reports, composition reports	http://www.sitime.com/support/quality-and-reliability
Performance Reports	Additional performance data such as phase noise, current consumption and jitter for selected frequencies	http://www.sitime.com/support/performance-measurement-report
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes

Revision History

Table 26. Revision History

Version	Release Date	Change Summary
0.50	7-Jan-2019	First release
0.51	19-Jan-2019	Improved 24 hour holdover stability specification for 0.2 and 0.25 ppm parts Improved I2C bus frequency specification
0.52	13-Feb-2019	Modified acceleration sensitivity spec
0.53	25-Feb-2019	Formatting changes Updated Stratum 3+ aging specs
0.54	22-Jul-2019	Modified ultra-low g-sensitivity spec
1.00	24-Sep-2020	Corrected typos for write/read I^2C polarity Clarified PCB cleaning instructions Added link for SiT6702DB Added ECCN and HTS codes Reduced initial tolerance for Stratum 3+ grade Updated typical performance plot for load sensitivity Formatting updates Added note for Theta Ja Changed conditions for 24-hour holdover stability spec Added Allan deviation spec and updated typical plot Updated DCTCXO Delay and Settling Time table Added 5 and 10 year aging specs for Stratum 3+ grade Added max and min aging specs for 1 and 20 years for Stratum 3+ grade, and changed ambient temperature to 85°C Slightly reduced minimum pull range specs and updated Tables 17 and 18 for Stratum 3+ grade Added max and min hysteresis specs for Stratum 3+ grade, clarified conditions with related figure Clarified 24-hour holdover stability spec condition Added max and min input voltage to Absolute Maximum Limits table Updated output impedance typical spec Updated ΔF/ΔT and F_dynamic min and max specs Clarified Initial Tolerance specification condition Relabeled “First Pulse Accuracy” parameter to “Time to Rated Frequency Stability” for clarity Tightened F_dynamic for Stratum 3+ from -40 to -20°C Revised Parallel Data Format section description and figures Fixed Ordering table Changed date format in rev table
1.11	21-Nov-2022	Updated Ordering packaging information with F option Updated hyperlinks and icons on page 1. Disclaimer update

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