

# GaAs IC 4 x 2 Switch Matrix 0.7–3.0 GHz



AS212-93

## Applications:

- DBS Switching Applications, Cable Modems, Cable TV

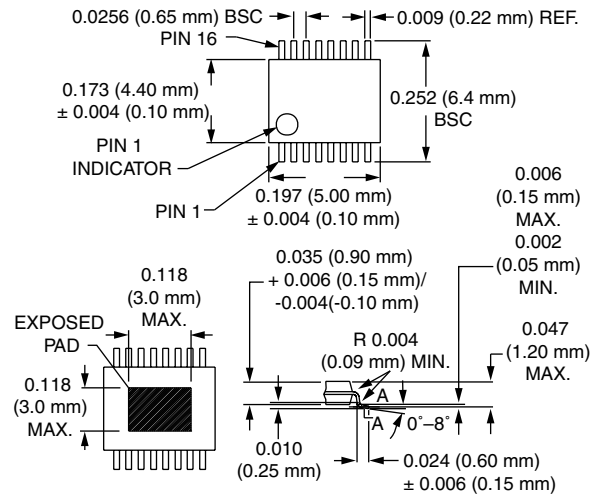
## Features

- Four Inputs, Two Output Switches
- Any Input Can Be Directed To Either Output
- Only Requires 4 Control Lines
- Low DC Power Consumption
- Small Low Cost TSSOP-16 Plastic Package
- High Isolation Between Ports

## Description

The AS212-93 is an IC FET 4 x 2 matrix switch in a low cost TSSOP-16 exposed paddle plastic package. The exposed paddle should be grounded. The AS212-93 enables 16 states directing any of the four inputs to any of the two outputs. DC block capacitors are required at

## TSSOP-16



each RF port. States are selected by 4 positive controls. All ports are absorptive. The AS212-93 switch is suitable for DBS switching applications.

## Electrical Specifications at 25°C (0, +5 V)

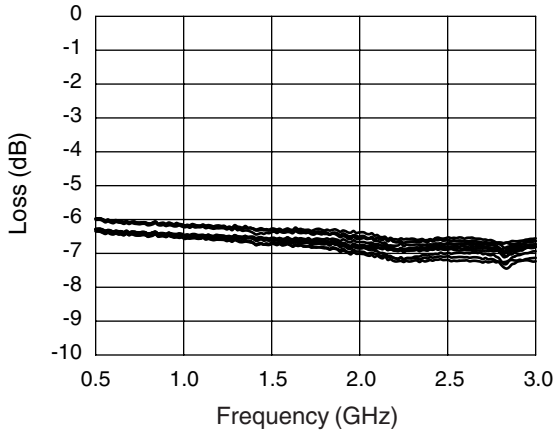
Parameter <sup>1</sup>	Frequency	Min.	Typ.	Max.	Unit
Insertion Loss	0.70–0.95		6.50	7.00	dB
	0.95–1.45		6.50	7.00	dB
	1.45–2.15		6.75	7.30	dB
	2.15–3.00		7.00	7.50	dB
Insertion Loss Flatness	0.70–3.00		1.0	2.0	dB
Isolation	0.70–0.95	25.0	33.0		dB
	0.95–1.45	23.0	28.5		dB
	1.45–2.15	22.5	28.5		dB
	2.15–3.00	19.5	25.5		dB
Return Loss Insertion Loss State	0.70–3.00	9	11		dB
Return Loss Isolation State	0.70–3.00	9	11		dB

## Operating Characteristics at 25°C (0, +5 V)

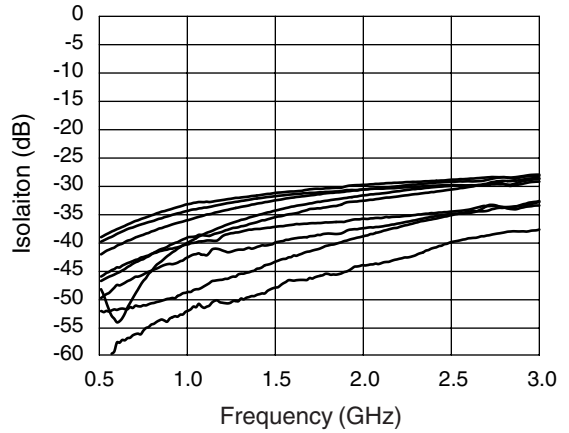
Parameter	Condition	Min.	Typ.	Max.	Unit
P <sub>-1</sub> dB	0, +5 V		12		dBm
V <sub>CC</sub>	@ 400 μA Max.	4.5		5.5	V
Control Voltages V <sub>1</sub> , V <sub>2</sub> , V <sub>3</sub> , V <sub>4</sub>	Low @ 50 μA Max.	0		0.2	V
	High @ 50 μA Max.	2.5		V <sub>CC</sub>	V

1. All measurements made in a 50 Ω system.

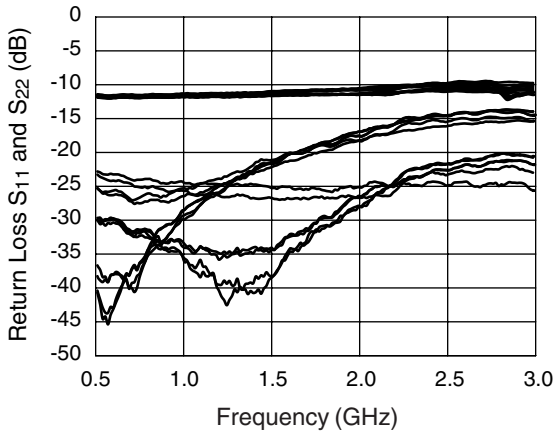
**Typical Performance Data (0, +3 V)**



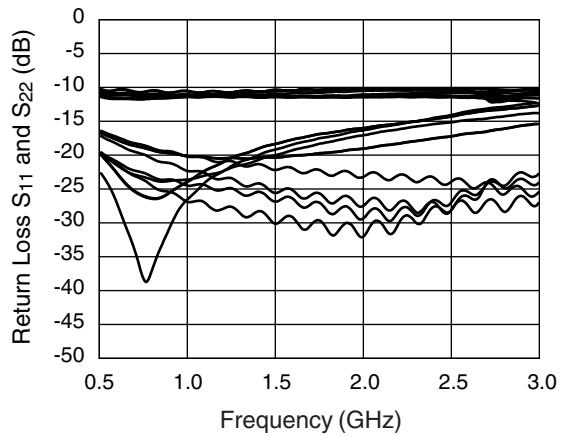
**Typical Insertion Loss  
(Various States Shown)**



**Typical Isolation  
(Including Worst Case)**



**Return Loss Insertion Loss State**



**Return Loss Isolation State**

**Absolute Maximum Ratings**

Characteristic	Value
RF Input Power	15 dBm
Supply Voltage	+6 V
Control voltage	+6 V
Operating Temperature	-40 to +85°C
Storage Temperature	-65 to +150°C

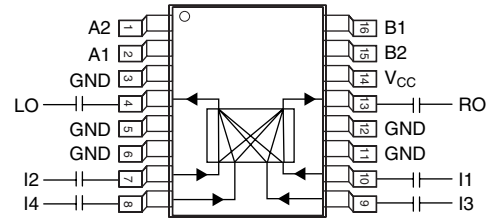
Note: Exceeding these parameters may cause irreversible damage.

### Truth Table

		Controls			
		For LO (Left Output)		For RO (Right Output)	
State #	Signal Path (Insertion Loss Path) <sup>1</sup>	SW A1	SW A2	SW B1	SW B2
0	I1->LO & I1->RO	0	0	0	0
1	I1->LO & I2->RO	0	0	0	1
2	I1->LO & I3->RO	0	0	1	0
3	I1->LO & I4->RO	0	0	1	1
4	I2->LO & I1->RO	0	1	0	0
5	I2->LO & I2->RO	0	1	0	1
6	I2->LO & I3->RO	0	1	1	0
7	I2->LO & I4->RO	0	1	1	1
8	I3->LO & I1->RO	1	0	0	0
9	I3->LO & I2->RO	1	0	0	1
10	I3->LO & I3->RO	1	0	1	0
11	I3->LO & I4->RO	1	0	1	1
12	I4->LO & I1->RO	1	1	0	0
13	I4->LO & I2->RO	1	1	0	1
14	I4->LO & I3->RO	1	1	1	0
15	I4->LO & I4->RO	1	1	1	1

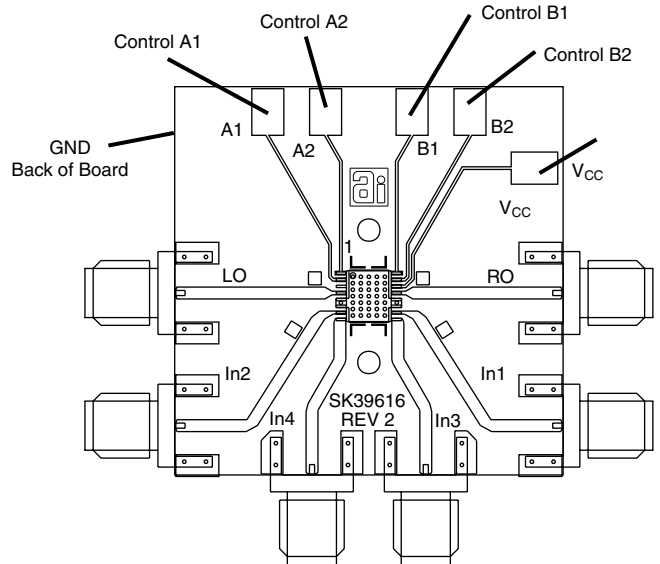
<sup>1</sup>. All other paths are in isolation.  
 "1" = 5 V.  
 "0" = 0 V.

### Pin Out

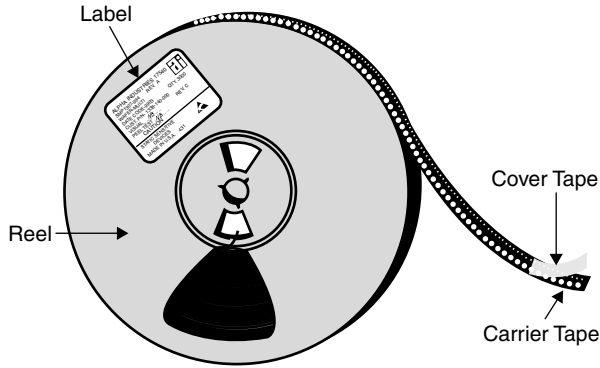


Unused leads and package bottom should be well grounded.  
 All paths are bidirectional.

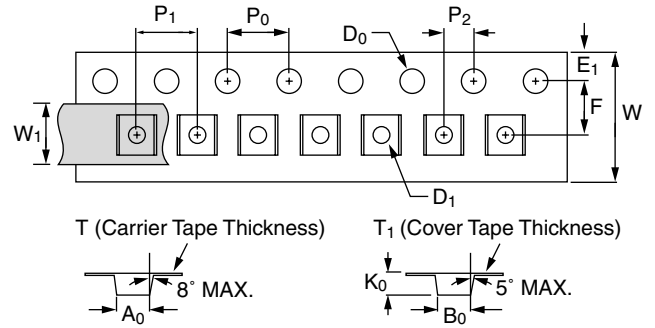
### Test Board



Bias V<sub>CC</sub> before applying bias to control lines.  
 Control lines need to be grounded for "0 V".  
 Control lines can not be left open circuit.



### Tape Dimensions

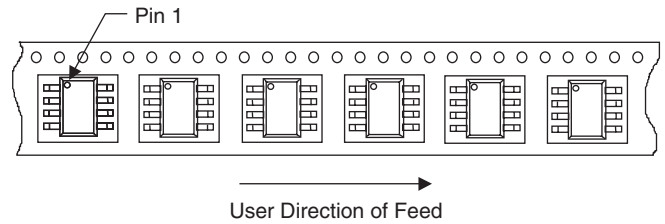


Description	Symbol	TSSOP-16
<b>Cavity</b>		
Length	A <sub>0</sub>	0.80±0.10
Width	B <sub>0</sub>	5.40±0.10
Depth	K <sub>0</sub>	1.60±0.10
Pitch	P <sub>1</sub>	8.00±0.10
Bottom Hole Diameter	D <sub>1</sub>	1.60±0.10
<b>Perforation</b>		
Diameter	D <sub>0</sub>	1.50±0.10
Pitch	P <sub>0</sub>	4.00±0.10
Position	E <sub>1</sub>	1.75±0.10
<b>Carrier Tape</b>		
Width	W	12.0±0.30
Thickness	T	0.30±0.05
<b>Cover Tape</b>		
Width	W <sub>1</sub>	9.20±0.10
Tape Thickness	T <sub>1</sub>	0.062±0.01
<b>Distance</b>		
Cavity to Perforation (Width Direction)	F	7.50±0.10
Cavity to Perforation (Length Direction)	P <sub>2</sub>	2.00±0.1

Note: All dimensions are in mm.

### SOIC, MSOP, QSOP, SSOP and TSSOP Devices

8, 10, 14, 16, 20, 28 Leads



Standard Reel Size	7"	13"
Standard Reel Quantity	1,000	3,000