SONY® CXA1365S

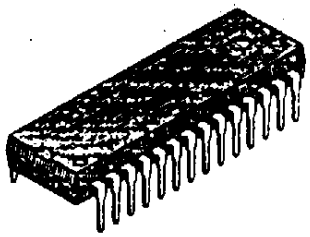
Sync Discrimination for CRT Display T-73-63

Description

CXA1365S is used for sync signal discrimination and waveform shaping in the CRT display.
There are 3 types of Sync input signals for discrimination.

V. separate sync signals
Composite sync or H. separate sync signals
Sync on video

28pin SDIP (Plastic)



Features

- Polarity and amplitude of input signals

	Polarity	Amplitude (Vp-p)
V. separate sync	: Positive/Negative	2 to 5
Composite sync	: Positive/Negative	0.2 to 1.2
H. separate sync	: Positive/Negative	2 to 5
Sync on video	: Negative (Sync signals part)	0.2 to 0.7
	(Video part)	0 to 1.5

Applications

CRT display monitor

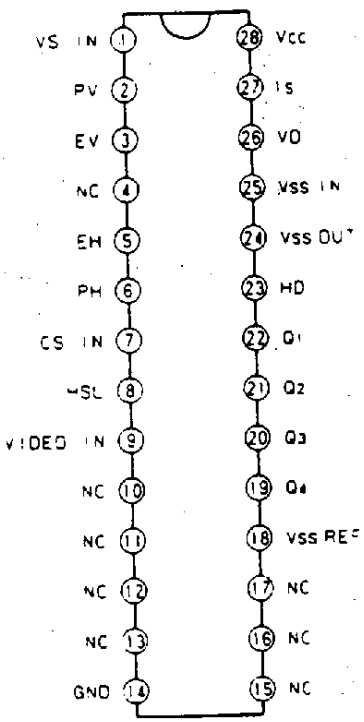
Operating Conditions

Supply voltage Vcc 8.5 to 9.5 V

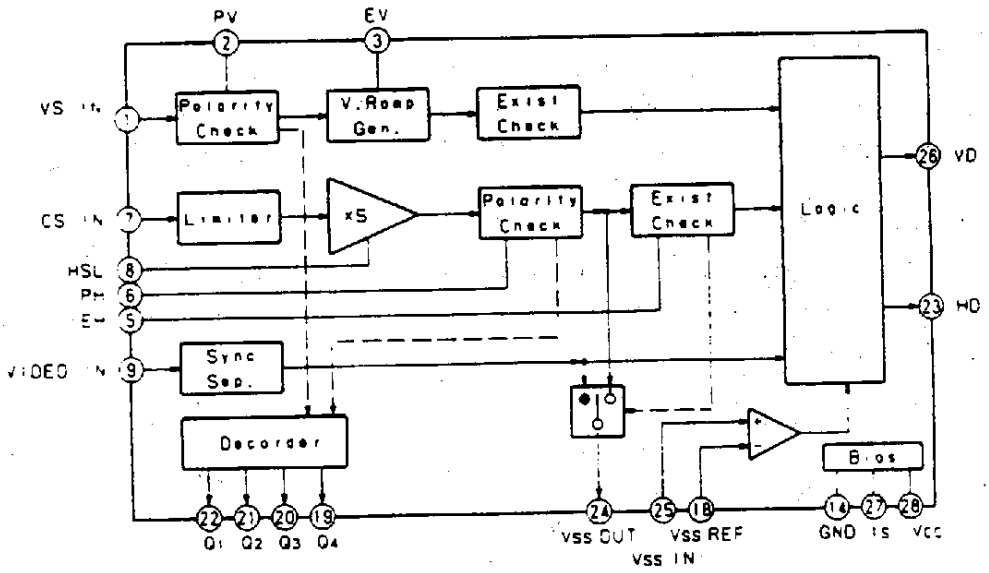
Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	Vcc	12	V
• Operating temperature	Topr	−20 to +75	°C
• Storage temperature	Tstg	−65 to +150	°C
• Allowable power dissipation	PD	1.35	W

Pin Configuration (Top View)



Block Diagram



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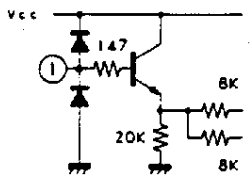
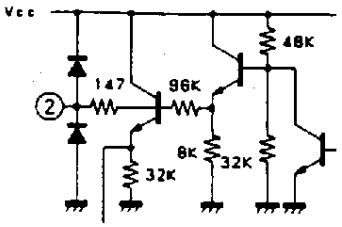
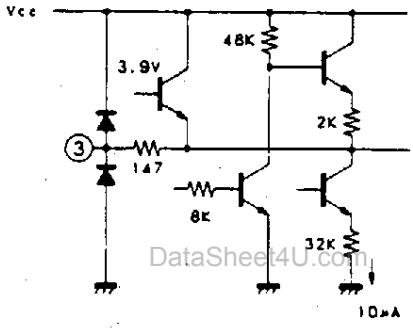
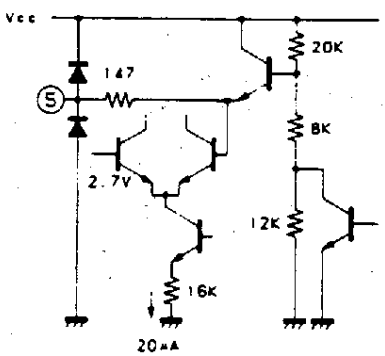
Pin Description and Equivalent Circuit

No.	Symbol	Pin voltage	Equivalent Circuit	Description
1	VS IN	——		V. separate sync is input at TTL level in both positive and negative polarity.
2 6	PV PH	0, 2.5V		This pin connects a 0.22µF integrating capacitor for the polarity check circuit to GND. When connecting the capacity at positive polarity, it is 2.5V, at negative polarity 0V and at no input 2.5V.
3	EV	3.2V to 6V		V. ramp waveforms generation part. Generates ramp waveforms synchronously with the input separate sync cycle and connects 0.22µF to GND. The ramp waveforms time constant during charge (Rise time) is almost determined through the 2kΩ and external 0.22µF. Same time constant during discharge (Fall time) is determined through the external 0.22 µF and the internal 10µA. When there is a V. separate sync, Pin 3 turns to 3.4V~6.0V, exist check is executed and sync existence established. When there is no V. separate sync, it turns to 3.2V.
4,10,11 12,13,15 16,17	NC	——	——	Pin not in use.
5	EH	2.0, 3.8V		During composite sync input, between this pin and GND is connected a 33 kΩ resistance for sync exist discrimination and a nearly peak hold circuit for 0.22µF capacitor. When there is a composite sync a nearly peak hold is executed at 3.4V to 3.8V, a comparison made with the 2.7V reference voltage and sync exist discriminated. When there is no composite sync, it turns to 2.0V.

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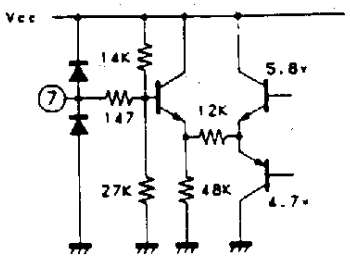
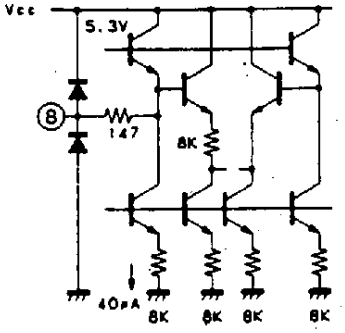
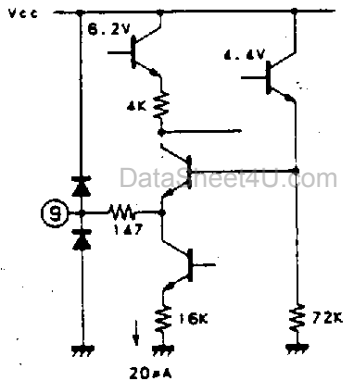
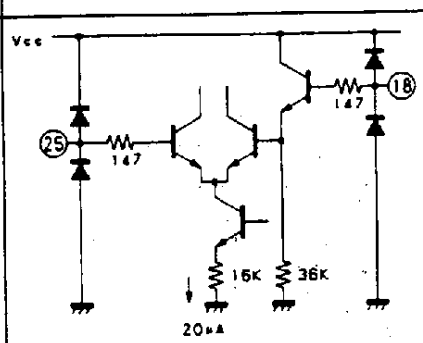
No.	Symbol	Pin voltage	Equivalent Circuit	Description
7	CS IN	5.9V		Inputs composite sync (Positive/Negative polarity) and H. separate sync (Positive/ Negative polarity). Amplitude either 0.2Vp-p and above or at TTL level.
8	HSL	4.6V		Connects limiter at composite sync input part and 0.1μF DC offset absorption capacitor for 5 times gain amplifier to GND.
9	VIDEO IN	3.0V		Inputs sync on video (Sync at negative polarity). Connects in series 0.47μF capacitor and 270Ω resistance between signal source and this pin. Slice level is determined by the relation between the total of 147Ω and the external resistance value multiplied by 20μA, the sync frequency, and sync width. When resistance value is small, slice level is low.
14	GND	0V	——	GND pin.
18	Vss REF	——		Reference pin for V. sync-separator. Provides reference voltage by connecting external resistance between Vcc and GND. Sets reference to 4.2V.

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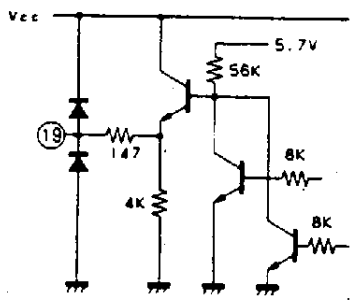
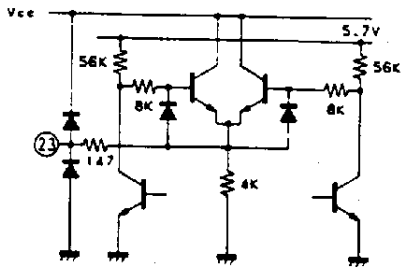
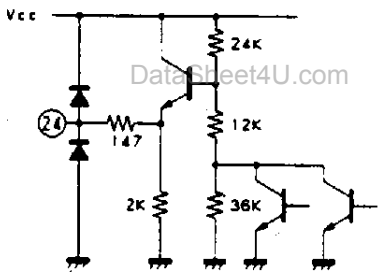
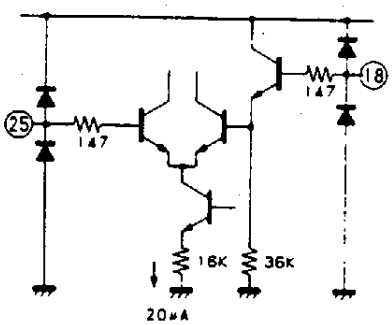
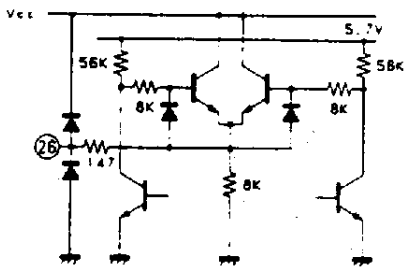
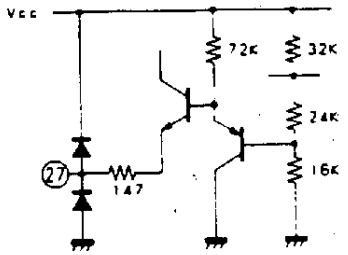
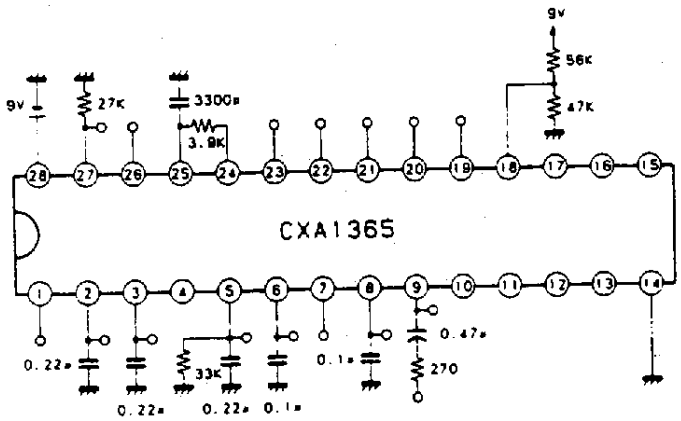
No.	Symbol	Pin voltage	Equivalent Circuit	Description
19 20 21 22	Q_4 Q_3 Q_2 Q_1	0, 4.5V		Outputs polarity information of synchronizing signal. High level at 4.5V. Low level at 0V. With V. sync separator polarity at P_V and composite sync polarity at P_H, the following table is obtained: P_V / P_H / Q_1 / Q_2 / Q_3 / Q_4 Negative / Negative / H / L / L / L Negative / Positive / L / H / L / L Positive / Negative / L / L / H / L Positive / Positive / L / L / L / H
23	HD	0, 4.5V		HD (H.Drive Pulse) output pin. Amplitude output at positive polarity from 0 to 4.5V.
24	Vss OUT	2.3, 5.3V		Composite sync or sync separated from sync on video is output for V. sync separator. Amplitude is at 2.3V to 5.3V and output at positive polarity.
25	Vss IN	——		Input pin for V. sync separator comparator. Connects an integrating circuit composed of 3.9kΩ resistance and 3300pF capacitor between pins 24 and 25. In the V. sync separator section when the integrated sync is anywhere between pin voltage and VBE (0.7V) voltage, the comparator operates.
26	VD	0, 4.5V		VD (V. Drive Pulse) output pin. Amplitude at 0 to 4.5V in positive polarity.

No.	Symbol	Pin voltage	Equivalent Circuit	Description
27	IS	2.0V		Reference voltage pin. Connects 27 kΩ resistance (1%) to GND. Current flowing through this resistance is taken as the reference current.
28	Vcc	9V		Supply pin. (9±0.5V)

Pin Voltage Test External Circuit



Electrical Characteristics (See the Electrical Characteristics Test Circuit)

No.	Item	Symbol	Test description	Test point	Min.	Typ.	Max.	Unit
1	VD output voltage	E_{VD}	Test VD output peak value during V. separate sync input. Input signal A. (tw=12.5μs)	VD (26pin)	(H level) 3.5 (L level) 0	4.5 0	5.0 0.4	V V
2	VD output pulse width ①	t_{V1}	Test VD output pulse width during V. separate sync input. Input signal A. (tw=12.5μs)	VD (26pin)	11.5	12.5	13.5	μs
3	VD output pulse width ②	t_{V2}	Test VD output pulse width during composite sync input. Input signal B. (tw=12.5μs)	VD (26pin)	8	10	12	μs
4	VD output pulse width ③	t_{V3}	Test VD output pulse width during sync on video input. Input signal C. (tw=12.5μs)	VD (26pin)	8	10	12	μs

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No.	Item	Symbol	Test description	Test point	Min.	Typ.	Max.	Unit
5	HD output voltage	E_{HO}	Test HD output peak value during composite sync input. Input signal D. (tw=0.65µs)	HD (23pin)	(H level) 3.5 (L level) 0	4.5 0	5.0 0.4	V V
6	HD output pulse width ①	th_1	Test HD output pulse width during composite sync input. Input signal D. (tw=0.65µs)	HD (23pin)	0.5	0.6	0.8	µs
7	HD output pulse width ②	th_2	Test HD output pulse width during composite sync input. Input signal E. (tw=2.5µs)	HD (23pin)	2.2	2.5	2.8	µs
8	HD output pulse width ③	th_3	Test HD output pulse width during composite sync input. Input signal B. (tw=0.65µs)	HD (23pin)	0.5	0.7	0.8	µs
9	HD output pulse width ④	th_4	Test HD output pulse width during sync on video input. Input signal C. (tw=0.65µs)	HD (23pin)	0.5	0.7	0.8	µs
10	PV voltage ①	V_{PV1}	Voltage integrated value of V. polarity discrimination circuit during V. separate sync input. Input signal F. (Negative logic)	PV (2pin)	——	0.0	—	V
11	PV voltage ②	V_{PV2}	Voltage integrated value of V. polarity discrimination circuit during V. separate sync input. Input signal G. (Positive logic)	PV (2pin)	——	2.5	—	V
12	PH voltage ①	V_{Ph1}	Voltage integrated value of H. polarity discrimination circuit during composite sync input. Input signal H. (Negative logic)	PH (6pin)	——	0.6	—	V
13	PH voltage ②	V_{Ph2}	Voltage integrated value of H. polarity discrimination circuit during composite sync input. Input signal I. (Positive logic)	PH (6pin)	——	2.1	—	V
14	EV voltage ①	V_{ev1}	Test voltage at V. ramp waveforms generation part during V. separate sync input. Input signal A.	EV (3pin)	——	6.0	—	V

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No.	Item	Symbol	Test description	Test point	Min.	Typ.	Max.	Unit
15	EV voltage ②	E_{ev2}	Test voltage at V. ramp waveforms generation part during V. separate sync input. No signal input.	EV (3pin)	—	3.2	—	V
16	EH voltage ①	V_{eh1}	Test sync existence and discrimination voltage during composite sync input. Input signal J.	EH (5pin)	—	3.4	—	V
17	EH voltage ②	V_{eh2}	Test sync existence and discrimination voltage during composite sync input. No signal input.	EH (5pin)	—	2.0	—	V
18	t delay ①	t_{d1}	Test delay difference between CS and HD during composite sync input. Or the time from CS (Positive logic) rise time (50%) to HD output rise time (50%). Input signal K.	HD (23pin)	—	200	250	ns
19	t delay ②	t_{d2}	Test delay difference between input signal sync and HD during sync on video input. Or the time from input sync fall time (50%) to HD output rise time (50%). Input signal C.	HD (23pin)	—	60	100	ns
20	Logic output voltage H	Q_H	Test polarity information output H level voltage of synchronizing signal.	Q_1 to Q_4 (19 pin~22pin)	3.5	4.5	5.0	V
21	Logic output voltage L	Q_L	Test polarity information output L level voltage of synchronizing signal	Q_1 to Q_4 (19 pin~22pin)	0	0	0.4	V
22	Consumption current	I_{CC}	V_{CC}=9V, Test consumption current during no signal input.	V_{CC} (28pin)	11	15	20	mA
23	Reference voltage	I_{REF}	V_{CC}=9V, Test reference current pin voltage during no signal input.	IS (27pin)	1.8	2.0	2.2	V

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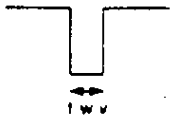
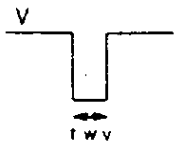
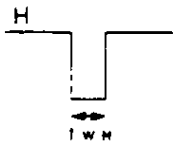
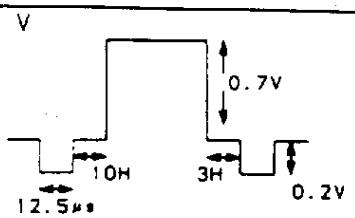
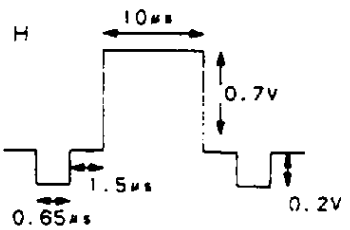
Signal	Item	V.SYNC IN (Pin1)	Composite SUNC IN (Pin 7)	VIDEO IN (Pin 9)
A	1, 2, 14	 fv=45Hz twv=12.5µs Negative logic 2Vpp		
B	3, 8		 fv=45Hz twv=12.5µs Negative logic 2Vpp  fH=80kHz twH=0.65µs Negative logic 2Vpp	
C	4, 9, 19			 fv=45Hz twv=12.5µs  fH=80kHz twH=0.65µs
D	5, 6		fH=80kHz twH=0.65µs Negative logic 0.25Vpp	
E	7		fv=80kHz twH=2.5µs Negative logic 0.25Vpp	

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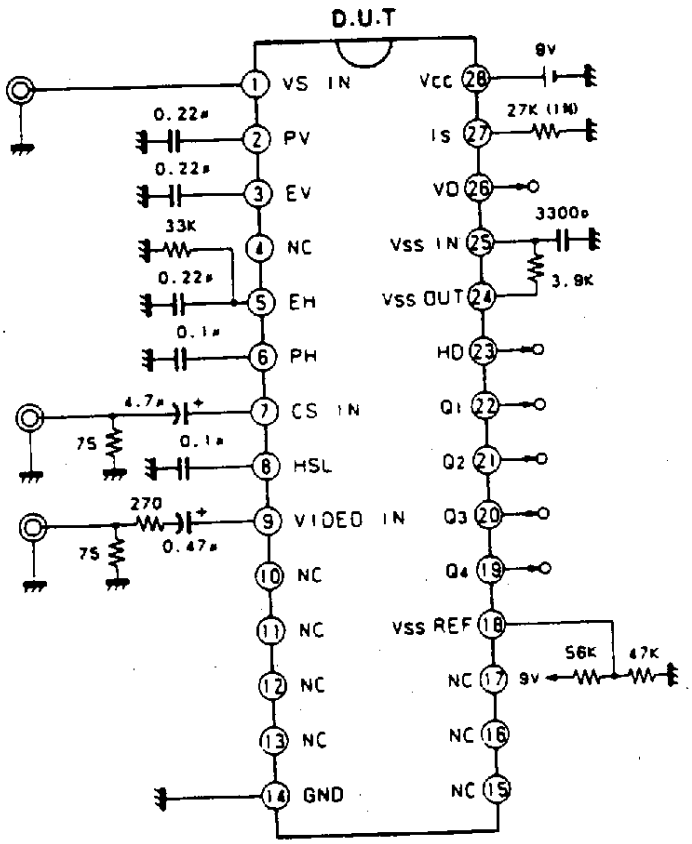
Signal	Item	V.SYNC IN (Pin1)	Composite SYNC IN (Pin 7)	VIDEO IN (Pin 9)
F	10	fv=120Hz twv=600µs Negative logic 2Vpp		
G	11	 fv=120Hz twv=600µs Positive logic 2Vpp		
H	12		fH=80kHz twH=2.5µs Negative logic 2Vpp	
I	13		fH=80kHz twH=2.5µs Positive logic 2Vpp	
J	16		fH=15kHz twH=3.3µs Negative logic 2Vpp	
K	18		fH=80kHz twH=0.65µs Positive logic 0.25Vpp	

Electrical Characteristics Test Circuit (Application Circuit)



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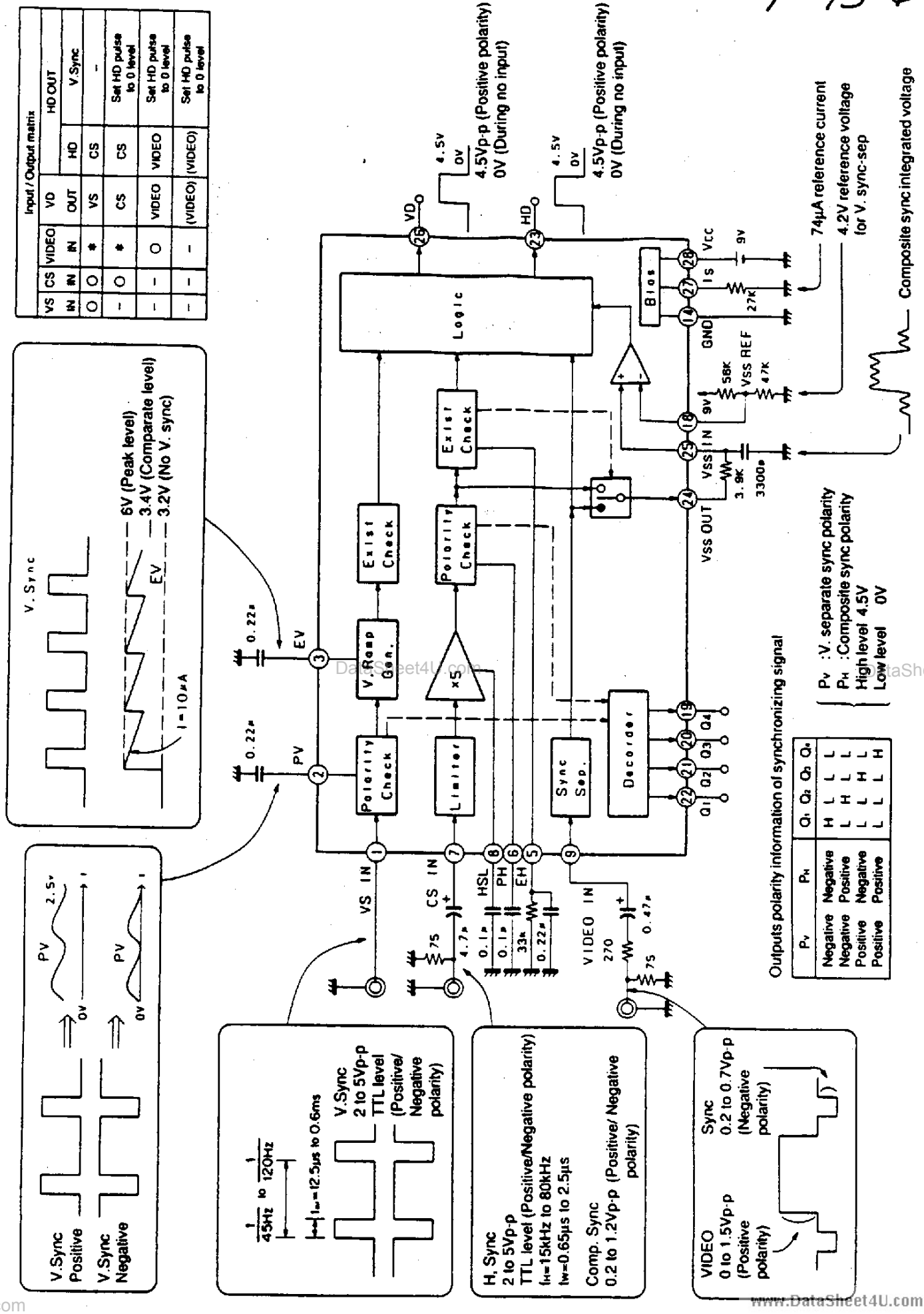
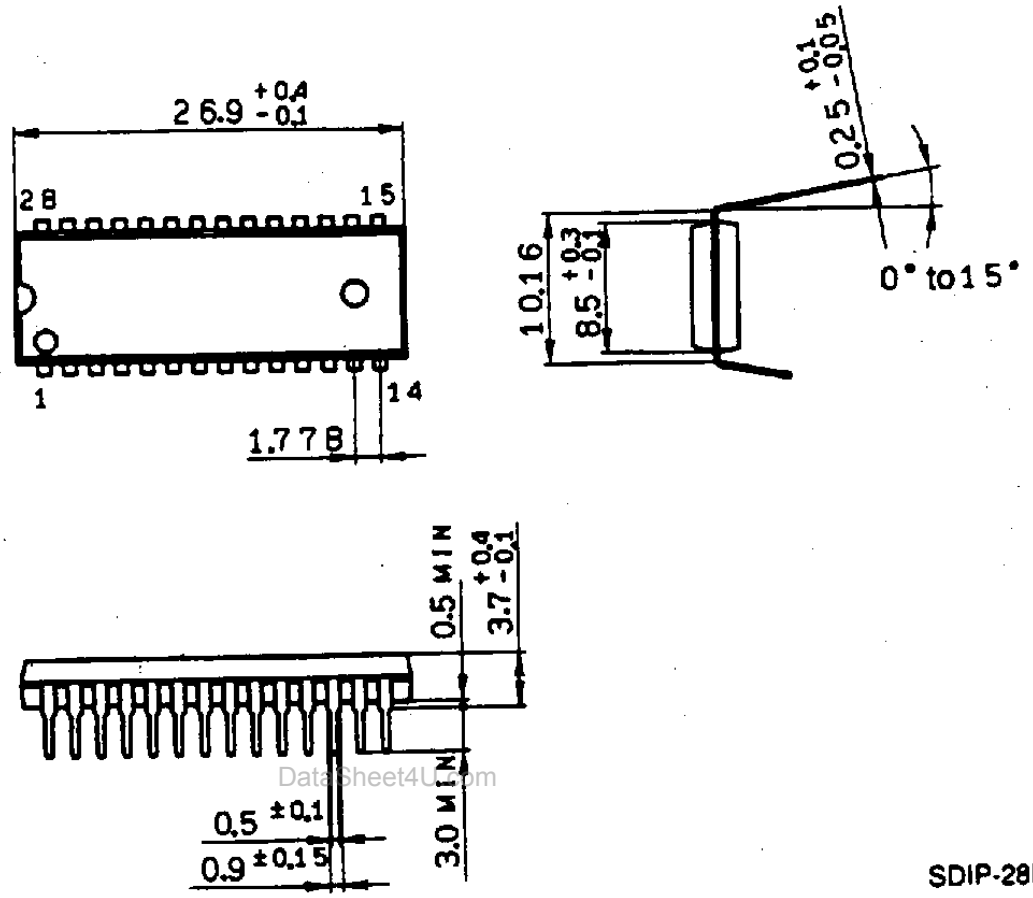
Operation and Input/Output Warveforms Description



SONY

Package Outline Unit: mm

CXA1365S 28pin SDIP (Plastic) 400mil 1.7g



SDIP-28P-01