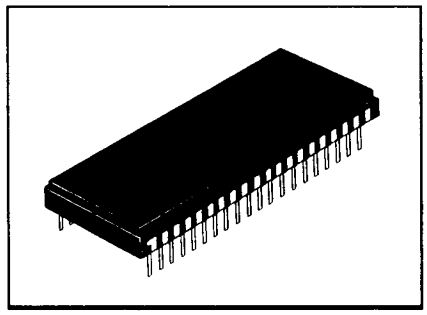
TELEDYNE PHILBRICK 40 ALLIED DRIVE, DEDHAM, MASSACHUSETTS 02026-9103

500ns MAX. 12-BIT A/D CONVERTER

4193/5

The 4193/4195 A/D converters are intended for applications requiring extremely fast, precise analog-to-digital conversion. The conversion speed is 500ns maximum. Proven monolithic circuits and recent advanced designs are combined to produce a device with improved performance but low cost. These devices are manufactured using thick and thin film hybrid technology.



The 4193 has an input range of 0 to 5V, while the 4195 input range is ±2.5V. Factory laser trims adjust all parameters so that most applications will require no additional adjustment. An optional gain adjust is provided for the user's convenience.

Signals are provided to interface the 4193 between the user's digital circuits and a track/hold (T/H). Conversions are initiated by a single pulse 50ns wide minimum. Data is valid 20ns before STATUS goes low. Data remains valid for at least 300ns after the next START pulse.

Timing signal (SAMPLE HOLD RESET) allows the user to increase overall sample rate with a T/H. After 380ns (typical), this signal changes state, signaling the converter is done using the analog input. This allows the T/H to begin acquiring the next sample while the 4193 is completing its internal digital encoding.

Power consumption is low typically, I.8W. Only three supplies are required: ±15V and +5V.

The 4193/4195 A/D converters are specified for 0°C to +70°C operation. The -83 versions are fully specified for operation over the -55° TO +125° temperature range and meet the high reliability requirements of MIL-STD-883, Class B. These devices can be ordered screened to Class S. Teledyne Philbrick is qualified to MIL-STD-1772.

FEATURES

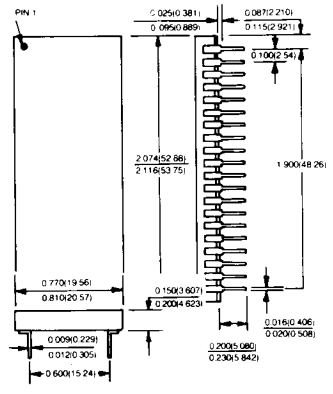
- ❑ 12-Bit Resolution
- ❑ 500ns.. Max. Conversion Time
- ❑ Low Power, 1.8W Max.
- ❑ Tri-State Output Buffers
- ❑ -55°C to +125°C Operation

APPLICATIONS

- ❑ Medical Instrumentation
- ❑ High Speed Data Acquisition

PIN DESIGNATIONS

1. ANALOG INPUT	15. +5V SUPPLY	28. BIT 7
2. ANALOG GROUND	16. REFERENCE OUT/IN	29. BIT 6
3. -15V SUPPLY	17. STATUS (E.O.C.)	30. BIT 5
4. TEST POINT (N/C)	18. DIGITAL GROUND	31. BIT 4
5. TEST POINT (N/C)	19. NC	32. BIT 3
6. GROUND	20. SAMPLE HOLD RESET	33. BIT 2
7. GROUND	21. TEST POINT (N/C)	34. BIT 1 (MSB)
8. N/C	22. +5V SUPPLY	35. TEST POINT (NC)
9. +15V SUPPLY	23. BIT 12 (LSB)	36. START CONVERT
10. N/C	24. BIT 11	37. OUTPUT ENABLE
11. GROUND	25. BIT 10	38. DIGITAL GROUND
12. GROUND	26. BIT 9	39. +5V SUPPLY
13. TEST POINT (N/C)	27. BIT 8	40. GROUND
14. GROUND		



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ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range: 4193/5	0°C to +70°C
4193/5-83	-55°C to +125°C
Storage Temperature	-65°C to +150°C
+15VC Supply (+V_{CC}, Pin 9)	-0.5V to +18V
-15V Supply (-V_{CC}, Pin 3)	+0.5 to -18V
+5V Supply (+V_{dd}, Pins 15, 22, 39)	-0.3 to +7V
Digital Inputs	-0.3V to +V_{dd}+0.3V
Analog Input: 4193	-1V to +6V
4195	-3.5V to +3.5V

SPECIFICATIONS (T_A = +25°C, Supply Voltages ±15V and +5V unless otherwise indicated). (1)

PARAMETER	MIN.	TYP.	MAX	UNITS
Analog Inputs				
Input Voltage Range: 4193	—	0 to 5	—	Volts
4195	—	-2.5 to +2.5	—	Volts
Input Impedance	—	1K/30	—	kΩ/pF
Digital Inputs				
Logic Levels: Logic "1"	+2.25	—	—	Volts
Logic "0"	0	—	+0.8	Volts
Loading: Start Convert Input I_{IH}	—	40		μA
Data Enable Input I_{IL}	—	-200	—	μA
Transfer Characteristics (3)				
Integral Linearity Error: Initial (+25°C)	—	±¼	±1	LSB
Over Temperature	—	±½	±1	LSB
Differential Linearity Error	—	±½	—	—
12-Bit No Missing Codes		Guaranteed Over Temperature		
Full Scale Absolute Accuracy Error (4)				
Initial (+25°C)	—	±0.05	±0.15	%FSR
Over Temperature	—	±0.1%	±0.3	%FSR
Unipolar Offset Error (4193) (5)				
Initial (+25°C)	—	±0.05	±0.1	%FSR
Over Temperature	—	±0.1	±0.15	%FSR
Drift	—	±10	—	PPM of FSR/°C
Bipolar Zero Error (4195) (6)				
Initial (+25°C)	—	±0.05	±0.1	%FSR
Over Temperature	—	±0.1	±0.2	%FSR
Drift	—	±10	—	PPM of FSR/°C
Gain Error (7):				
Initial (+25°C)	—	±0.05	±0.1	%
Over Temperature	—	±0.1	±0.3	%
Drift	—	±20	—	PPM/°C
Digital Outputs				
Output Coding (8): 4193		Straight Binary		
4195		Offset Binary		
Output Drive Capability (2)	5	—	—	LS TTL Loads
Dynamic Characteristics				
Conversion Time (9)	—	450	.500	nsec
Start Convert Pulse Width (10)	50	—	—	nsec
Delay Falling Edge of Start to Status "1"	—	25	—	nsec
Delay Falling Edge of Start to Previous Output Data Invalid	200	300	—	nsec
Delay Falling Edge of Status to Output Data Valid	—	—	0	nsec

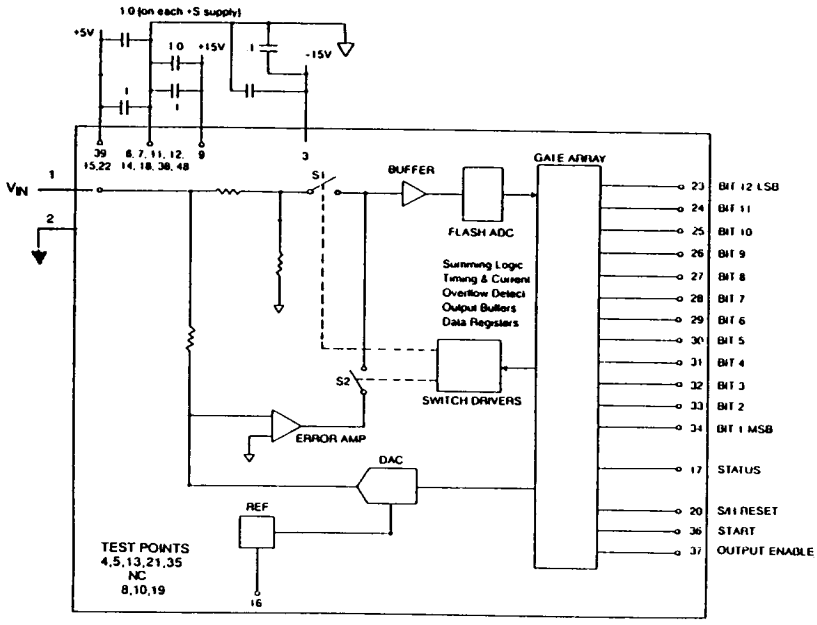

Figure 1. 4193 Pin Connections and Block Diagram

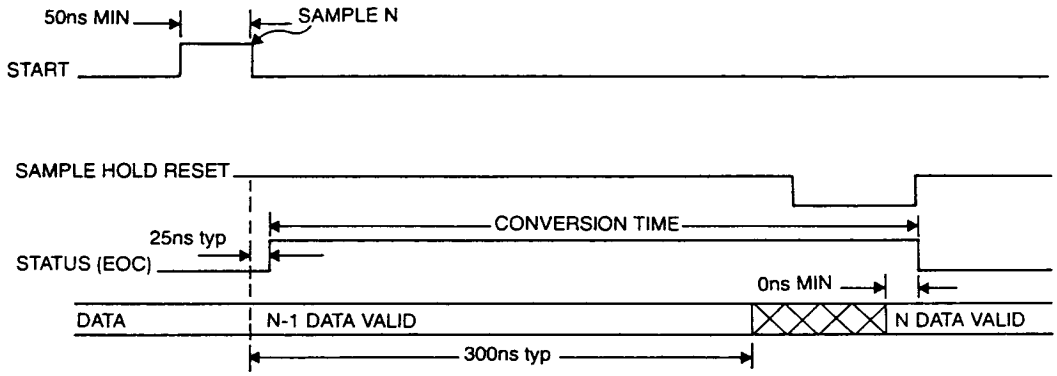

Figure 2. Conversion Timing

Circuit Description

The 4193 circuit uses a two stage subranging technique. First the input is approximated to seven bits. Then the seven bit word is applied to an accurate 12 bit DAC. The output of the DAC and the input are subtracted and amplified to create an error signal which is then digitized to seven bits. Combining the first and second seven bit word results in a 12 bit accurate result. See Figure 1, Pin Connections and Block Diagram.

The circuit uses a flash converter, a 7 bit DAC with >12 bit accuracy, and a digital gate array. Analog switches are used to multiplex the input of the flash converter between the analog input and the error signal, thus saving the cost and power of a second flash converter.

The timing of the ADC is initiated by a single START pulse 50ns wide minimum. See Figure 2, Conversion Timing. STATUS goes high on the falling edge of START. The conversion is complete when STATUS goes low. SAMPLE HOLD RESET signals the 4193 is done using the analog input on its falling edge. Using this signal to control the timing of a track and hold amplifier improves the conversion rate. While the ADC is completing the conversion, the T/H may begin acquiring the next sample. See the 4193-4860 application for an example.

The analog input signal is encoded to seven bits just after the falling edge of the START pulse. The data is saved in the gate array and transmitted to the DAC.

The output of the DAC is subtracted from the analog input and the difference is amplified. Meanwhile S1 opens and S2 closes. The error signal goes to the Flash ADC.

After the DAC and Error Amp settle, the error signal is encoded to seven bits. The data is sent to the gate array. S2 opens and S1 closes. SAMPLE HOLD RESET goes low signaling that the ADC is done using the analog input.

The data from the second encode is added to the data from the first encode. The result is a twelve bit word precisely scaled to the analog input.

Using a 4860 with 4193

This example shows the interconnections and timing requirements for a 4860 used with the 4193 ADC. See Figure 3, 1.33 MSPS using a 4193 and 4860.

The 4860 is driven from the 4193 through a D type flip-flop. Prior to the start pulse 200ns must be allowed for the 4860 to acquire the input signal. A l00ns (minimum) start pulse occurs which is applied to the 4193 and D flip-flop. Hold goes low after the rising edge of the start pulse. About 100ns later, the start pulse goes low. Then the first conversion of the two step conversion occurs. Since the conversion begins right after start goes low, time must be allowed for the 4860 and the 4193 to sett' into hold. The 4193 is done with the analog inpt. about 375ns after the conversions begins (negative edge of start). $\overline{\text{Hold}}$ goes high putting the 4860 into track. This allows aquisition time and conversion time to overlap, increasing the system update rate. The combined 4860 and 4193 conversion time can be as low as 750ns with full scale dynamic inputs.

	INPUT VOLTAGE (VOLTS)		OUTPUT CODING
SCALE	4193	4195	DATA
F.S.	5.0000	2.5000	1**********
F.S. - 1 LSB	4.9988	2.4988	111111111111
¾ F.S. + ½ LSB	3.7506	1.2506	110000000000
¾ F.S.	3.7500	1.2500	1**********
½ F.S. + ½ LSB	2.5006	0.0006	100000000000
½ F.S.	2.5000	0.0000	0**********
½ F.S. - ½ LSB	2.4994	-0.0006	011111111111
¼ F.S.	1.2500	-1.2500	0**********
¼ F.S. - ½ LSB	1.2494	-1.2506	001111111111
1 LSB	+0.0012	-2.4988	000000000001
0	0.0000	-2.5000	000000000000

Table A. Input Voltage and Output Coding

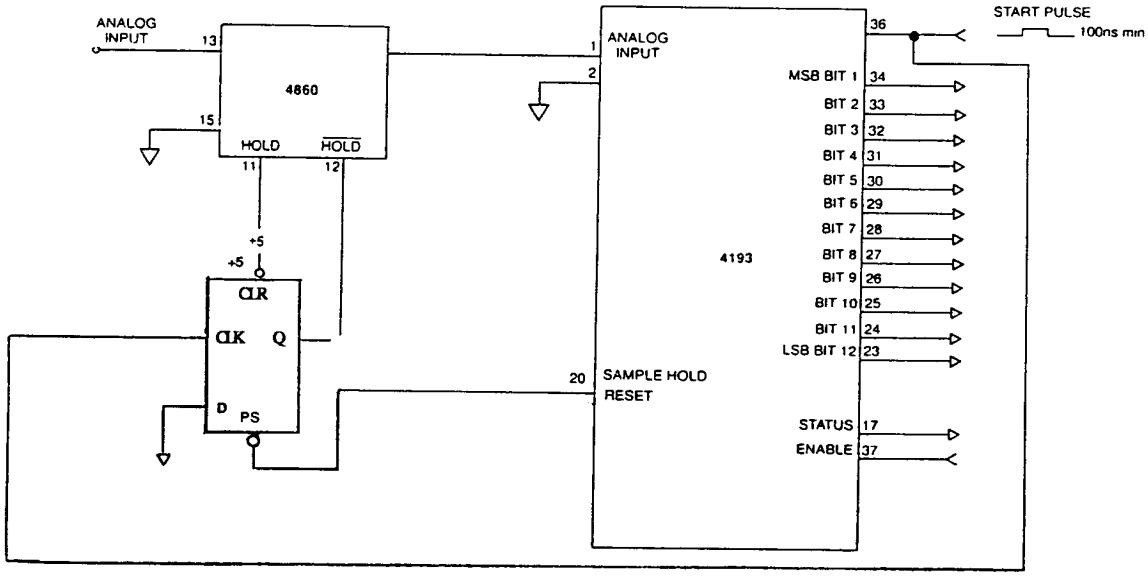

Figure 3. 1.33 MSPS using a 4193 and 4860

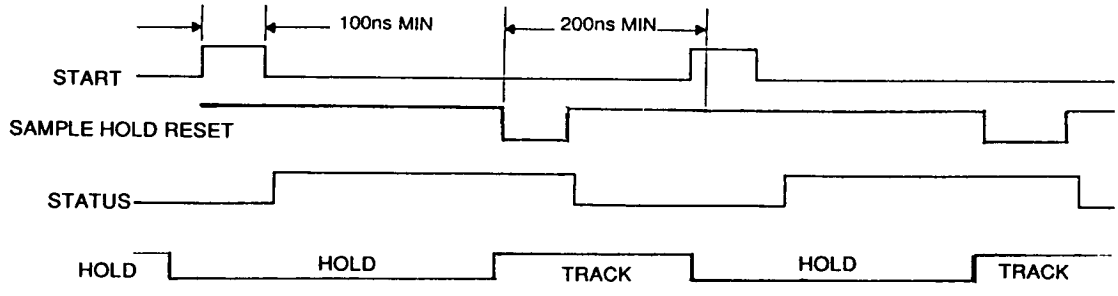

Figure 4. 4193/4860 Timing

Printed in U.S.A. 2/88 2K Rev #1

TELEDYNE PHILBRICK

ERRATA SHEET

4193/95 500NS MAX. 12-BIT A/D CONVERTER

REV #1 2/88 2K (*CODE ON DATA SHEET*)

PIN DESIGNATIONS:

To read:

PIN 6	ANALOG GROUND
PIN 7	ANALOG GROUND
PIN 11	DIGITAL GROUND
PIN 12	ANALOG GROUND
PIN 19	TEST POINT (N/C)
PIN 40	DIGITAL GROUND

FEATURES:

To Read: **Low Power, 1.72 W - TYPICAL --- not** 1.8W Max.

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3/88

PARAMETER	MIN.	TYP.	MAX	UNITS
Reference Output				
Internal Reference: Voltage	—	+5.000	—	Volts
Accuracy	—	±2	—	%
Drift	—	±10	—	PPM/°C
External Current	—	5	—	μA
Power Supply Requirements				
Power Supply Range: +15V Supply	+14.55	+15	+15.45	Volts
-15V Supply	-14.55	-15	-15.45	Volts
+5V Supply	+4.75	+5	+5.25	Volts
Power Supply Rejection: +15V Supply	—	±0.02	—	%FSR/%Vs
-15V Supply	—	±0.02	—	%FSR/%Vs
+5V Supply	—	±0.002	—	%FSR/%Vs
Current Drain: +15V Supply	—	20	26	mA
-15V Supply	—	38	48	mA
+5V Supply	—	170	210	mA
Power Consumption	—	1.72	2.16	W
Thermal Characteristics				
Thermal Impedance: Case to Ambient, CA	—	17.2	—	°C/W
Junction to Case, JC	—	7.8	—	°C/W
Junction to Ambient, JA	—	25	—	°C/W

NOTES

(1) Unless otherwise indicated, listed specifications apply for all 4193 and 4195 models. Drift specifications apply over each device's specified temperature range.
(2) One LS TTL load is defined as sinking 20μA with a logic "1" applied and sourcing 0.4mA with a logic "0" applied.
(3) FSR = Full Scale Range. For both the 4193 and 4195, FSR = 5 volts. For a 12-bit converter, 1 LSB = 0.024% FSR.
(4) Full Scale Accuracy Error is defined as the difference between the actual and the ideal input voltage at which the 1111 1111 1110 to 1111 1111 1111 digital-output transition occurs. It includes offset, gain, linearity and noise errors and encompasses the drifts of those errors when specified over temperature.
(5) Unipolar offset error is defined for the 4193 as the difference between the actual and ideal input voltage at which the 0000 0000 0000 to 0000 0000 0001 transition occurs.
(6) Bipolar zero error is defined as the difference between the actual and the ideal input voltage at which the 0111 1111 1111 to 1000 0000 0000 transition occurs for the 4195.
(7) Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full input voltage span from the input voltage at which the output changes from 1111 1111 1111 to 1111 1111 1110 to the input voltage at which the output changes from 0000 0000 0001 to 0000 0000 0000. Initial gain error is adjustable to zero with an external potentiometer.
(8) See Output Coding table for details.
(9) Conversion time is defined as the width of the converter's Status output pulse. See Timing Diagram.
(10) Actual conversion process is initiated on the falling edge of the Start Convert Signal. See Timing Diagram.

Applying the 4193

The 4193 is designed for digitizing fast changing input signals. Combined with a track/hold (T/H), such as the 4860, it will sample dynamic signals at better than 1.3 MSPS (Mega Samples per Second). This assures digitized data with low harmonic distortion and good signal to noise ratio.

Grounding and Bypassing

Careful layout is a must for all high speed circuits and the 4193 is no exception. A ground plane is highly recommended. It will improve the ADC's performance and also the associated drive circuitry, amplifier or track and hold. The ±15V supplies should be bypassed with 1.0μf tantalum capacitors in parallel with .1μf ceramic capacitors. The +5V supply should be bypassed with a 1.0μf tantalum capacitor in parallel with a .1μf ceramic on each +5V pin (15, 22, 39). All grounds should be connected together to the ground plane. All three power supplies are used as analog supplies. In addition, the +5V supply is a digital supply.

Input Drive Requirements

The 4193 is easy to drive. The input resistance is nominally 1.0KΩ. Unlike successive approximation converters very little noise is generated at the analog input. However, best performance is assured by using a wide bandwidth low output impedance driver.

Output Coding

The 4193 has straight binary and the 4195 has offset binary coding. See Table A, Output Coding, for details.

Gain Adjust

Pin 16 has a two way function. The internal reference may be used by leaving this terminal open or adding a small (.1μf) capacitor to ground. An external reference may be used also. Connect a +5.000V reference to this pin. Gain may also be adjusted ±.5% using the circuit below.