TC40H192P/F
TC40H193P/F

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

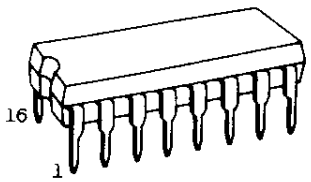
TC40H192 SYNCHRONOUS BCD UP/DOWN COUNTER
(DUAL CLOCK WITH CLEAR)
TC40H193 SYNCHRONOUS 4-BIT BINARY UP/DOWN COUNTER
(DUAL CLOCK WITH CLEAR)

The TC40H192 and the TC40H193 are synchronous type 4-bit up/down counters.

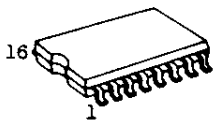
CLEAR input is active at "H" level, and PRESET input at "L" level, respectively. Both of them perform asynchronous operation.

The UP COUNT input and DOWN COUNT input of CLOCK are independent, and perform COUNT operation at the rising edge of pulse, respectively.

The TC40H192 and the TC40H193 are compatible in function and pin assignment with the TTL74192/74193.



DIP16(3D16A-P)

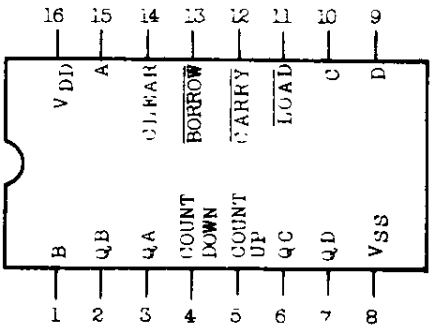


MFP16(F16GC-P)

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5 ∿ V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5 ∿ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ∿ V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Storage Temperature	Tstg	-65 ∿ 150	°C
Lead Temp./Time	Tsol	260°C • 10 sec	

PIN CONNECTION



TRUTH TABLE

TC40H192 /193

COUNT UP	COUNT DOWN	$\overline{LOAD}$	CLEAR	ACTION
↑	H	H	L	COUNT UP
↓	H	H	L	NO COUNT
H	↑	H	L	COUNT DOWN
H	↓	H	L	NO COUNT
✱	✱	L	L	PRESET
✱	✱	✱	H	RESET

✱ Don't care

TC40H192

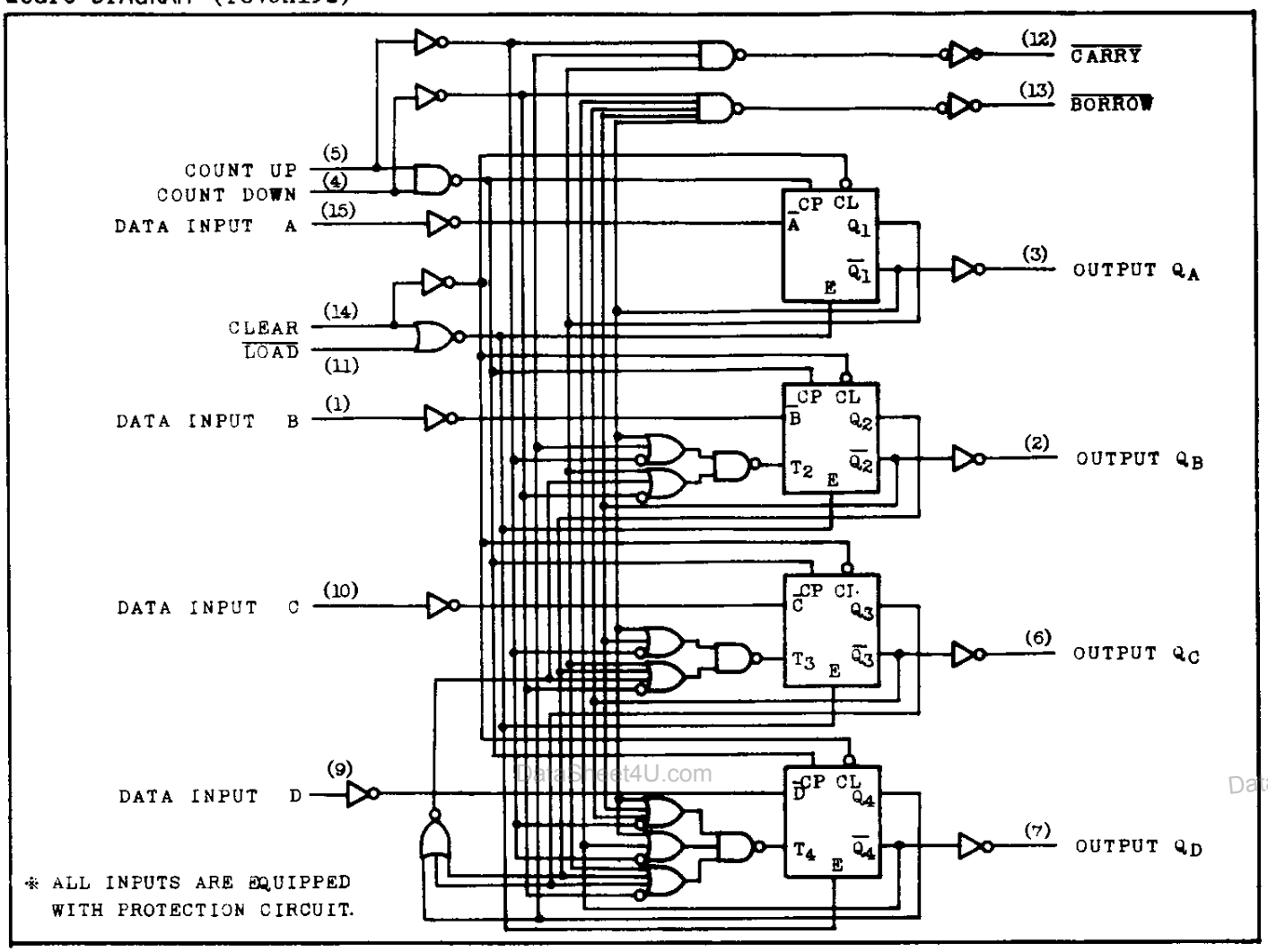
COUNT	Q_A	Q_B	Q_C	Q_D
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

TC40H193

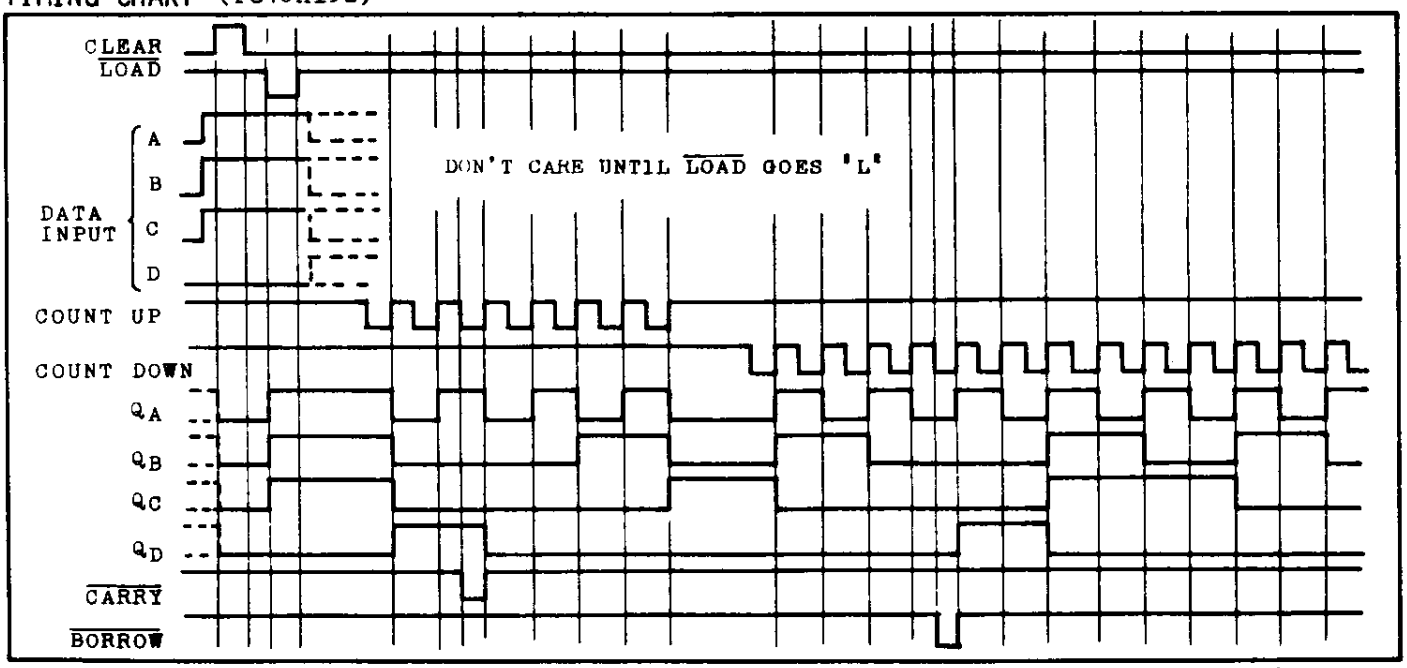
COUNT	Q_A	Q_B	Q_C	Q_D
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
A	L	H	L	H
B	H	H	L	H
C	L	L	H	H
D	H	L	H	H
E	L	H	H	H
F	H	H	H	H

TC40H192P/F
TC40H193P/F

LOGIC DIAGRAM (TC40H192)

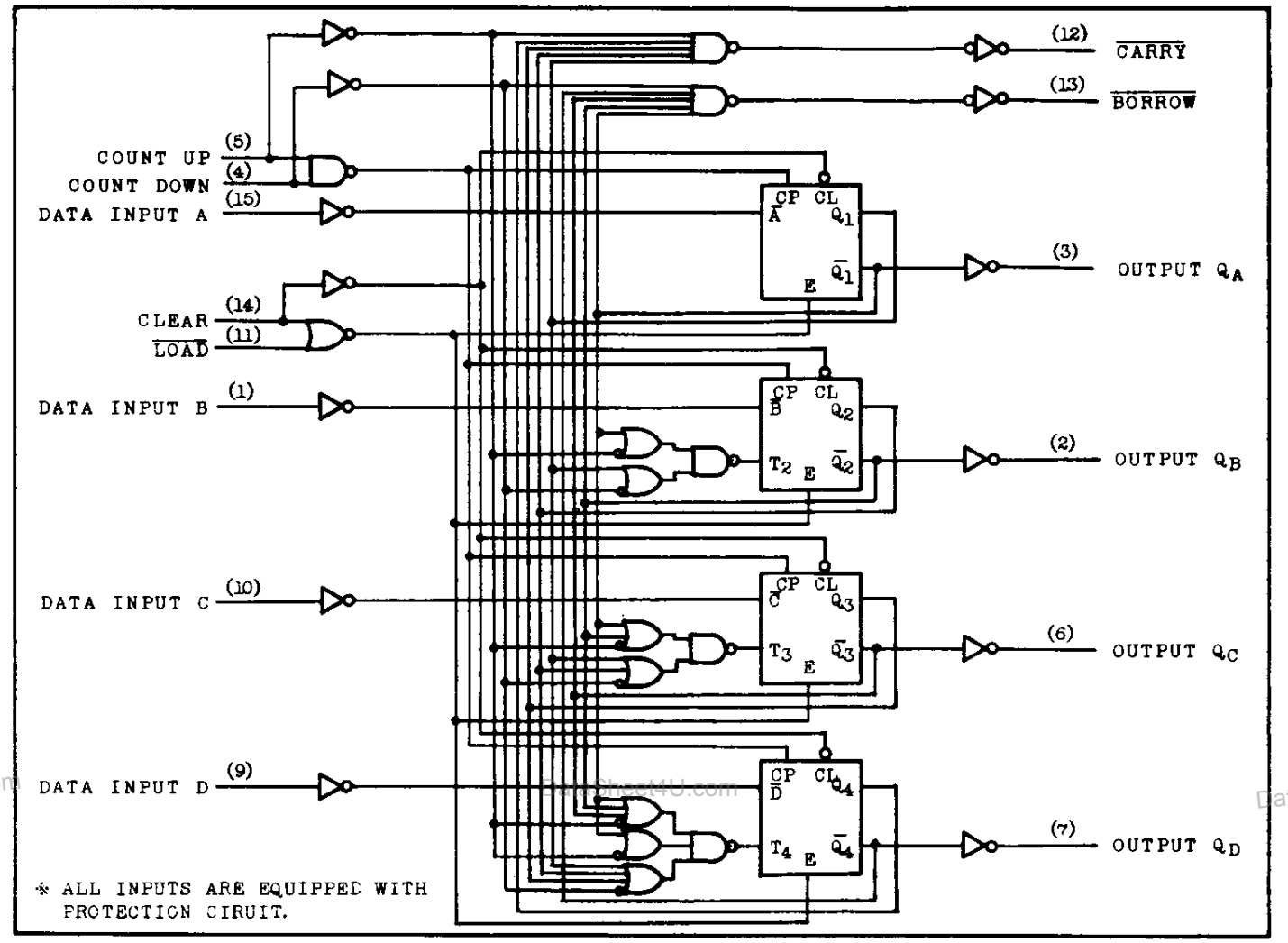


TIMING CHART (TC40H192)

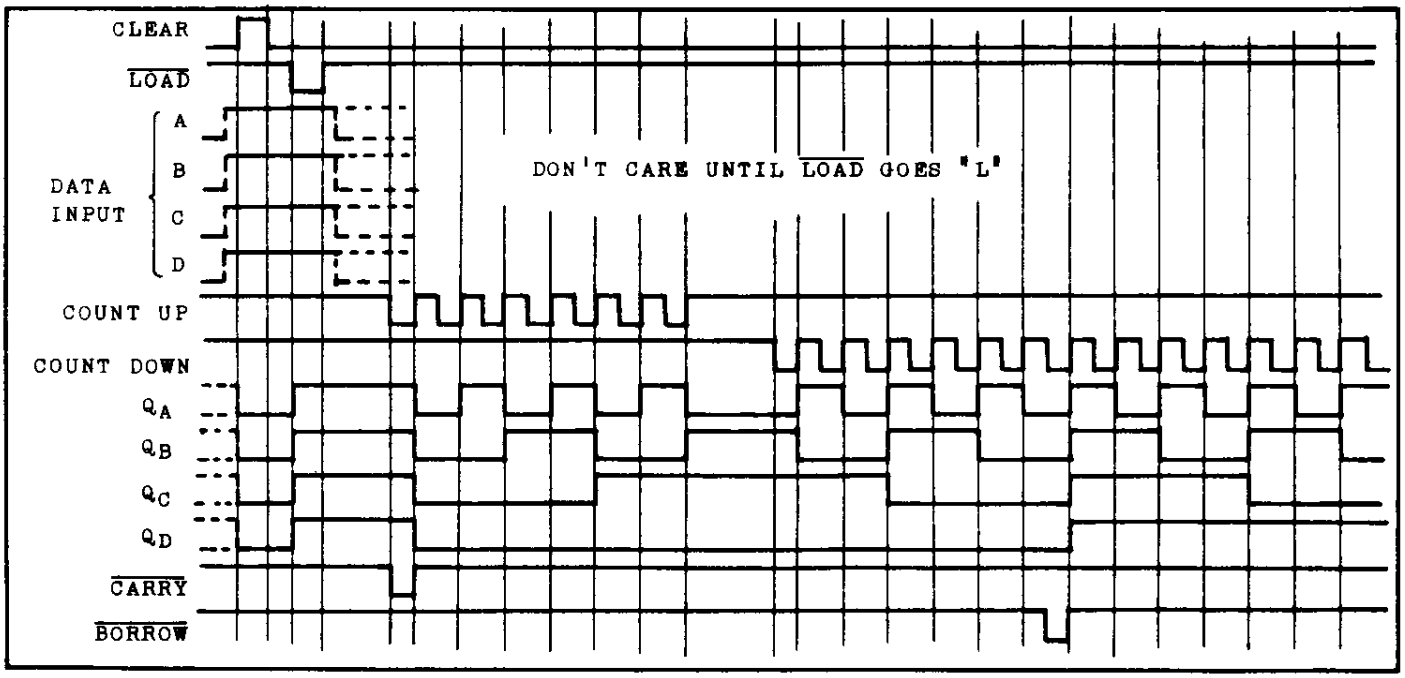


TC40H192P/F
TC40H193P/F

LOGIC DIAGRAM (TC40H193)



TIMING CHART (TC40H193)



TC40H192P/F
TC40H193P/F

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	-	2	-	8	V
Input Voltage	V_{IN}	-	0	-	V_{DD}	V
Operating Temperature	T_{opr}		-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	TYP.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Current	I_{OH}	V_{OH}=4.6V $V_{IN}=V_{SS},V_{DD}$	5	-0.52	-	-0.44	-	-	-0.36	-	mA
Low Level Output Current	I_{OL}	V_{OL}=0.4V $V_{IN}=V_{SS},V_{DD}$	5	1.4	-	1.1	-	-	0.8	-	mA
Input Voltage "H" Level	V_{IH}	$\|I_{OUT}\|$<1μA V_{OUT}=0.5V V_{OUT}=4.5V	5	4.0	-	4.0	-	-	4.0	-	V
Input Voltage "L" Level	V_{IL}		5	-	1.0	-	-	1.0	-	1.0	V
Input Current "H" Level	I_{IH}	V_{IH}=8.0V	8	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0.0V	8	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Quiescent Supply Current	I_{DD}	*$V_{IN}=V_{SS},V_{DD}$	5	-	12.5	-	0.005	12.5	-	75	μA

* All valid input combinations.

SWITCHING CHARACTERISTICS (T_a=25°C, V_{SS}=0.0V, V_{DD}=5.0V, C_L=15pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t_{or}	-	-	22	40	ns
Output Fall Time	t_{of}		-	16	30	ns
Propagation Delay Time	t_{pLH}	CLOCK - Q	-	80	135	ns
	t_{pHL}		-	55	90	ns
Propagation Delay Time	t_{pLH}, t_{pHL}	CLOCK - $\overline{\text{CARRY}}$ $\overline{\text{BORROW}}$	-	45	83	ns
	t_{pLH}, t_{pHL}	$\overline{\text{LOAD}}$ - $\overline{\text{CARRY}}$ $\overline{\text{BORROW}}$	-	90	150	ns
	t_{pLH}, t_{pHL}	LOAD - Q	-	75	135	ns
	t_{pHL}	CLEAR - Q	-	70	105	ns
	t_{pLH}, t_{pHL}	CLEAR - $\overline{\text{CARRY}}$ $\overline{\text{BORROW}}$	-	90	150	ns
Data Hold Time	t_{hold}	$\overline{\text{LOAD}}$ - DATA	-	0	10	ns
Data Setup Time	t_{setup}	$\overline{\text{LOAD}}$ - DATA	-	8	20	ns
Min. Clear Removal Time	t_{rem}	CLEAR - CLOCK	-	33	50	ns
Min. Load Removal Time	t_{rem}	$\overline{\text{LOAD}}$ - CLOCK	-	53	80	ns

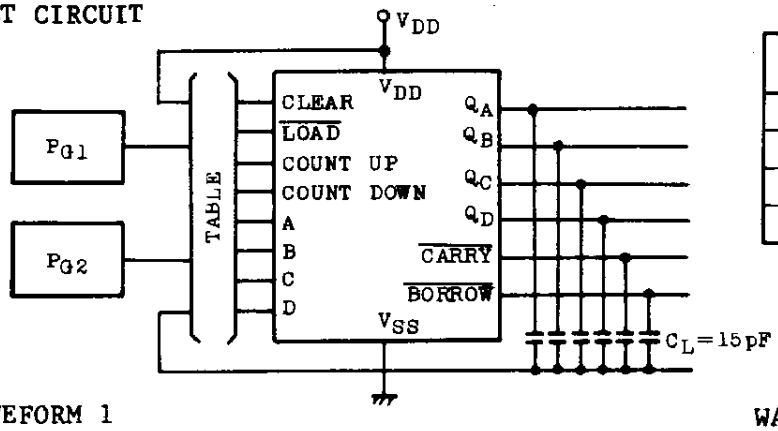
TC40H192P/F
TC40H193P/F

SWITCHING CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Min. Preset Width of Pulse	t_w	$\overline{LOAD}$	-	38	70	ns
Min. Clear Width of Pulse	t_w	CLEAR	-	30	53	ns
Max. Clock Rise Time / Fall Time	$t_{r\phi}$ / $t_{f\phi}$	-	1.0	50	-	μs
Max. Clock Frequency	f_{MAX}	-	5	10	-	MHz
Input Capacitance	C_{IN}	-	-	5	-	pF

SWITCHING TIME TEST CIRCUIT WAVEFORM

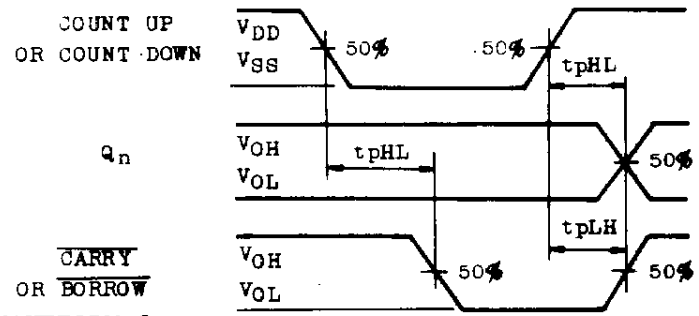
TEST CIRCUIT



TEST NO.	CLEAR	$\overline{LOAD}$	COUNT UP	COUNT DOWN	DATA n
1	L	H	P_{G1}	H	L
1	L	H	H	P_{G1}	L
2	L	P_{G1}	L	L	P_{G2}
3	P_{G1}	P_{G2}	L	L	H

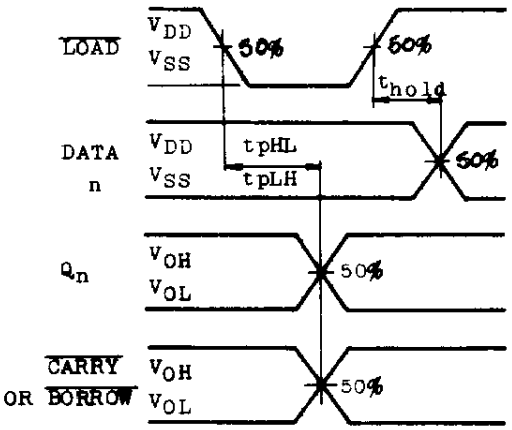
WAVEFORM 1

TEST No.1



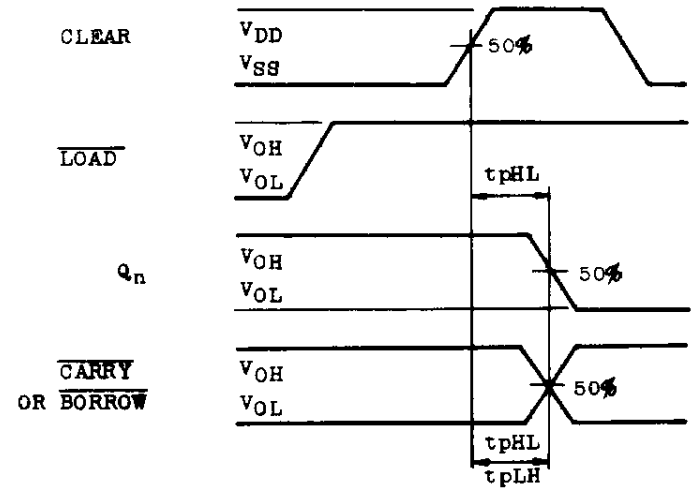
WAVEFORM 2

TEST NO.2



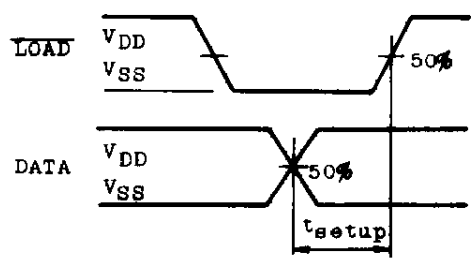
WAVEFORM 3

TEST No.3



WAVEFORM 4

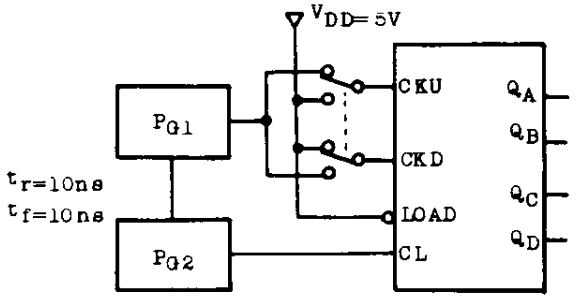
TEST No.4

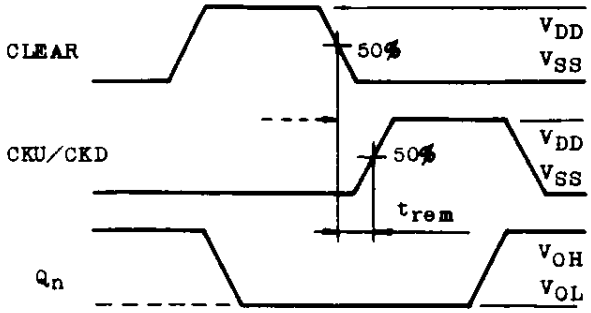


TC40H192P/F
TC40H193P/F

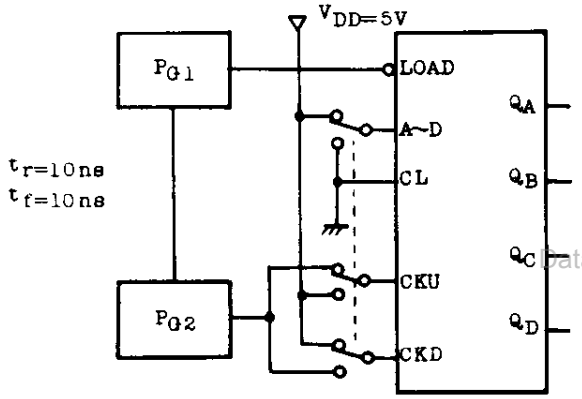
SWITCHING TIME TEST CIRCUIT & WAVEFORM

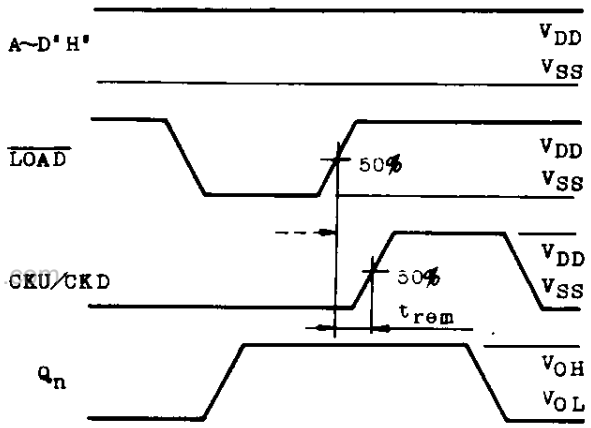
Minimum Clear Removal Time Test Circuit

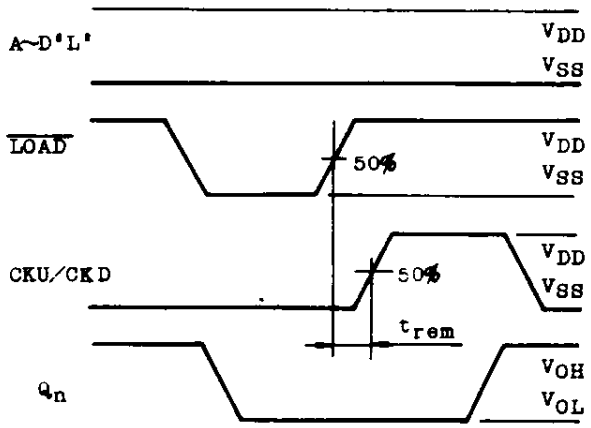




Minimum Load Removal Time Test Circuit

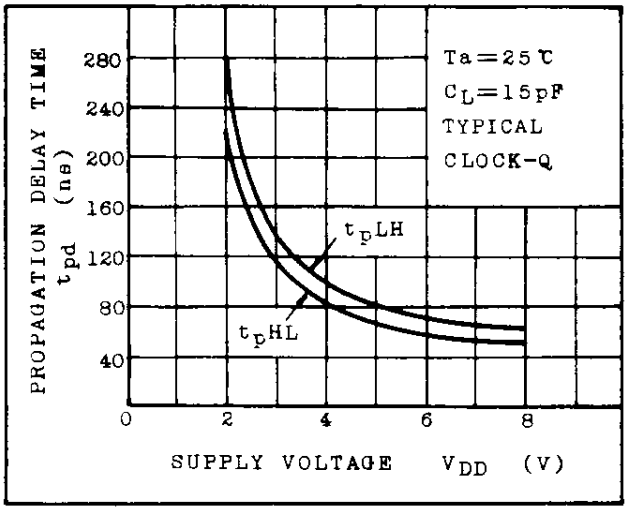




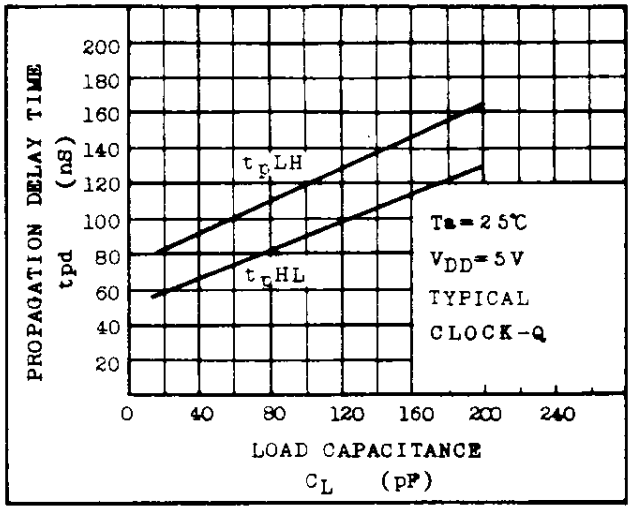


TC40H192P/F
TC40H193P/F

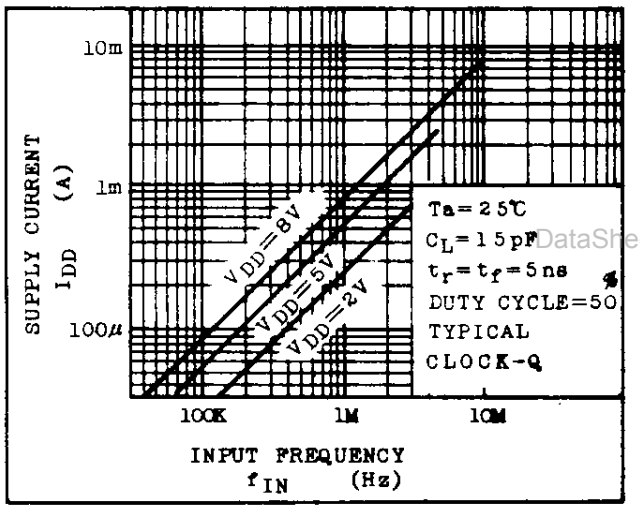
t_{pd} - V_{DD}



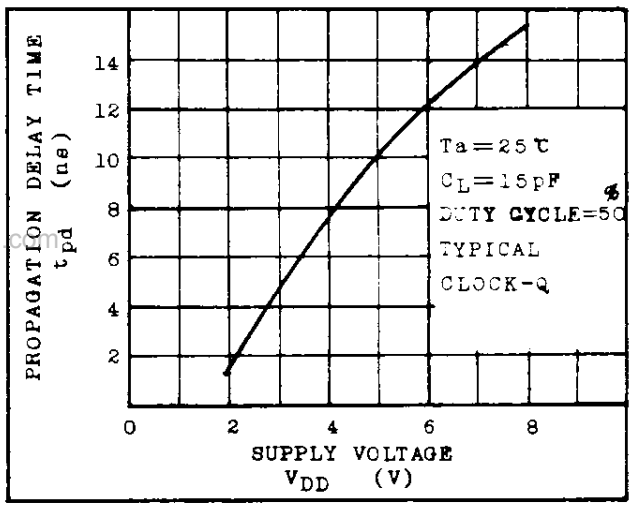
t_{pd} - C_L



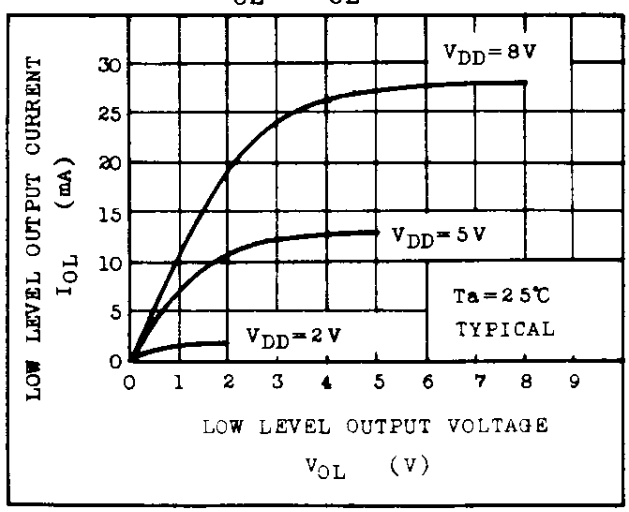
I_{DD} - f_{IN}



t_{pd} - V_{DD}



I_{OL} - V_{OL}



I_{OH} - (V_{DD} - V_{OH})