| | |
|---|---|
| $V_{Drive}$ | +15/-4V |
| $I_G$ | ±10 A |
| $R_G$ | 1 Ω |

# CGD1200HB2P-BM3

## Dual Channel Differential Isolated Gate Driver
## 1200 V BM3 SiC Half-Bridge Module Companion Tool

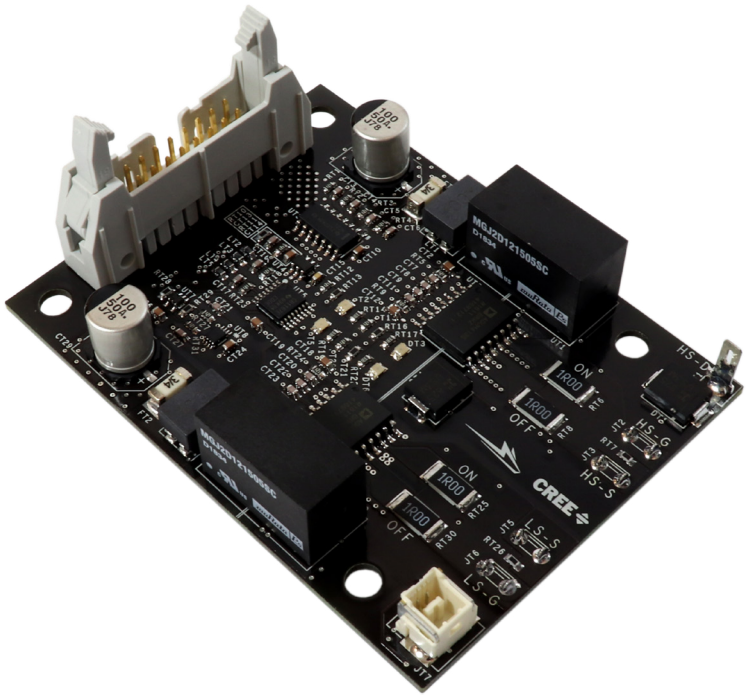
### Technical Features

- Optimized for use with Cree's High-Performance 1200 V BM3 Half-Bridge Power Modules
- High-Frequency, Ultra-Fast Switching Operation
- On-Board 2 W Isolated Power Supplies
- Primary OVLO and UVLO with Hysteresis
- On-Board Overcurrent, Shoot-Through, and Reverse Polarity Protection
- Differential Inputs for Increased Noise Immunity
- Very Low Isolation Capacitance
- Single-Ended to Differential Daughter Board Available for Purchase (CGD12HB00D)

### Applications

- DC Bus Voltages up to 1000 V

### Package



### Maximum Ratings

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DC}$ | Supply Voltage | -0.5 to 13.2 | V |
| $V_I$ | Logic Level Inputs | -0.5 to 5.5 | |
| $I_O$ | Output Peak Current ($T_A$ = 25 °C) | ±10 | A |
| $P_{Drive}$ | Output Power per Channel ($T_A$ = 25 °C) | 2 | W |
| $f_S$ | Maximum Switching Frequency (Module & MOSFET Dependent, see Power Estimate Section) | 90 | kHz |
| $T_{op}$ | Ambient Operating Temperature | -40 to +85 | °C |
| $T_{stg}$ | Storage Temperature | -40 to +125 | |

## Gate Driver Electrical Characterization

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{DC}$ | Supply Voltage | 10.2 | 12 | 13.2 | V | |
| $V_{UVLO}$ | Under Voltage Lockout | 7.7 | 8.5 | 9.3 | | Turn On, Voltage Going High |
| | UVLO Hysteresis | | 0.80 | | | |
| $V_{OVLO}$ | Over Voltage Clamping | 13.8 | 15 | 16.2 | | |
| $V_{IH}$ | High Level Logic Input Voltage | 3.5 | | 5.5 | | Single-Ended Inputs |
| $V_{IL}$ | Low Level Logic Input Voltage | 0 | | 1.5 | | |
| $V_{IDCM}$ | Differential Input Common Mode Range | -7 | - | +12 | | Differential Inputs |
| $V_{IDTH}$ | Differential Input Threshold Voltage | -200 | -125 | -50 | mV | $V_{ID} = V_{Pos-Line} – V_{Neg-Line}$ |
| $V_{OD}$ | Differential Output Magnitude | 2 | 3.1 | | V | $R_L$=100 Ω |
| $V_{GATE,HIGH}$ | High Level Output Voltage | | +15 | | | |
| $V_{GATE,LOW}$ | Low Level Output Voltage | | -4 | | | |
| $V_{IOWM}$ | Working Isolation Voltage | | 1000 | | | $V_{RMS}$ |
| $C_{ISO}$ | Isolation Capacitance | | 4.9 | | pF | Per Channel |
| CMTI | Common Mode Transient Immunity | 100 | | | kV/µs | $V_{CM}$ = 1000 V |
| $R_{GIC-ON}$ | Output Resistance [1] | | 0.48 | 0.98 | Ω | Gate Drive Buffer<br>Tested at 1 A |
| $R_{GIC-OFF}$ | Output Resistance [1] | | 0.32 | 0.63 | | |
| $R_{GEXT-ON}$ | External Turn-on Resistance [2] | | 1.0 | | | External SMD Resistor<br>2512 (6432 Metric) |
| $R_{GEXT-OFF}$ | External Turn-off Resistance [2] | | 1.0 | | | |
| $t_{ON}$ | Output Rise Time | | 174 | | ns | $R_{G-Ext}$ = 1 Ω<br>$C_{Load}$ = 47 nF<br>From 10% to 90% |
| $t_{OFF}$ | Output Fall Time | | 157 | | | |
| $t_{PHL}$ | Propagation Delay (Turn Off) | | 108 | | | $R_{G-Ext}$ = 1 Ω<br>$C_{Load}$ = 0 nF |
| $t_{PHL}$ | Propagation Delay (Turn On) | | 106 | | | |
| $t_{Blank}$ | Over-current Blanking Time | | 0.6 | | µs | $R_{G-Ext}$ = 1 Ω, $C_{Load}$ = 47 nF |
| $t_{PD-FAULT}$ | Over-current Propagation Delay to FAULT Signal Low | | 0.5 | 2 | | Does Not Include Blanking |
| $t_{ss}$ | Soft-Shutdown Time | | 3 | | | |
| $R_{SS}$ | Soft-Shutdown Resistance [3] | | 10.2 | 22 | Ω | Tested at 250 mA |
| $R_{MC}$ | Miller Clamp Resistance | | 1.1 | 2.75 | | Tested at 100 mA |
| $V_{MC}$ | Miller Clamp Voltage Threshold | -2.25 | -2.0 | -1.75 | V | Referenced to Source |

1 Output resistance of gate driver IC.
2 Additional output resistance is added with SMD resistors. Separate resistors for turn-on and turn-off allowing tunable dynamic performance.
3 Soft-Shutdown network will safely turn off the gate in the event an over-current is detected.

## Input Connector Information

| Pin Number | Parameter | Description |
|---|---|---|
| 1 | $V_{DC}$ | Power supply input pin (+12 V Nominal Input) |
| 2 | Common | Common |
| 3 | HS-P (*) | Positive line of 5 V differential high-side PWM signal pair. Terminated Into 120 Ω. |
| 4 | HS-N (*) | Negative line of 5 V differential high-side PWM signal pair. Terminated into 120 Ω. |
| 5 | LS-P (*) | Positive line of 5 V differential low-side PWM signal pair. Terminated into 120 Ω. |
| 6 | LS-N (*) | Negative line of 5 V differential low-side PWM signal pair. Terminated into 120 Ω. |
| 7 | $\overline{\text{FAULT- P}}$ (*) | Positive line of 5 V differential fault condition signal pair. Drive strength 20 mA. A low state on FAULT indicates when a de-saturation fault has occurred. The presence of a fault precludes the gate drive output from going high. |
| 8 | $\overline{\text{FAULT- N}}$ (*) | Negative line of 5 V differential fault condition signal pair. Drive strength 20 mA. |
| 9 | N/A | Unused, do not connect. |
| 10 | N/A | Unused, do not connect. |
| 11 | $\overline{\text{PS-Dis}}$ | Pull down to disable power supply. Pull up (+5 V) or leave floating to enable. Gate and source are connected with 10 kΩ when disabled. |
| 12 | Common | Common |
| 13 | PWM-EN | Pull down to disable PWM input logic. Pull up (+5 V) or leave floating to enable. Gate driver output will be held low through turn-off gate resistor if power supplies are enabled. |
| 14 | Common | Common |
| 15 | Reset | When a fault exists, bring this pin high (+5 V) to clear the fault. |
| 16 | Common | Common |

*** Inputs 3 - 10 are differential pairs.**

## Signal Descriptions

- **PWM Signals:** High-side and low-side PWM are RS-422 compatible differential inputs. The termination impedance of the differential receiver is 120 Ω. Overlap protection is provided to prevent both the high-side and low-side gates from turning on simultaneously. The overlap protection should not be used as a dead time generator.

- **FAULT Signal:** The fault signal is a RS-422 compatible differential output with a maximum drive strength of 20mA. A high signal (positive line > negative line) means there are no fault conditions for either gate driver channel. This signal will be low if an over-current fault or UVLO fault condition is detected on either channel. A red LED will indicate a fault condition. The LED, DT3, indicates a high-side fault and DT6 indicates a low-side fault.

- **UVLO Fault:** The UVLO circuit detects when the output rails of the isolated DC/DC converter fall below safe operating conditions for the gate driver. A UVLO fault indicates that the potential between the split output rails has fallen below the UVLO active level. The gate for the channel where the fault occurred will be pulled low through $R_G$ for the duration of the fault regardless of the PWM input signal. The fault will automatically clear once the potential has risen above the UVLO inactive level. There is hysteresis for this fault to ensure safe operating conditions. The UVLO faults for both channels are combined along with the over-current fault in the FAULT output signal. When there is no UVLO fault present, a green LED indicates a power good state. The LED, DT2, indicates a high-side power good status and DT5 indicates a low-side power good status.

- **Over-Current Fault:** An over-current fault is an indication of an over-current event in the SiC power module. The over-current protection circuit measures the drain-source voltage, and the fault will indicate if this voltage has risen above a level corresponding to the safe current limit. When a fault has occurred the corresponding gate driver channel will be disabled, and the gate will be pulled down through a soft-shutdown resistor, $R_{SS}$. The drain-source limit can be configured through on-board resistors. The over-current fault is latched upon detection and must be cleared by the user with a high pulse of at least 500 ns on the RESET signal.

- **PS-DIS:** The PS-DIS signal disables the output of the isolated DC/DC converters for the two channels. It is a single-ended input that must be pulled low to turn off the power supplies. With the power supplies disabled, the power module's gate will be connected to the source with a 10 kΩ resistor to prevent unwanted charge-up of the gate capacitance. This signal can be used for startup sequencing. PS-DIS is a +5 V logic-level input; connecting +12 V to the PS-DIS pin will damage the gate driver.

- **PWM-EN:** This is a single-ended input that enables the PWM inputs for both channels. When this signal is pulled down the differential receivers for both channels are disabled and the gates will both be pulled low through $R_{GEXT-OFF}$. All protection circuitry and power supplies will continue to operate including FAULT and RTD outputs. PWM-EN is a +5 V logic-level input; connecting +12 V to the PWM-EN pin will damage the gate driver.

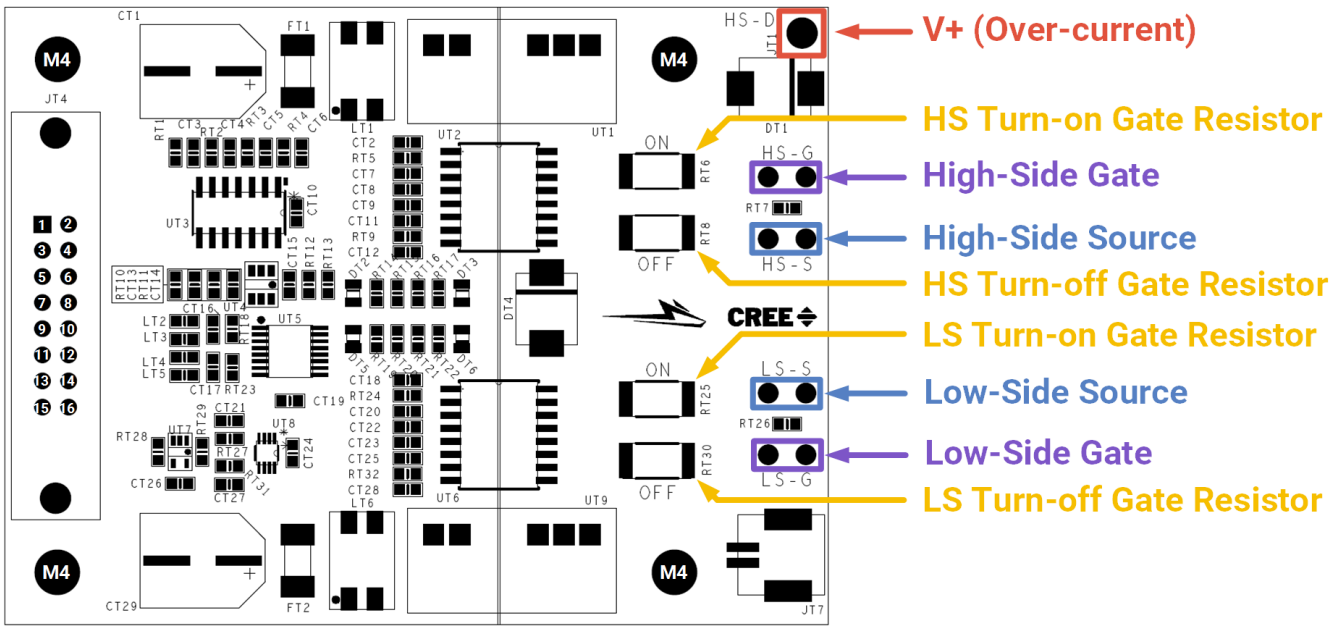
- **Over-Voltage and Reverse Polarity Protection:** Power input on pin 1 of gate driver connector features a power management IC to protect the gate driver from damage by connecting a power source that exceeds the voltage rating of the gate driver or if the current limit is exceeded. There is also a diode and MOSFET in-line with the power input to protect against connecting a power source with positive and negative polarity reversed.

## Truth Table

| PWM | $\overline{\text{PWM-EN}}$ | PS-DIS | RESET | Overcurrent/ UVLO | $\overline{\text{FAULT}}$ | Output |
|---|---|---|---|---|---|---|
| H | H or Z | H or Z | L | No | H | H |
| L | H or Z | H or Z | L | No | H | L |
| X | L | H or Z | L | No | H | L |
| X | X | L | X | No | L | Z |
| X | H or Z | H or Z | L | Yes | L | L |

**H = High | L = Low | X = Irrelevant | Z = High Impedance**

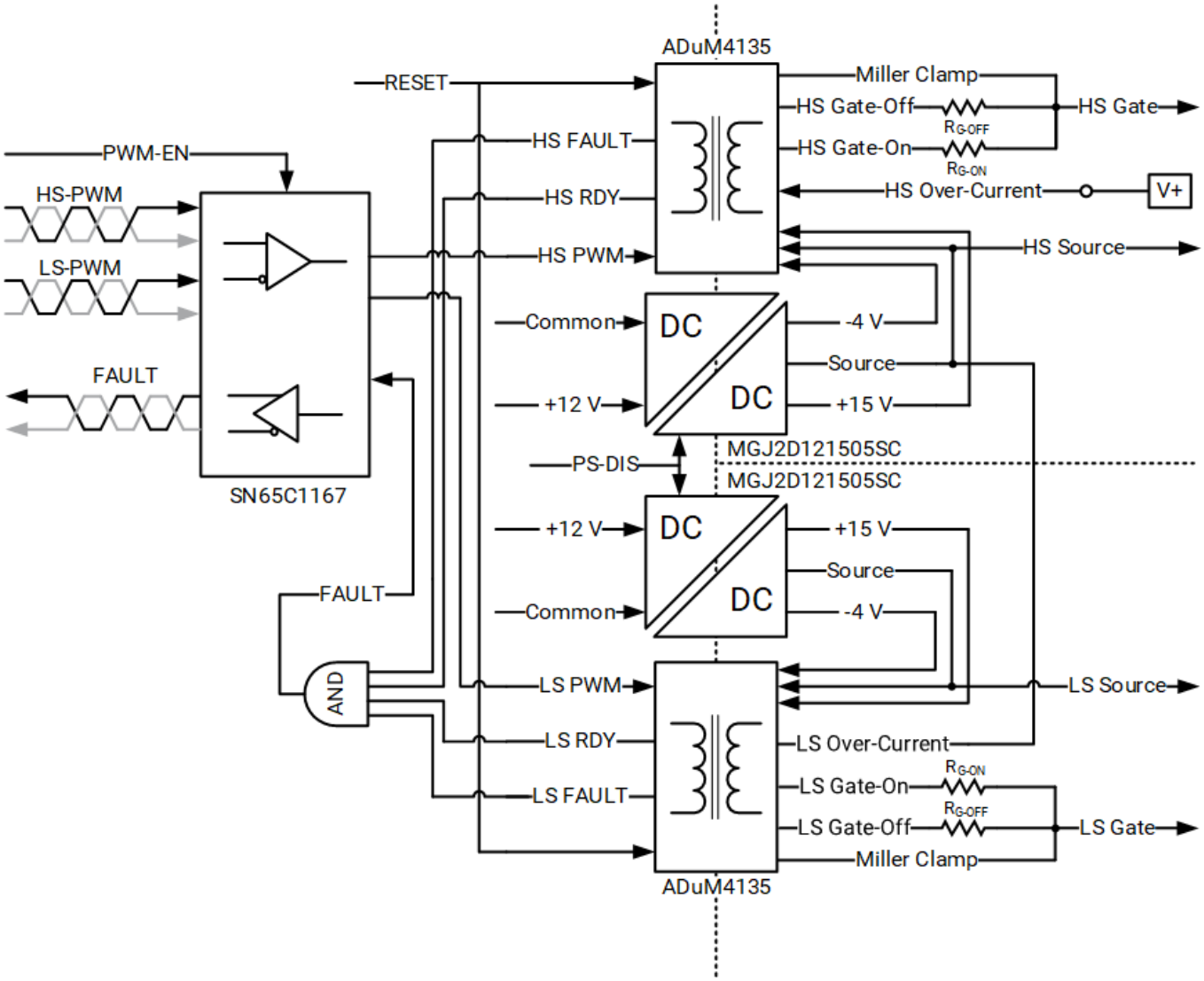
## Gate Driver Interface






Rev. -, 2020-05-10 CGD1200HB2P-BM3 4600 Silicon Dr., Durham, NC 27703

## Function Block Diagram

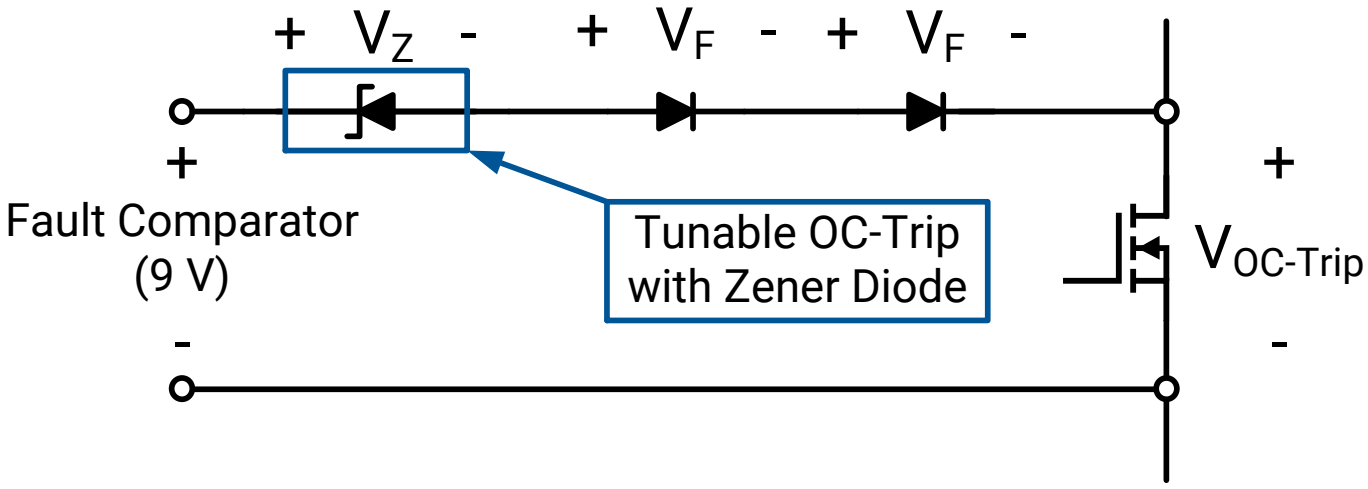


## Over-Current Trip Level

The over-current (OC) fault detection circuit measures the on-state VDS voltage across each switch position and triggers a fault condition if the voltage rises above a set level. The internal comparator trip voltage in the ADuM4135 gate driver IC is 9 V. Considering the forward voltage of the high-voltage blocking diodes and a tunable Zener diode, the over-current trip level is calculated with the following equation:

$$V_{OC\text{-}Trip} = 9V - V_Z - 2V_F$$

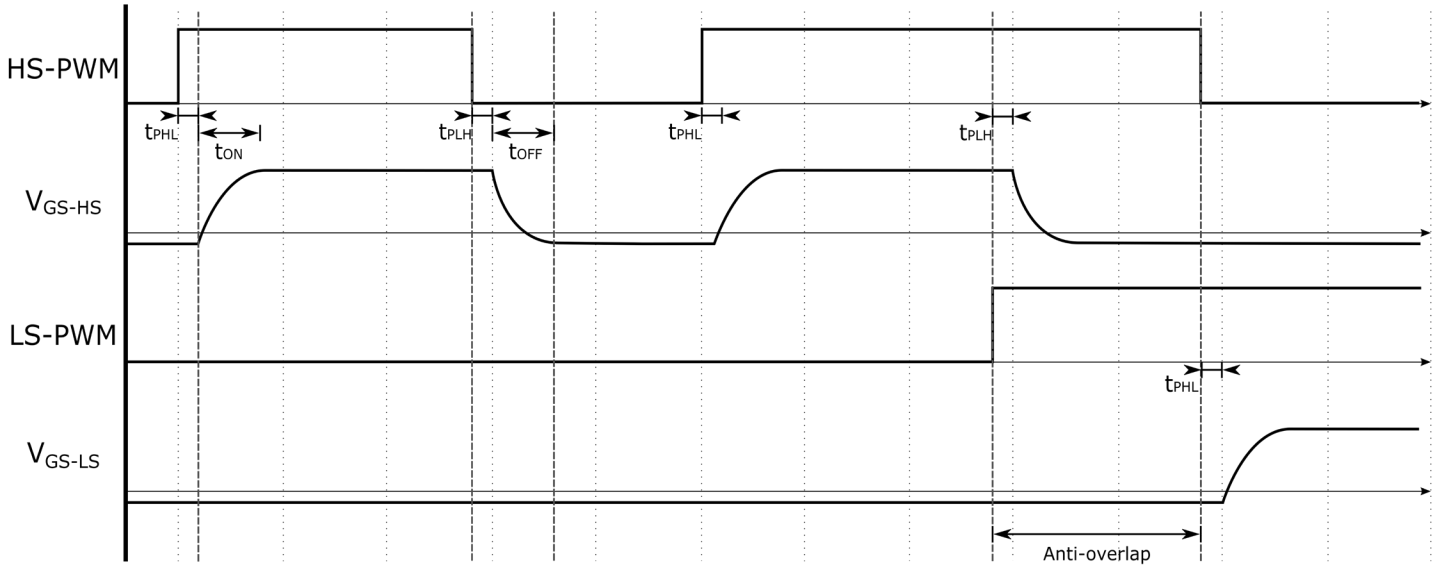
where the forward voltage of the high-voltage diodes, $V_F$, is approximately 0.5 V, and the Zener voltage, $V_Z$, included on the gate driver is 5.1 V (Nexperia® PDZ5.1BGW). As shipped, the over-current trip level is 2.9 V. If it is desired to change the over-current trip level, the Zener diode should be in a SOD123 package such as the diodes in the PDZ-GW series from Nexperia USA Inc. The Zener diodes are labelled DB2 and DB10 on the PCB.



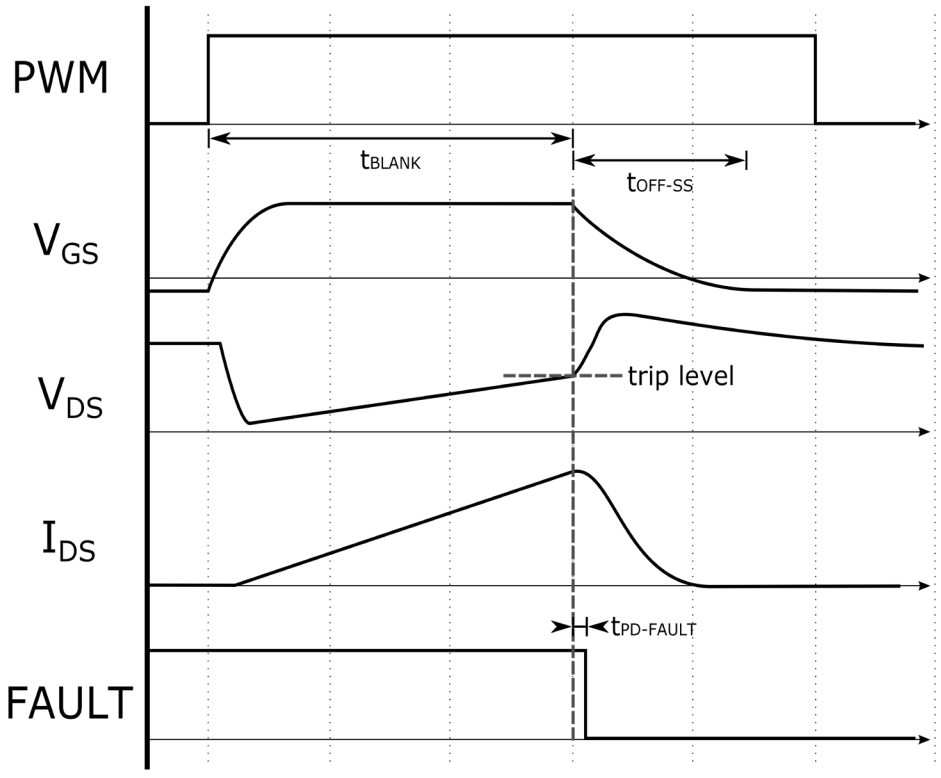

To select an appropriate over-current trip level, refer to the ID vs. VDS output characteristic curves in the module datasheet.

The HS-OC connector, JT1, cannot be left floating as the over-current fault will trip immediately when the high-side gate is actuated. If bench-top testing of the gate driver is required, it is acceptable to short the HS-OC connection to the high-side source to prevent the over-current fault from tripping. The same phenomenon exists for the low-side, and it is acceptable to short the high-side source (low-side drain) to the low-side source for bench-top testing. The over-current fault condition must be acknowledged with the Reset signal to return to normal operation of the gate driver.

## Timing Information




*Gate Timing Diagram*




*Over-Current Protection Timing Diagram*

## Input Connector Information

- 16 Positions Header, 0.100” (2.54mm) Pitch, Through Hole, Gold (SBH11-PBPC-D08-ST-BK)
- 0.110” (2.79mm) Quick Connect Male Solder Connector Non-Insulated (TE Connectivity® 735187-2)

## Suggested Mating Parts

- 16 Position Rectangular Header, IDC, Gold, 28 AWG (SFH210-PPPC-D08-ID-BK)
- 16 Position Header, 0.100” (2.54mm) Pitch, Through Hole, Gold (SFH11-PBPC-D08-RA-BK)
- 16 Position Header, 0.100” (2.54mm) Pitch, Through Hole, Right Angle, Gold (SFH11-PBPC-D08-RA-BK)

## Output Connector Information

- Quick Connect Female Connector, 0.110” (2.79mm), Non-Insulated (Keystone® 3534)

## Power Estimates

The gate driver power required is calculated using the formula below. The gate charge is dependent on the datasheets of the module being driven. Once the required gate driver power is calculated, the required input power can be calculated from the efficiency curves on the power supplies datasheet. This calculation is for one channel of the gate driver.

$$P_{sw} = Q_G * F_{SW} * \Delta V_{PS}$$

$P_{sw}$: gate driver power (per channel)
$Q_G$: total gate charge (MOSFET gate charge × number of MOSFETs per switch position)
$F_{SW}$: switching frequency
$\Delta V_{PS}$: difference in isolated power supply voltage rails ($V_{PS,HIGH}$ - $V_{PS,LOW}$)

Example:

Calculate the maximum switching frequency for WAB400M12BM3.

| | |
|---|---|
| $P_{sw}$ | 2 W (rated output power of isolated power supply on gate driver) |
| $Q_G$ | 1040 nC (provided in WAB400M12BM3 datasheet) |
| $V_{PS,HIGH}$ | 15 V (isolated power supply’s positive output voltage) |
| $V_{PS,LOW}$ | -5 V (isolated power supply’s negative output voltage) |
| $\Delta V_{PS}$ | 20 V |

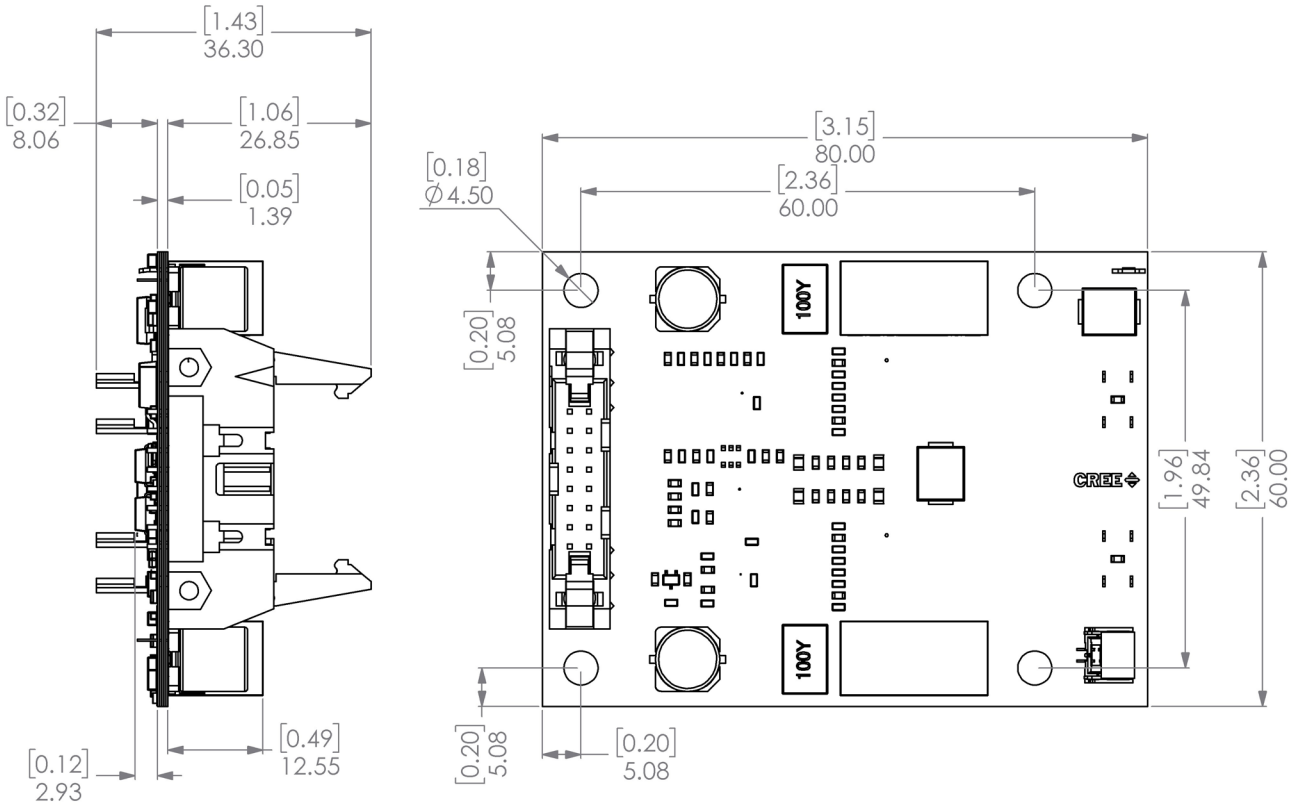
$$2\ W = 1040\ nC * F_{SW\text{-}Max} * 20\ V$$

$F_{SW\text{-}Max} \approx 90$ kHz with margin

## Supporting Links & Tools

- WAB400M12BM3: 1200 V, 400 A SiC Half-Bridge Module
- WAB300M12BM3: 1200 V, 300 A SiC Half-Bridge Module
- CGD12HB00D: Differential Transceiver Board for CGD1200HB2P-BM3
- KIT-CRD-CIL12N-BM: Dynamic Performance Evaluation Board for 62mm Modules (CPWR-AN36)
- CGD1200HB2P-BM3 Gate Driver Design Files (Schematic, PCB Artwork, and Bill of Materials)

## Dimensions ([Inches] mm)




## Important Notes

- This Cree-designed gate driver hardware for Cree components is meant to be used as an evaluation tool in a lab setting and to be handled and operated by highly qualified technicians or engineers. The hardware is not designed to meet any particular safety standards and the tool is not a production qualified assembly.
- Each part that is used in this gate driver and is manufactured by an entity other than Cree or one of Cree's affiliates is provided "as is" without warranty of any kind, including but not limited to any warranty of non-infringement, merchantability, or fitness for a particular purpose, whether express or implied. There is no representation that the operation of each such part will be uninterrupted or error free.
- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, or air traffic control systems.
- The SiC MOSFET module switches at speeds beyond what is customarily associated with IGBT-based modules. Therefore, special precautions are required to realize optimal performance. The interconnection between the gate driver and module housing needs to be as short as possible. This will afford optimal switching time and avoid the potential for device oscillation. Also, great care is required to insure minimum inductance between the module and DC link capacitors to avoid excessive VDS overshoot.