

## DUAL OPERATIONAL AMPLIFIER—YD4558

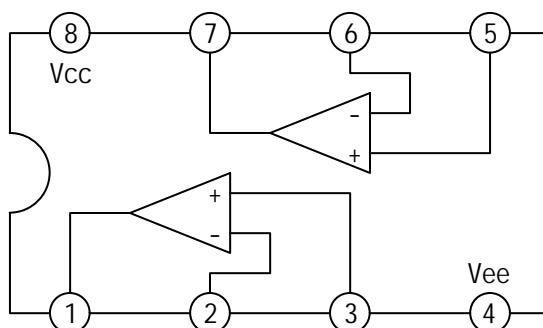
### DESCRIPTION

The YD4558 is a monolithic integrated circuit designed for dual operational amplifier.

### FEATURES

- \*NO frequency compensation required
- \*NO latch-up
- \*Large common mode and differential voltage range
- \*Parameter tracking cover temperature range
- \*Gain and phase match between amplifiers
- \*Internally frequency compensated
- \*Low noise input transistors ( $V_{in}=2.5 \mu V$ )

### BLOCK DIAGRAM



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**ABSOLUTE MAXIMUM RATINGS** (Tamb=25 )

| PARAMETER                  |      | SYMBOL               | VALUE      | UNIT |
|----------------------------|------|----------------------|------------|------|
| Supply Voltage             |      | V <sub>CC</sub>      | ± 18       | V    |
| Differential Input Voltage |      | V <sub>I(DIFF)</sub> | ± 30       | V    |
| Power Dissipation          | DIP8 | P <sub>D</sub>       | 500        | mW   |
|                            | SOP8 |                      | 250        |      |
| D terminal Output Voltage  |      | V <sub>I</sub>       | ± 15       | V    |
| Operating Temperature      |      | T <sub>opr</sub>     | -20 ~ +75  |      |
| Storage Temperature        |      | T <sub>stg</sub>     | -40 ~ +125 |      |

**ELECTRICAL CHARACTERISTICS**(V<sub>CC</sub>=15V, V<sub>EE</sub>=-15V, Tamb=25 , Unless otherwise specified)

| PARAMETER                       | SYMBOL              | TEST CONDITION   | MIN  | TYP  | MAX  | UNIT |
|---------------------------------|---------------------|--|------|------|------|------|
| Supply Current                  | I <sub>CC</sub>     |  |      | 4.0  | 6.0  | mA   |
| Input Offset Voltage            | V <sub>IO</sub>     | R <sub>s</sub> < 10k   |      | 0.5  | 6    | mV   |
| Input Offset Current            | I <sub>IO</sub>     |  |      | 5    | 200  | nA   |
| Input Bias Current              | I <sub>BIAS</sub>   |  |      | 25   | 500  | nA   |
| Large Signal Voltage Gain       | A <sub>VO</sub>     | V <sub>o(p-p)</sub> =10V,<br>R <sub>L</sub> < 2k                     | 86   | 100  |      | dB   |
| Common Mode Input Voltage Range | V <sub>ICM</sub>    |  | ± 12 | ± 14 |      | V    |
| Common Mode Rejection Ratio     | K <sub>CMR</sub>    | R <sub>s</sub> < 10k   | 70   | 90   |      | dB   |
| Supply Voltage Rejection Ratio  | K <sub>SVR</sub>    | R <sub>s</sub> < 10k   | 76.5 | 90   |      | dB   |
| Output Voltage Swing            | V <sub>o(p-p)</sub> | R <sub>s</sub> > 10k   |      | ± 12 | ± 14 | V    |
| Slew Rate                       | SR                  | V <sub>i</sub> =20mV, R <sub>L</sub> > 2k ,<br>C <sub>L</sub> < 100p |      | 1.0  |      | V/μs |
| Rise Time                       | T <sub>RISE</sub>   | V <sub>i</sub> =20mV, R <sub>L</sub> > 2k ,<br>C <sub>L</sub> < 100p |      | 0.3  |      | μs   |
| Overshoot                       | OS                  | V <sub>i</sub> =20mV, R <sub>L</sub> > 2k ,<br>C <sub>L</sub> < 100p |      | 15   |      | %    |

OUTLINE DRAWING

