

TPS23880 Type-4 4-Pair 8-Channel PoE 2 PSE Controller with Programmable SRAM

1 Features

- IEEE 802.3bt PSE solution for PoE 2 Type 3 or Type 4 Power Over Ethernet applications
- Eight independent PSE channels
- [SRAM Programmable memory](#)
- Programmable power limiting accuracy $\pm 3\%$
- Selectable 2-pair or 4-pair port power allocations
 - 15.4 W, 30 W, 45 W, 60 W, 75 W or 90 W
- Single and dual signature PD compatibility
- Dedicated 14-bit integrating current ADC per port
 - Inherent filtering
 - Noise immune MPS for DC disconnect
 - 2% Current sensing accuracy
 - 100-ms Rolling port current averaging
- 1- or 3-Bit fast port shutdown input
- Auto-class discovery and power measurement
- *Never Fooled* 4-Point detection
- Inrush and operational foldback protection
- 425-mA and 1.25-A Selectable current limits
- Port re-mapping
- 8-Bit or 16-bit I²C communication
- Flexible processor controlled operating modes
 - Auto, semi auto and manual / diagnostic
- Per Port voltage monitoring and telemetry
- -40°C to $+125^{\circ}\text{C}$ Temperature operation

2 Applications

- [Video recorder \(NVR, DVR, and so forth\)](#)
- [Small business switch](#)
- [Campus and branch switches](#)

3 Description

The TPS23880 is an 8-channel power sourcing equipment (PSE) controller engineered to insert power onto Ethernet cables in accordance with the IEEE 802.3bt standard. The eight individual power channels can be configured in any combination of 2-Pair (1-channel) or 4-Pair (2-channels) PoE Ports. The PSE controller can detect powered devices (PDs) that have a valid signature, complete mutual identification, and apply power.

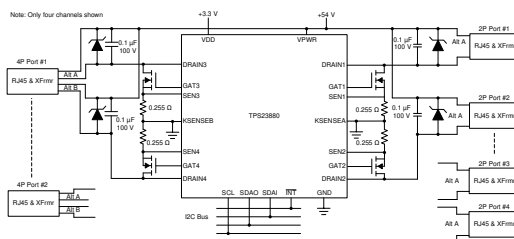
Programmable SRAM enables in-field firmware upgradability over I²C to ensure IEEE compliance and interoperability with the latest PoE enabled devices. Dedicated per port ADCs provide continuous port current monitoring and the ability to perform parallel classification measurements for faster port turn on times. A $\pm 3\%$ accurate programmable port power limit provides the ability to expand the maximum power sourced above 90 W without exceeding 100 W while also making system level power management control more easy to implement and reliable. The Fast Shutdown (OSS) input provides up to eight levels of per port shutdown priority for applications requiring immediate disabling of multiple ports. The 255-m Ω current sense resistor and external FET architecture allow designs to balance size, efficiency, thermal and solution cost requirements.

Port remapping and pin-to-pin compatibility with the TPS2388, TPS23881, and TPS23882 devices eases migration from previous generation PSE designs and enables interchangeable 2-layer PCB designs to accommodate different system PoE power configurations.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|-----------|-------------------|
| TPS23880 | VQFN (56) | 8.00 mm × 8.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

Table of Contents

| | | | |
|--|----|--|-----|
| 1 Features | 1 | 9.4 Device Functional Modes..... | 31 |
| 2 Applications | 1 | 9.5 I ² C Programming..... | 33 |
| 3 Description | 1 | 9.6 Register Maps..... | 36 |
| 4 Revision History | 2 | 10 Application and Implementation | 116 |
| 5 Device Comparison Table | 3 | 10.1 Application Information..... | 116 |
| 6 Pin Configuration and Functions | 4 | 10.2 Typical Application..... | 118 |
| Pin Functions..... | 5 | 11 Power Supply Recommendations | 127 |
| 6.1 Detailed Pin Description..... | 5 | 11.1 VDD..... | 127 |
| 7 Specifications | 7 | 11.2 VPWR..... | 127 |
| 7.1 Absolute Maximum Ratings..... | 7 | 12 Layout | 128 |
| 7.2 ESD Ratings..... | 7 | 12.1 Layout Guidelines..... | 128 |
| 7.3 Recommended Operating Conditions..... | 7 | 12.2 Layout Example..... | 129 |
| 7.4 Thermal Information..... | 7 | 13 Device and Documentation Support | 130 |
| 7.5 Electrical Characteristics..... | 8 | 13.1 Documentation Support..... | 130 |
| 7.6 Typical Characteristics..... | 15 | 13.2 Receiving Notification of Documentation Updates..... | 130 |
| 8 Parameter Measurement Information | 20 | 13.3 Support Resources..... | 130 |
| 8.1 Timing Diagrams..... | 20 | 13.4 Trademarks..... | 130 |
| 9 Detailed Description | 24 | 13.5 Electrostatic Discharge Caution..... | 130 |
| 9.1 Overview..... | 24 | 13.6 Glossary..... | 130 |
| 9.2 Functional Block Diagram..... | 28 | 14 Mechanical, Packaging, and Orderable Information | 130 |
| 9.3 Feature Description..... | 29 | | |

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| | |
|---|-------------|
| Changes from Revision F (May 2020) to Revision G (August 2020) | Page |
| • Updated the numbering format for tables, figures and cross-references throughout the document..... | 1 |
| Changes from Revision E (December 2019) to Revision F (May 2020) | Page |
| • Deleted Autonomous operation description throughout data sheet for clarification | 4 |
| • Changed Gate 1-8 voltage MAX value from 12 to 13 V in the Abs Max Ratings table | 7 |
| Changes from Revision D (October 2019) to Revision E (December 2019) | Page |
| • Fixed typo in device number on first page | 1 |
| Changes from Revision C (July 2019) to Revision D (October 2019) | Page |
| • Added TPS23882 to the Device Comparison Table | 3 |
| Changes from Revision B (October 2018) to Revision C (July 2019) | Page |
| • Changed the MOSFET drawing in the application schematics | 118 |
| Changes from Revision A (May 2018) to Revision B (September 2018) | Page |
| • Changed from Advance Information to Production Data | 1 |
| Changes from Revision * (March 2018) to Revision A (May 2019) | Page |
| • First Public Release..... | 1 |

5 Device Comparison Table

| KEY FEATURES | TPS23880 | TPS23881 | TPS23882 |
|---|---|---|----------------------------------|
| Compatible with TI's <i>FirmPSE</i> system firmware | N/A | Yes | Yes |
| Pin to Pin compatible | Yes | Yes | Yes |
| Number of PSE Channels | 8 | 8 | 8 |
| Supported IEEE 802.3 PSE Types | PoE 2 802.3bt Type 3 or 4 (2 or 4 Pair) | PoE 2 802.3bt Type 3 or 4 (2 or 4 Pair) | PoE 2 802.3bt Type 3 (2-Pair) |
| R _{SENSE} | 0.255 Ω | 0.200 Ω | 0.200 Ω |
| 2-Pair P _{CUT} programable ranges | 0.5 W to 54 W | 2 W to 65 W | 2 W to 65 W |
| 4-Pair P _{CUT} programable ranges | 0.5 W to 108 W | 4 W to 127 W | N/A |
| 90+ W 4-pair P _{CUT} accuracy | ±3.0 % | ±2.5 % | N/A |
| Channel capacitance measurement range | N/A | 1 μF to 12 μF | 1 μF to 12 μF |
| ULA Packaging | No | Yes (TPS23881A) | N/A |
| I ² C Programmable SRAM Memory | 16 kB | 16 kB | 16 kB |

6 Pin Configuration and Functions

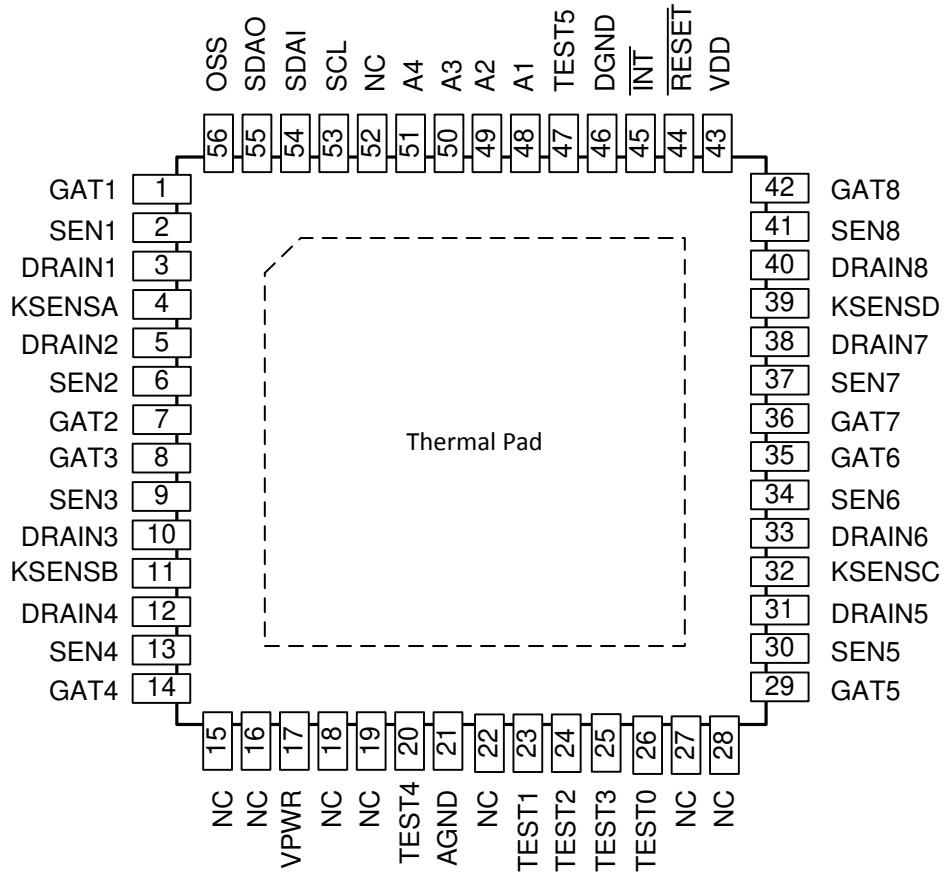


Figure 6-1. RTQ Package With Exposed Thermal Pad 56-Pin VQFN Top View

Pin Functions

| PIN | | I/O | DESCRIPTION |
|-------------|------------------------------|-----|--|
| NAME | NO. | | |
| A1-4 | 48–51 | I | I ² C A1-A4 address lines. These pins are internally pulled up to VDD. |
| AGND | 21 | — | Analog ground. Connect to GND plane and exposed thermal pad. |
| DGND | 46 | — | Digital ground. Connect to GND plane and exposed thermal pad. |
| DRAIN1-8 | 3, 5, 10, 12, 31, 33, 38, 40 | I | Channel 1-8 output voltage monitor. |
| GAT1-8 | 1, 7, 8, 14, 29, 35, 36, 42 | O | Channel 1-8 gate drive output. |
| INT | 45 | O | Interrupt output. This pin asserts low when a bit in the interrupt register is asserted. This output is open-drain. |
| KSENSA/B | 4, 11 | I | Kelvin point connection for SEN1-4 |
| KSENSC/D | 32, 39 | I | Kelvin point connection for SEN5-8 |
| NC | 15, 16, 18, 19 | O | No connect pins. These pins are internally biased at 1/3 and 2/3 of VPWR in order to control the voltage gradient from VPWR. Leave open. |
| | 22, 27, 28, 52 | — | No connect pin. Leave open. |
| OSS | 56 | I | Channel 1-8 fast shutdown. This pin is internally pulled down to DGND. |
| RESET | 44 | I | Reset input. When asserted low, the TPS23880 is reset. This pin is internally pulled up to VDD. |
| SCL | 53 | I | Serial clock input for I ² C bus. |
| SDAI | 54 | I | Serial data input for I ² C bus. This pin can be connected to SDAO for non-isolated systems. |
| SDAO | 55 | O | Serial data output for I ² C bus. This pin can be connected to SDAI for non-isolated systems. This output is open-drain. |
| SEN1-8 | 2, 6, 9, 13, 30, 34, 37, 41 | I | Channel 1-8 current sense input. |
| TEST0-5 | 20, 23, 24, 25, 26, 47 | I/O | Used internally for test purposes only. Leave open. |
| Thermal pad | — | — | The DGND and AGND terminals must be connected to the exposed thermal pad for proper operation. |
| VDD | 43 | — | Digital supply. Bypass with 0.1 μ F to DGND pin. |
| VPWR | 17 | — | Analog 54-V positive supply. Bypass with 0.1 μ F to AGND pin. |

6.1 Detailed Pin Description

The following descriptions refer to the pinout and the functional block diagram.

DRAIN1-DRAIN8: Channels 1-8 output voltage monitor and detect sense. Used to measure the port output voltage, for port voltage monitoring, port power good detection and foldback action. Detection probe currents also flow into this pin.

The TPS23880 uses an innovative 4-point technique to provide reliable PD detection and avoids powering an invalid load. The discovery is performed by sinking two different current levels via the DRAIN_n pin, while the PD voltage is measured from VPWR to DRAIN_n. If prior to starting a new detection cycle the port voltage is >2.5 V, an internal 100-k Ω resistor is connected in parallel with the port and a 400-ms detect backoff period is applied to allow the port capacitor to be discharged before the detection cycle starts.

There is an internal resistor between each DRAIN_n pin and VPWR in any operating mode except during detection or while the port is ON. If the port n is not used, DRAIN_n can be left floating or tied to GND.

GAT1-GAT8: Channels 1-8 gate drive outputs are used for external N-channel MOSFET gate control. At port turn on, it is driven positive by a low current source to turn the MOSFET on. GAT_n is pulled low whenever any of the input supplies are low or if an overcurrent timeout has occurred. GAT_n is also pulled low if the port is turned off by use of manual shutdown inputs. Leave floating if unused.

For improved design robustness, the current foldback functions limit the power dissipation of the MOSFET during low resistance load or short-circuit events and during the inrush period at port turn on. There is also fast overload protection comparator for major faults like a direct short that forces the MOSFET to turn off in less than a microsecond.

While a port is on and its P_{CUT} threshold is exceeded, a timer starts. During that time, linear current limiting ensures the current does not exceed I_{LIM} combined with current foldback action. When the timer reaches the $t_{OVL D}$ (or t_{START} if at port turn on) limit, the port shuts off. When the port current goes below P_{CUT} , the counter counts down at a rate $1/16^{th}$ of the increment rate and the counter must reach a count of 0 before the port can be turned on again.

The circuit leakage paths between the $GATn$ pin and any nearby $DRAINn$ pin, GND or Kelvin point connection must be minimized (< 250 nA), to ensure correct MOSFET control.

INT: This interrupt output pin asserts low when a bit in the interrupt register is asserted. This output is open-drain.

KSENSA, KSENSB, KSENSC, KSENSD: Kelvin point connection used to perform a differential voltage measurement across the associated current sense resistors.

Each KSENS is shared between two neighbor SEN pins as following: KSENSA with SEN1 and SEN2, KSENSB with SEN3 and SEN4, KSENSC with SEN5 and SEN6, KSENSD with SEN7 and SEN8. To optimize the measurement accuracy, ensure proper PCB layout practices are followed.

OSS: Fast shutdown, active high. This pin is internally pulled down to DGND, with an internal 1- μ s to 5- μ s deglitch filter.

The turn off procedure is similar to a port reset using Reset command (1Ah register). The 3-bit OSS function allows for a series of pulses on the OSS pin to turn off individual or multiple ports with up to 8 levels of priority.

RESET: Reset input, active low. When asserted, the TPS23880 resets, turning off all ports and forcing the registers to their power-up state. This pin is internally pulled up to VDD, with internal 1- μ s to 5- μ s deglitch filter. The designer can use an external RC network to delay the turn-on. There is also an internal power-on-reset which is independent of the \overline{RESET} input.

SCL: Serial clock input for I²C bus.

SDAI: Serial data input for I²C bus. This pin can be connected to SDAO for non-isolated systems.

SDAO: Open-drain I²C bus output data line. Requires an external resistive pull-up. The TPS23880 uses separate SDAO and SDAI lines to allow optoisolated I²C interface. SDAO can be connected to SDAI for non-isolated systems.

A4-A1: I²C bus address inputs. These pins are internally pulled up to VDD. See [Section 9.6.2.13](#) for more details.

SEN1-8: Channel current sense input relative to KSENSn (see KSENSn description). A differential measurement is performed using KSENSA-D Kelvin point connection. Monitors the external MOSFET current by use of a 0.255- Ω current sense resistor connected to GND. Used by current foldback engine and also during classification. Can be used to perform load current monitoring via ADC conversion.

When the TPS23880 performs the classification measurements, the current flows through the external MOSFETs. This avoids heat concentration in the device and makes it possible for the TPS23880 to perform classification measurements on multiple ports at the same time. For the current limit with foldback function, there is an internal 2- μ S analog filter on the SEN1-8 pins to provide glitch filtering. For measurements through an ADC, an anti-aliasing filter is present on the SEN1-8 pins. This includes the port-powered current monitoring, port policing, and DC disconnect.

If the port is not used, tie SENn to GND.

VDD: 3.3-V logic power supply input.

VPWR: High voltage power supply input. Nominally 54 V.

AGND and DGND: Ground references for internal analog and digital circuitry respectively. Not connected together internally. Both pins require a low resistance path to the system GND plane. If a robust GND plane is used to extract heat from the device's thermal pad, these pins may be connected together through the thermal pad connection on the pcb.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|---|--|------|-----|------|
| Voltage | VPWR | -0.3 | 70 | V |
| | VDD | -0.3 | 4 | V |
| | OSS, RESET, A1-A4 | -0.3 | 4 | V |
| | SDAI, SDAO, SCL, INT | -0.3 | 4 | V |
| | SEN1-8, KSENSA, KSENSB, KSENSC, KSENSD | -0.3 | 3 | V |
| | GATE1-8 | -0.3 | 13 | V |
| | DRAIN1-8 | -0.3 | 70 | V |
| | TEST0-3, ATST_DCPL0, DTST_DCPL1 | -0.3 | 4 | V |
| | AGND | -0.3 | 0.3 | V |
| Sink Current | INT, SDA | | 20 | mA |
| Lead Temperature 1/6mm from case for 10 seconds | | | 260 | °C |
| T _{stg} | Storage temperature | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | ±2000 |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | ± 500 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|-------------------|---------------------------|-----|-----|-----|------|
| V _{VDD} | | 3 | 3.3 | 3.6 | V |
| V _{VPWR} | | 44 | 54 | 57 | V |
| | Voltage Slew rate on VPWR | | | 1 | V/μs |
| f _{SCL} | SCL clock frequency | | | 400 | kHz |
| T _J | Junction temperature | -40 | | 125 | °C |

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TPS23880 | | UNIT |
|-------------------------------|--|--------------------|--|------|
| | | RTQ Package (VQFN) | | |
| | | 56 PINS | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 25.3 | | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 9.7 | | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 3.7 | | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 0.2 | | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 3.7 | | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 0.5 | | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

Conditions are $-40 < T_J < 125$ °C unless otherwise noted. $V_{VDD} = 3.3$ V, $V_{VPWR} = 54$ V, $V_{DGND} = V_{AGND}$, DGND, KSENSA, KSENSB, KSENSC and KSENSD connected to AGND, and all outputs are unloaded, $2x\text{FBn} = 0$. Positive currents are into pins. $R_S = 0.255$ Ω , to KSENSA (SEN1 or SEN2), to KSENSB (SEN3 or SEN4), to KSENSC (SEN5 or SEN6) or to KSENSD (SEN7 or SEN8). Typical values are at 25 °C. All voltages are with respect to AGND unless otherwise noted. Operating registers loaded with default values unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|--|---|-------|-------|-------|---------------|
| INPUT SUPPLY VPWR | | | | | | |
| I_{VPWR} | VPWR Current consumption | VVPWR = 54 V | | 10 | 12.5 | mA |
| V_{UVLOPW_F} | VPWR UVLO falling threshold | Check internal oscillator stops operating | 14.5 | | 17.5 | V |
| V_{UVLOPW_R} | VPWR UVLO rising threshold | | 15.5 | | 18.5 | V |
| V_{PUV_F} | VPWR Undervoltage falling threshold | VPUV threshold | 25 | 26.5 | 28 | V |
| INPUT SUPPLY VDD | | | | | | |
| I_{VDD} | VDD Current consumption | | | 6 | 12 | mA |
| V_{UVDD_F} | VDD UVLO falling threshold | For channel deassertion | 2.1 | 2.25 | 2.4 | V |
| V_{UVDD_R} | VDD UVLO rising threshold | | 2.45 | 2.6 | 2.75 | V |
| V_{UVDD_HYS} | Hysteresis VDD UVLO | | | 0.35 | | V |
| V_{UW_F} | VDD UVLO warning threshold | | 2.6 | 2.8 | 3 | V |
| A/D CONVERTERS | | | | | | |
| T_{CONV_I} | Conversion time | All ranges, each channel | 0.64 | 0.8 | 0.96 | ms |
| T_{CONV_V} | Conversion time | All ranges, each channel | 0.82 | 1.03 | 1.2 | ms |
| T_{INT_CUR} | Integration time, Current | Each channel, channel ON current | 82 | 102 | 122 | ms |
| T_{INT_DET} | Integration time, Detection | | 13.1 | 16.6 | 20 | ms |
| $T_{INT_channelV}$ | Integration time, Channel Voltage | channel powered | 3.25 | 4.12 | 4.9 | ms |
| T_{INT_inV} | Integration time, Input Voltage | | 3.25 | 4.12 | 4.9 | ms |
| | Input voltage conversion scale factor and accuracy | VVPWR = 57 V | 15175 | 15565 | 15955 | Counts |
| | | | 55.57 | 57 | 58.43 | V |
| | | VVPWR = 44 V | 11713 | 12015 | 12316 | Counts |
| | | | 42.89 | 44 | 45.10 | V |
| | Powered Channel voltage conversion scale factor and accuracy | VVPWR - VDRAINn = 57 V | 15175 | 15565 | 15955 | Counts |
| | | | 55.57 | 57 | 58.43 | V |
| | | VVPWR - VDRAINn = 44 V | 11713 | 12015 | 12316 | Counts |
| | | | 42.89 | 44 | 45.10 | V |
| $\delta V/V_{\text{Channel}}$ | Voltage reading accuracy | | -2.5 | | 2.5 | % |
| | Powered Channel current conversion scale factor and accuracy | Channel current = 770 mA | 10750 | 10970 | 11190 | Counts |
| | | | 754.5 | 770 | 785.4 | mA |
| | | Channel Current = 7.5 mA | 85 | 107 | 130 | Counts |
| | | | 5.966 | 7.5 | 9.125 | mA |
| $\delta I/I_{\text{Channel}}$ | Current reading accuracy | Channel Current = 50 mA | -3 | | 3 | % |
| | | Channel Current = 770 mA | -2 | | 2 | |
| | Powered Channel current full scale output | Channel currents = 1.15 A | 14959 | 15671 | | Counts |
| | | | 1.05 | 1.1 | | A |
| σI | Current Reading Repeatability | Full Scale reading | -7.5 | | 7.5 | mA |
| $\delta R/R_{\text{Channel}}$ | Resistance reading accuracy | $15 \text{ k}\Omega \leq R_{\text{Channel}} \leq 33 \text{ k}\Omega$, $C_{\text{Channel}} \leq 0.25 \mu\text{F}$ | -7 | | 7 | % |
| I_{bias} | Sense Pin bias current | Channel ON or during class | -2.5 | | 0 | μA |

7.5 Electrical Characteristics (continued)

Conditions are $-40 < T_J < 125$ °C unless otherwise noted. $V_{DD} = 3.3$ V, $V_{PWR} = 54$ V, $V_{DGND} = V_{AGND}$, DGND, KSENSA, KSENSB, KSENSC and KSENSD connected to AGND, and all outputs are unloaded, $2x\text{FBn} = 0$. Positive currents are into pins. $R_S = 0.255$ Ω, to KSENSA (SEN1 or SEN2), to KSENSB (SEN3 or SEN4), to KSENSC (SEN5 or SEN6) or to KSENSD (SEN7 or SEN8). Typical values are at 25 °C. All voltages are with respect to AGND unless otherwise noted. Operating registers loaded with default values unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|---|--|------|------|------|--------|
| GATE 1-8 | | | | | | |
| V_{GOH} | Gate drive voltage | V_{GATEn} , $I_{GATE} = -1$ μA | 10 | | 12.5 | V |
| I_{GO-} | Gate sinking current with Power-on Reset, OSS detected or channel turnoff command | $V_{GATEn} = 5$ V | 60 | 100 | 190 | mA |
| $I_{GO\ short-}$ | Gate sinking current with channel short-circuit | $V_{GATEn} = 5$ V, $V_{SENn} \geq V_{short}$ (or $V_{short2X}$ if 2X mode) | 60 | 100 | 190 | mA |
| I_{GO+} | Gate sourcing current | $V_{GATEn} = 0$ V, default selection | 39 | 50 | 63 | μA |
| $t_{D_off_OSS}$ | Gate turnoff time from 1-bit OSS input | From OSS to $V_{GATEn} < 1$ V, $V_{SENn} = 0$ V, MbitPrty = 0 | 1 | | 5 | μs |
| t_{OSS_OFF} | Gate turnoff time from 3-bit OSS input | From Start bit falling edge to $V_{GATEn} < 1$ V, $V_{SENn} = 0$ V, MbitPrty = 1 | 72 | | 104 | μs |
| $t_{P_off_CMD}$ | Gate turnoff time from channel turnoff command | From Channel off command to $V_{GATEn} < 1$ V, $V_{SENn} = 0$ V | | | 300 | μs |
| $t_{P_off_RST}$ | Gate turnoff time with /RESET | From /RESET low to $V_{GATEn} < 1$ V, $V_{SENn} = 0$ V | 1 | | 5 | μs |
| DRAIN 1-8 | | | | | | |
| V_{PGT} | Power-Good threshold | Measured at V_{DRAINn} | 1 | 2.13 | 3 | V |
| V_{SHT} | Shorted FET threshold | Measured at V_{DRAINn} | 4 | 6 | 8 | V |
| R_{DRAIN} | Resistance from DRAINn to VPWR | Any operating mode except during detection or while the Channel is ON, including in device RESET state | 80 | 100 | 190 | kΩ |
| AUTOCLASS | | | | | | |
| t_{Class_ACS} | Start of Autoclass Detection | Measured from the start of Class | 90 | | 100 | ms |
| t_{AUTO_PSE1} | Start of Autoclass Power Measurement | Measured from the end of Inrush | 1.4 | | 1.6 | s |
| | | Measured from setting the MACx bit while channel is already powered | | | 10 | ms |
| t_{AUTO} | Duration of Autoclass Power Measurement | | 1.7 | 1.8 | 1.9 | s |
| t_{AUTO_window} | Autoclass Power Measurement Sliding Window | | 0.15 | | 0.3 | s |
| P_{AC} | Autoclass Channel Power conversion scale factor and accuracy | $VPWR = 52$ V, $VDRAINn = 0$ V, Channel current = 770 mA | 76 | 80 | 84 | Counts |
| | | $VPWR = 50$ V, $VDRAINn = 0$ V, Channel current = 100 mA | 9 | 10 | 11 | |

7.5 Electrical Characteristics (continued)

Conditions are $-40 < T_J < 125$ °C unless otherwise noted. $V_{DD} = 3.3$ V, $V_{PWR} = 54$ V, $V_{DGND} = V_{AGND}$, DGND, KSENSA, KSENSB, KSENSC and KSENSD connected to AGND, and all outputs are unloaded, $2x_{FBn} = 0$. Positive currents are into pins. $R_S = 0.255$ Ω , to KSENSA (SEN1 or SEN2), to KSENSB (SEN3 or SEN4), to KSENSC (SEN5 or SEN6) or to KSENSD (SEN7 or SEN8). Typical values are at 25 °C. All voltages are with respect to AGND unless otherwise noted. Operating registers loaded with default values unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|--|---|------|------|------|------------|
| DETECTION | | | | | | |
| I_{DISC} | Detection current | First and 3rd detection points VVPWR - VDRAINn = 0 V | 145 | 160 | 190 | μ A |
| | | 2nd and 4th detection points VVPWR - VDRAINn = 0 V | 235 | 270 | 300 | |
| ΔI_{DISC} | 2nd – 1st detection currents | VVPWR - VDRAINn = 0 V | 98 | 110 | 118 | μ A |
| V_{det_open} | Open circuit detection voltage | Measured as VVPWR - VDRAINn | 23.5 | 26 | 29 | V |
| R_{REJ_LOW} | Rejected resistance low range | | 0.86 | | 15 | k Ω |
| R_{REJ_HI} | Rejected resistance high range | | 33 | | 100 | k Ω |
| R_{ACCEPT} | Accepted resistance range | | 19 | 25 | 26.5 | k Ω |
| R_{SHORT} | Shorted Channel threshold | | | | 360 | Ω |
| R_{OPEN} | Open Channel Threshold | | 400 | | | k Ω |
| t_{DET} | Detection Duration | Time to complete a detection, 4Pxx = 0 | 275 | 350 | 425 | ms |
| t_{CC} | Connection Check Duration | Time to complete connection check after a valid detection, 4Pxx = 1 | | 150 | 400 | ms |
| t_{DET_BOFF} | Detect backoff pause between discovery attempts | VVPWR - VDRAINn > 2.5 V | 300 | 400 | 500 | ms |
| | | VVPWR - VDRAINn < 2.5 V | 20 | | 100 | ms |
| t_{DET_DLY} | Detection delay | From command or PD attachment to Channel detection complete 4Pxx = 0 | | | 590 | ms |
| CLASSIFICATION | | | | | | |
| V_{CLASS} | Classification Voltage | VVPWR - VDRAINn, VSEn \geq 0 mV $I_{channel} \geq 180$ μ A | 15.5 | 18.5 | 20.5 | V |
| I_{CLASS_Lim} | Classification Current Limit | VVPWR - VDRAINn = 0 V | 65 | 80 | 90 | mA |
| I_{CLASS_TH} | Classification Threshold Current | Class 0-1 | 5 | | 8 | mA |
| | | Class 1-2 | 13 | | 16 | mA |
| | | Class 2-3 | 21 | | 25 | mA |
| | | Class 3-4 | 31 | | 35 | mA |
| | | Class 4-Class overcurrent | 45 | | 51 | mA |
| t_{LCE} | Classification Duration (1st Finger) | From detection complete | 95 | | 105 | ms |
| t_{CLE2-5} | Classification Duration (2nd- 5th Finger) | From Mark complete | 6.5 | | 12 | ms |
| MARK | | | | | | |
| V_{MARK} | Mark Voltage | 4 mA \geq Ichannel \geq 180 μ A VVPWR - VDRAINn | 7 | | 10 | V |
| I_{MARK_Lim} | Mark Sinking Current Limit | VVPWR - VDRAINn = 0 V | 10 | 70 | 90 | mA |
| t_{ME} | Mark Duration | | 6 | | 12 | ms |

7.5 Electrical Characteristics (continued)

Conditions are $-40 < T_J < 125$ °C unless otherwise noted. $V_{VDD} = 3.3$ V, $V_{VPWR} = 54$ V, $V_{DGND} = V_{AGND}$, DGND, KSENSA, KSENSB, KSENSC and KSENSD connected to AGND, and all outputs are unloaded, $2x\text{FBn} = 0$. Positive currents are into pins. $R_S = 0.255$ Ω, to KSENSA (SEN1 or SEN2), to KSENSB (SEN3 or SEN4), to KSENSC (SEN5 or SEN6) or to KSENSD (SEN7 or SEN8). Typical values are at 25 °C. All voltages are with respect to AGND unless otherwise noted. Operating registers loaded with default values unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------|--|--|------|--------|-------|------|
| DC DISCONNECT | | | | | | |
| V_{IMIN} | DC disconnect threshold | DCDTxx = 0 | 1.02 | 1.6575 | 2.295 | mV |
| | | DCDTxx = 1 | 0.51 | 1.1475 | 1.785 | |
| t_{MPDO} | PD Maintain Power signature dropout time limit | TMPDO = 00 | 320 | | 400 | ms |
| | | TMPDO = 01 | 75 | | 100 | |
| | | TMPDO = 10 | 150 | | 200 | |
| | | TMPDO = 11 | 600 | | 800 | |
| t_{MPS} | PD Maintain Power Signature time for validity | | 2.5 | 3 | | ms |
| PORT POWER POLICING | | | | | | |
| $\delta P_{CUT}/P_{CUT}$ | PCUT tolerance | Policing settings < 15 W | 0 | 5 | 10 | % |
| | | Policing settings \geq 15 W | 0 | 3 | 6 | |
| $t_{OVL D}$ | PCUT time limit | TOVLD = 00 | 50 | | 70 | ms |
| | | TOVLD = 01 | 25 | | 35 | |
| | | TOVLD = 10 | 100 | | 140 | |
| | | TOVLD = 11 | 200 | | 280 | |
| I_{CUT_MAX} | Internal ICUT Clamp | Measured per channel POL = 1111 1111b | 1 | 1.025 | 1.050 | A |
| PORT CURRENT INRUSH | | | | | | |
| V_{Inrush} | IInrush limit, ALTIRNn = 0 | VVPWR - VDRAINn = 1 V | 25 | 38 | 51 | mV |
| | | VVPWR - VDRAINn = 10 V | 25 | 38 | 51 | |
| | | VVPWR - VDRAINn = 15 V | 43 | 56 | 69 | |
| | | VVPWR - VDRAINn = 30 V | 102 | | 114.7 | |
| | | VVPWR - VDRAINn = 55 V | 102 | | 114.7 | |
| | IInrush limit, ALTIRNn = 1 | VVPWR - VDRAINn = 1 V | 25 | 38 | 51 | |
| | | VVPWR - VDRAINn = 10 V | 47 | 60 | 73 | |
| | | VVPWR - VDRAINn = 15 V | 69 | 82 | 95 | |
| | | VVPWR - VDRAINn = 30 V | 102 | | 114.7 | |
| | | VVPWR - VDRAINn = 55 V | 102 | | 114.7 | |
| t_{START} | Maximum current limit duration in start-up | TSTART = 00 | 50 | | 70 | ms |
| | | TSTART = 01 | 25 | | 35 | |
| | | TSTART = 10 | 100 | | 140 | |

7.5 Electrical Characteristics (continued)

Conditions are $-40 < T_J < 125$ °C unless otherwise noted. $V_{DD} = 3.3$ V, $V_{PWR} = 54$ V, $V_{DGND} = V_{AGND}$, DGND, KSENSA, KSENSB, KSENSC and KSENSD connected to AGND, and all outputs are unloaded, $2x\text{FBn} = 0$. Positive currents are into pins. $R_S = 0.255$ Ω , to KSENSA (SEN1 or SEN2), to KSENSB (SEN3 or SEN4), to KSENSC (SEN5 or SEN6) or to KSENSD (SEN7 or SEN8). Typical values are at 25 °C. All voltages are with respect to AGND unless otherwise noted. Operating registers loaded with default values unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|--|-----|-----|-------|---------------|
| PORT CURRENT FOLDBACK | | | | | | |
| V_{LIM} | ILIM 1X limit, $2x\text{FBn} = 0$ and $\text{ALTFBn} = 0$ | $\text{VDRAINn} = 1$ V | 102 | | 114.7 | mV |
| | | $\text{VDRAINn} = 15$ V | 102 | | 115 | |
| | | $\text{VDRAINn} = 30$ V | 66 | 74 | 81 | |
| | | $\text{VDRAINn} = 50$ V | 30 | 38 | 46 | |
| | ILIM 1X limit, $2x\text{FBn} = 0$ and $\text{ALTFBn} = 1$ | $\text{VDRAINn} = 1$ V | 102 | | 114.7 | |
| | | $\text{VDRAINn} = 30$ V | 99 | | 114.7 | |
| | | $\text{VDRAINn} = 40$ V | 60 | 67 | 74 | |
| | | $\text{VDRAINn} = 50$ V | 30 | 38 | 46 | |
| V_{LIM2X} | ILIM 2X limit, $2x\text{FBn} = 1$ and $\text{ALTFBn} = 0$ | $\text{VDRAINn} = 1$ V | 310 | 320 | 330 | mV |
| | | $\text{VDRAINn} = 10$ V | 200 | 220 | 240 | |
| | | $\text{VDRAINn} = 30$ V | 66 | 74 | 81 | |
| | | $\text{VDRAINn} = 50$ V | 30 | 38 | 46 | |
| | ILIM 2X limit, $2x\text{FBn} = 1$ and $\text{ALTFBn} = 1$ | $\text{VDRAINn} = 1$ V | 310 | 320 | 330 | |
| | | $\text{VDRAINn} = 20$ V | 176 | 186 | 196 | |
| | | $\text{VDRAINn} = 40$ V | 60 | 67 | 74 | |
| | | $\text{VDRAINn} = 50$ V | 30 | 38 | 46 | |
| t_{LIM} | ILIM time limit | $2x\text{FBn} = 0$ | 55 | 60 | 65 | ms |
| | | $\text{TLIM} = 00$ | 55 | 60 | 65 | |
| | $2x\text{FBn} = 1$ | $\text{TLIM} = 01$ | 15 | 16 | 17 | |
| | | $\text{TLIM} = 10$ | 10 | 11 | 12 | |
| | | $\text{TLIM} = 11$ | 6 | 6.5 | 7 | |
| SHORT CIRCUIT DETECTION | | | | | | |
| V_{short} | I_{SHORT} threshold in 1X mode and during inrush | | 234 | | 306 | mV |
| $V_{\text{short}2X}$ | I_{SHORT} threshold in 2X mode | | 357 | | 408 | |
| $t_{D_off_SEN}$ | Gate turnoff time from SENn input | $2x\text{FBn} = 0$, $\text{VDRAINn} = 1$ V From V_{SENn} pulsed to 0.425 V. | | | 0.9 | μs |
| | | $2x\text{FBn} = 1$, $\text{VDRAINn} = 1$ V From V_{SENn} pulsed to 0.62 V. | | | 0.9 | |
| CURRENT FAULT RECOVERY (BACKOFF) TIMING | | | | | | |
| t_{ed} | Error delay timing. Delay before next attempt to power a channel following power removal due to error condition | P_{CUT} , I_{LIM} or I_{Inrush} fault Semi-auto mode | 0.8 | 1 | 1.2 | s |
| δI_{fault} | Duty cycle of I_{channel} with current fault | | 5.5 | | 6.7 | % |
| THERMAL SHUTDOWN | | | | | | |
| | Shutdown temperature | Temperature rising | 135 | 146 | | °C |
| | Hysteresis | | | 7 | | °C |

7.5 Electrical Characteristics (continued)

Conditions are $-40 < T_J < 125$ °C unless otherwise noted. $V_{VDD} = 3.3$ V, $V_{VPWR} = 54$ V, $V_{DGND} = V_{AGND}$, DGND, KSENSA, KSENSB, KSENSC and KSENSD connected to AGND, and all outputs are unloaded, $2x\text{FBn} = 0$. Positive currents are into pins. $R_S = 0.255$ Ω , to KSENSA (SEN1 or SEN2), to KSENSB (SEN3 or SEN4), to KSENSC (SEN5 or SEN6) or to KSENSD (SEN7 or SEN8). Typical values are at 25 °C. All voltages are with respect to AGND unless otherwise noted. Operating registers loaded with default values unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|--|------|-----|-----|------------|
| DIGITAL I/O (SCL, SDAI, A1-A4, /RESET, OSS unless otherwise stated) | | | | | | |
| V_{IH} | Digital input High | | 2.1 | | | V |
| V_{IL} | Digital input Low | | | | 0.9 | V |
| V_{IT_HYS} | Input voltage hysteresis | | 0.17 | | | V |
| V_{OL} | Digital output Low | SDAO at 9mA | | | 0.4 | V |
| | Digital output Low | /INT at 3mA | | | 0.4 | V |
| R_{pullup} | Pullup resistor to VDD | /RESET, A1-A4, TEST0 | 30 | 50 | 80 | k Ω |
| $R_{pulldown}$ | Pulldown resistor to DGND | OSS, TEST1, TEST2 | 30 | 50 | 80 | k Ω |
| t_{FLT_INT} | Fault to /INT assertion | Time to internally register an Interrupt fault, from Channel turn off | | 50 | 500 | μ s |
| $T_{RESETmin}$ | /RESET input minimum pulse width | | | | 5 | μ s |
| T_{bit_OSS} | 3-bit OSS bit period | MbitPrty = 1 | 24 | 25 | 26 | μ s |
| t_{OSS_IDL} | Idle time between consecutive shutdown code transmission in 3-bit mode | MbitPrty = 1 | 48 | 50 | | μ s |
| t_{r_OSS} | Input rise time of OSS in 3-bit mode | 0.8 V \rightarrow 2.3 V, MbitPrty = 1 | 1 | | 300 | ns |
| t_{f_OSS} | Input fall time of OSS in 3-bit mode | 2.3 V \rightarrow 0.8 V, MbitPrty = 1 | 1 | | 300 | ns |
| I2C TIMING REQUIREMENTS | | | | | | |
| t_{POR} | Device power-on reset delay | | | | 20 | ms |
| f_{SCL} | SCL clock frequency | | 10 | | 400 | kHz |
| t_{LOW} | LOW period of the clock | | 0.5 | | | μ s |
| t_{HIGH} | HIGH period of the clock | | 0.26 | | | μ s |
| t_{fo} | SDAO output fall time | SDAO, 2.3 V \rightarrow 0.8 V, $C_b = 10$ pF, 10 k Ω pull-up to 3.3 V | 10 | | 50 | ns |
| | | SDAO, 2.3 V \rightarrow 0.8 V, $C_b = 400$ pF, 1.3 k Ω pull-up to 3.3 V | 10 | | 50 | ns |
| C_{I2C} | SCL capacitance | | | | 10 | pF |
| C_{I2C_SDA} | SDAI, SDAO capacitance | | | | 6 | pF |
| t_{SU_DATW} | Data setup tme (Write operation) | | 50 | | | ns |
| t_{HD_DATW} | Data hold time (Write operation) | | 0 | | | ns |
| t_{HD_DATR} | Data hold time (Read operation) | SDAO, VDD/2 threshold, $C_b = 10$ pF, 1.3 k Ω pull-up to 3.3 V | 150 | | 400 | ns |
| t_{f_SDA} | Input fall times of SDAI | 2.3 V \rightarrow 0.8 V | 20 | | 120 | ns |
| t_{r_SDA} | Input rise times of SDAI | 0.8 V \rightarrow 2.3 V | 20 | | 120 | ns |
| t_r | Input rise time of SCL | 0.8 V \rightarrow 2.3 V | 20 | | 120 | ns |
| t_f | Input fall time of SCL | 2.3 V \rightarrow 0.8 V | 20 | | 120 | ns |
| t_{BUF} | Bus free time between a STOP and START condition | | 0.5 | | | μ s |
| t_{HD_STA} | Hold time After (Repeated) START condition | | 0.26 | | | μ s |
| t_{SU_STA} | Repeated START condition setup time | | 0.26 | | | μ s |
| t_{SU_STO} | STOP condition setup time | | 0.26 | | | μ s |
| t_{DG} | Suppressed spike pulse width, SDAI and SCL | | 50 | | | ns |

7.5 Electrical Characteristics (continued)

Conditions are $-40 < T_J < 125$ °C unless otherwise noted. $V_{VDD} = 3.3$ V, $V_{VPWR} = 54$ V, $V_{DGND} = V_{AGND}$, DGND, KSENSA, KSENSB, KSENSC and KSENSD connected to AGND, and all outputs are unloaded, $2x\text{FBn} = 0$. Positive currents are into pins. $R_S = 0.255$ Ω , to KSENSA (SEN1 or SEN2), to KSENSB (SEN3 or SEN4), to KSENSC (SEN5 or SEN6) or to KSENSD (SEN7 or SEN8). Typical values are at 25 °C. All voltages are with respect to AGND unless otherwise noted. Operating registers loaded with default values unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|-------------------------|-----------------|-----|-----|-----|------|
| $t_{\text{WDT_I2C}}$ | I2C Watchdog trip delay | | 1.1 | 2.2 | 3.3 | sec |

7.6 Typical Characteristics

Conditions are $-40 < T_J < 125$ °C unless otherwise noted. $V_{VDD} = 3.3$ V, $V_{VPWR} = 54$ V, $V_{DGND} = V_{AGND}$, DGND, KSENSA, KSENSB, KSENSC and KSENSD connected to AGND, and all outputs are unloaded, $2x\text{FBn} = 0$. Positive currents are into pins. $R_S = 0.255$ Ω, to KSENSA (SEN1 or SEN2), to KSENSB (SEN3 or SEN4), to KSENSC (SEN5 or SEN6) or to KSENSD (SEN7 or SEN8). Typical values are at 25 °C. All voltages are with respect to AGND unless otherwise noted. Operating registers loaded with default values unless otherwise noted.

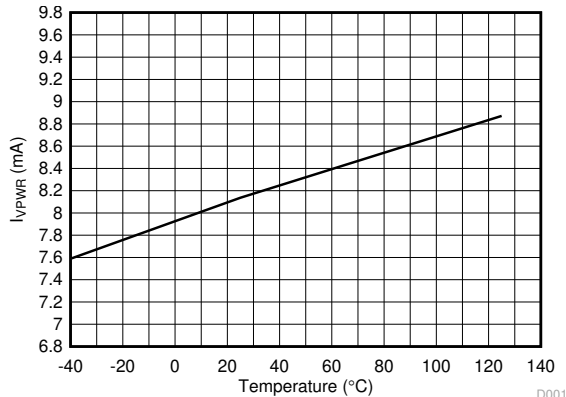


Figure 7-1. VPWR Current Consumption vs Temperature

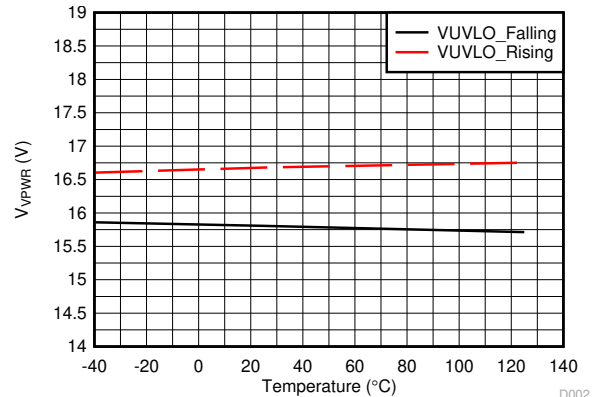


Figure 7-2. VPWR UVLO Thresholds vs Temperature

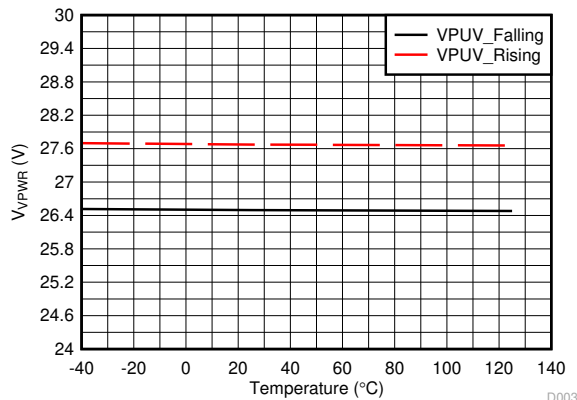


Figure 7-3. VPUV Thresholds vs Temperature

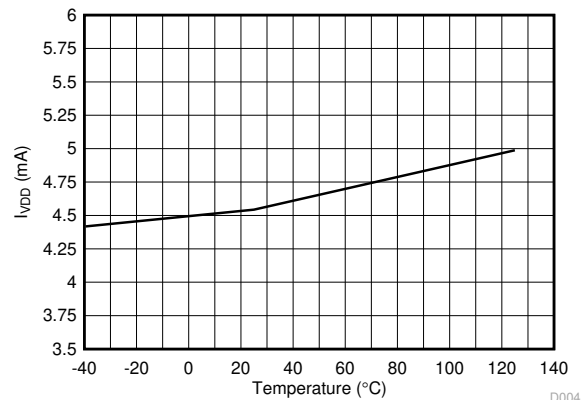


Figure 7-4. VDD Current Consumption vs Temperature

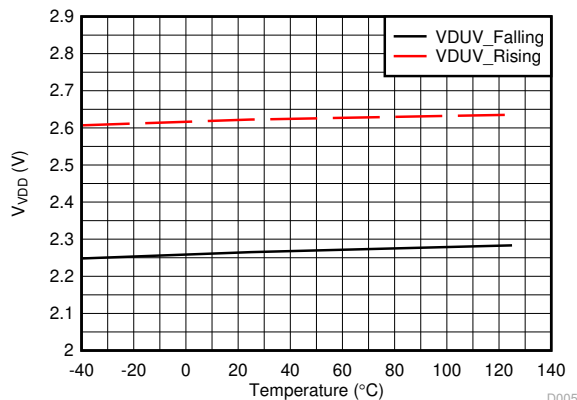


Figure 7-5. VDUV Thresholds vs Temperature

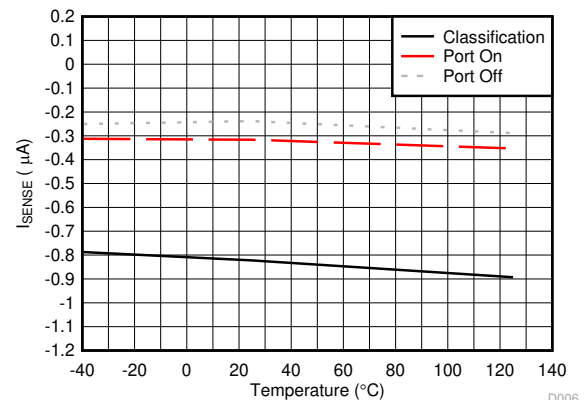


Figure 7-6. SENSE Pin Bias Current vs Temperature

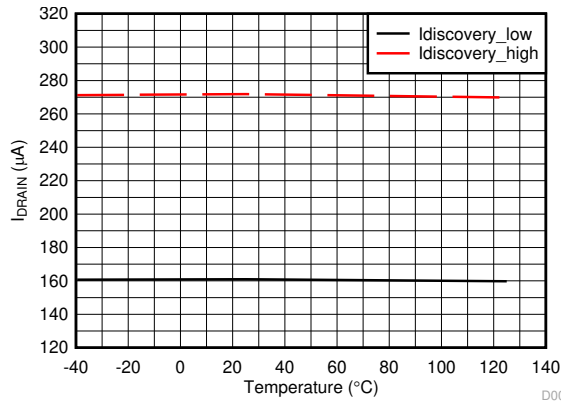


Figure 7-7. Discovery Currents vs Temperature

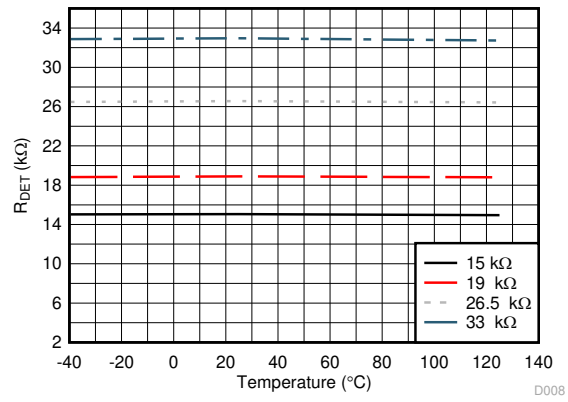


Figure 7-8. Discovery Resistance Measurement vs Temperature

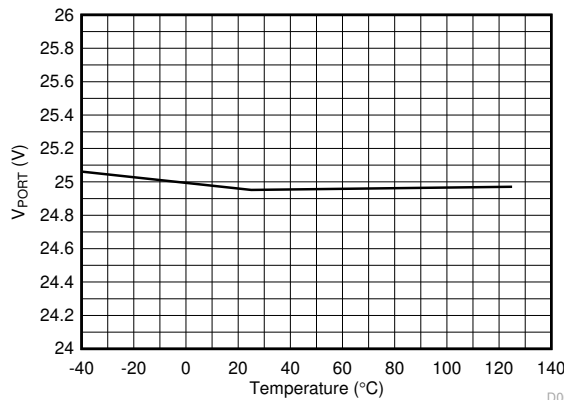


Figure 7-9. Discovery Open Circuit Voltage vs Temperature

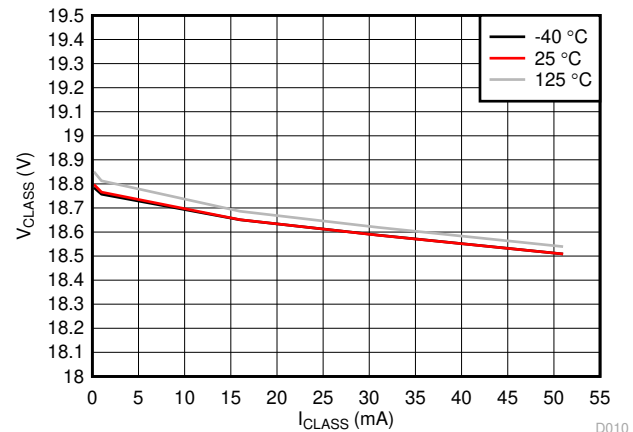


Figure 7-10. Classification Voltage vs ICLASS and Temperature

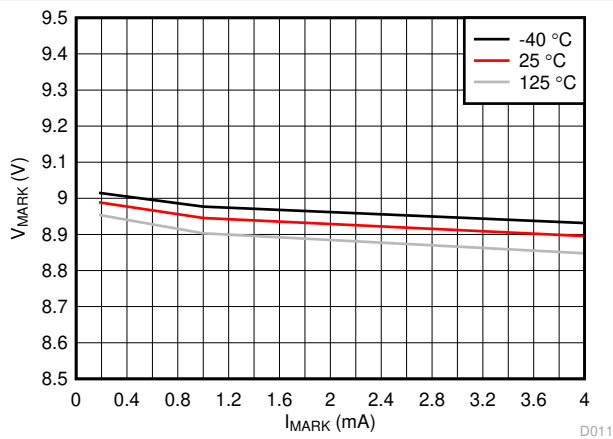


Figure 7-11. Mark Voltage vs I_{MARK} and Temperature

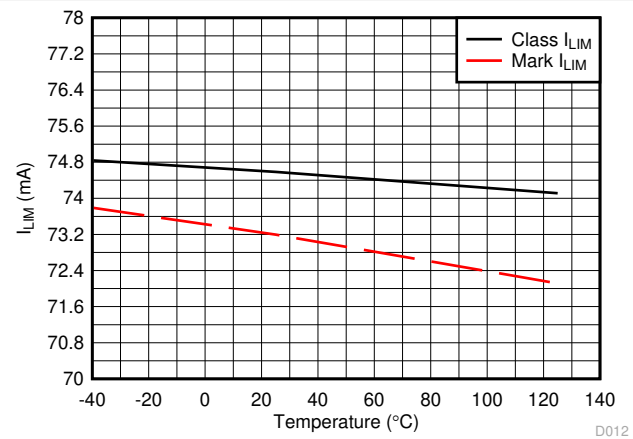


Figure 7-12. Classification and Mark Current Limit vs Temperature

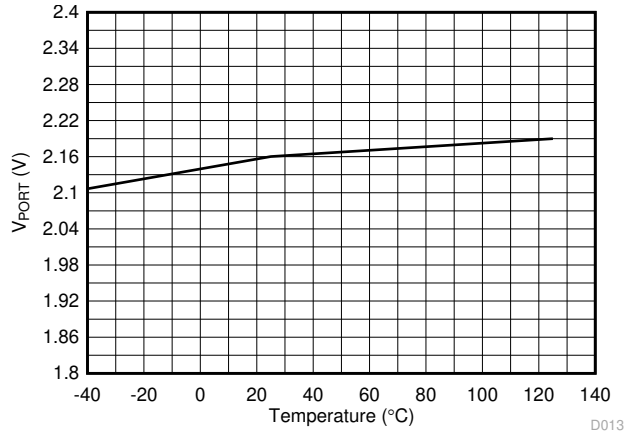


Figure 7-13. Power Good Threshold vs Temperature

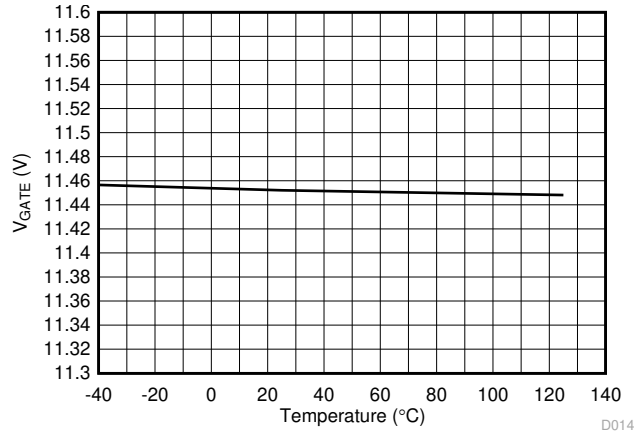


Figure 7-14. Gate Voltage (Port On) vs Temperature

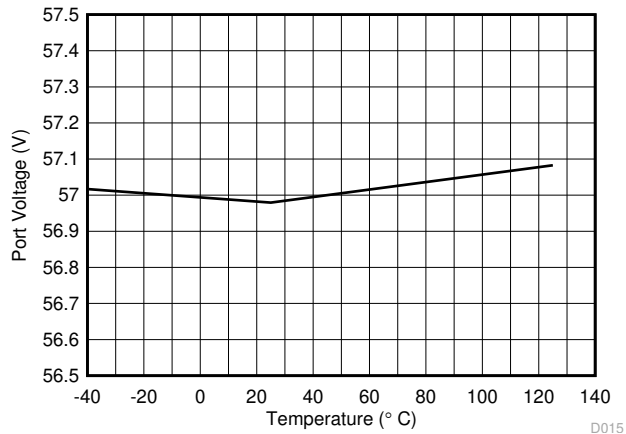


Figure 7-15. Port Voltage ADC Measurement vs Temperature

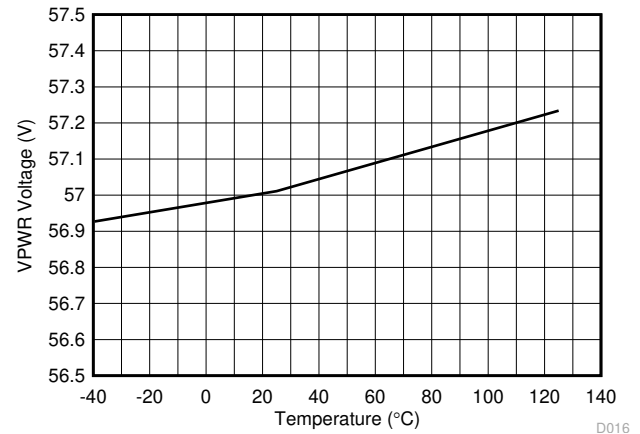


Figure 7-16. VPWR Voltage ADC Measurement vs Temperature

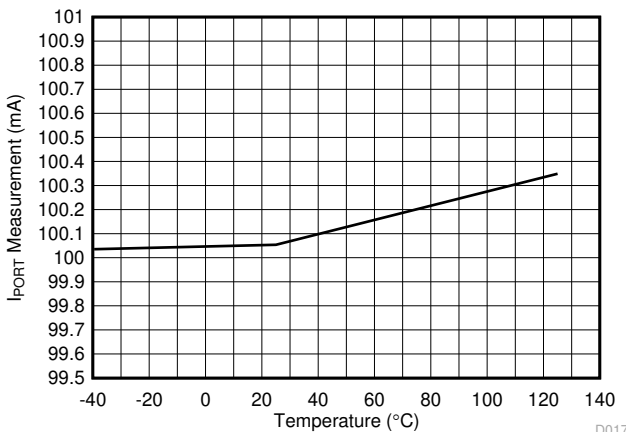


Figure 7-17. Port Current ADC Measurement (100mA) vs Temperature

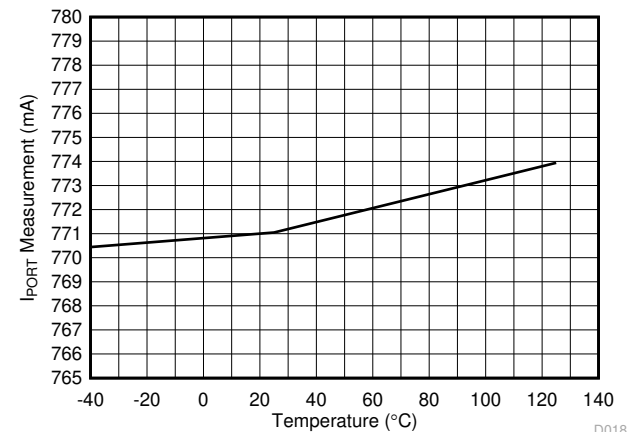


Figure 7-18. Port Current ADC Measurement (770mA) vs Temperature

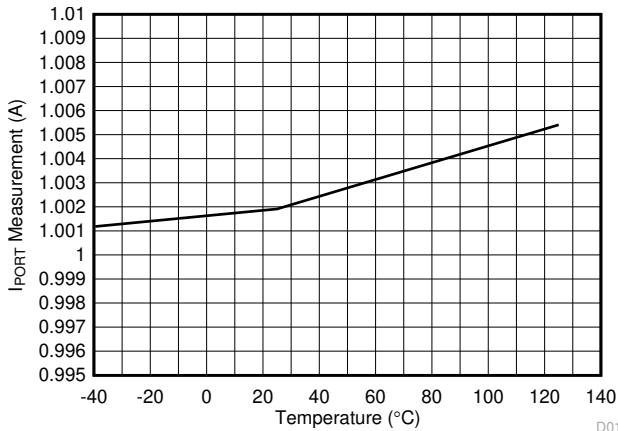


Figure 7-19. Port Current ADC Measurement (1 A) vs Temperature

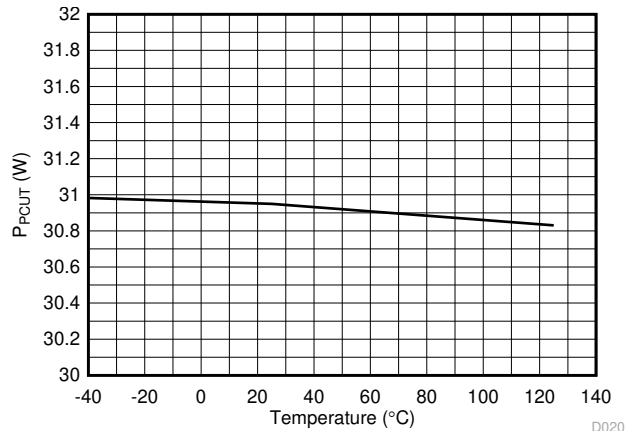


Figure 7-20. 2-Pair PCut Threshold (30W) vs Temperature

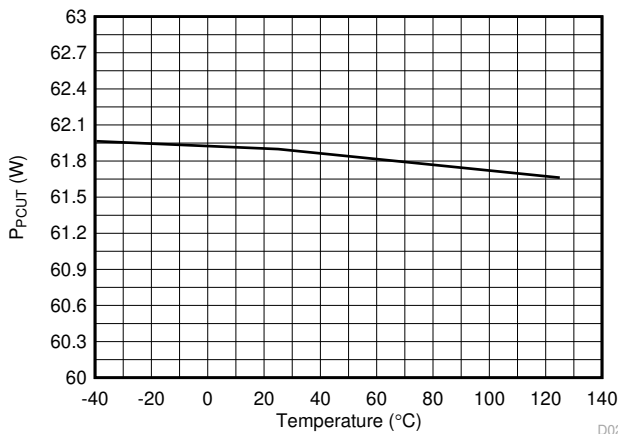


Figure 7-21. 4-Pair PCut Threshold (60W) vs Temperature

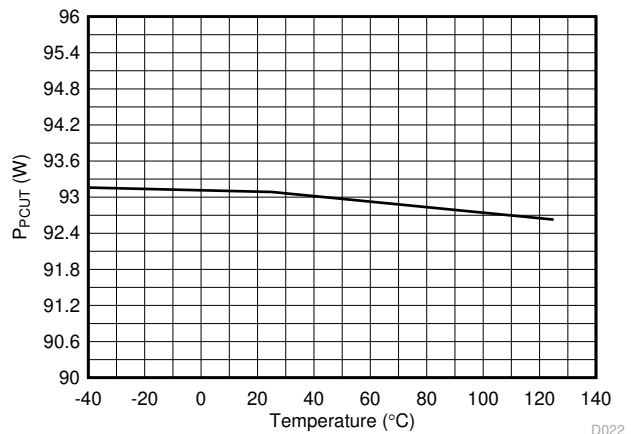


Figure 7-22. 4-Pair PCut Threshold (90W) vs Temperature

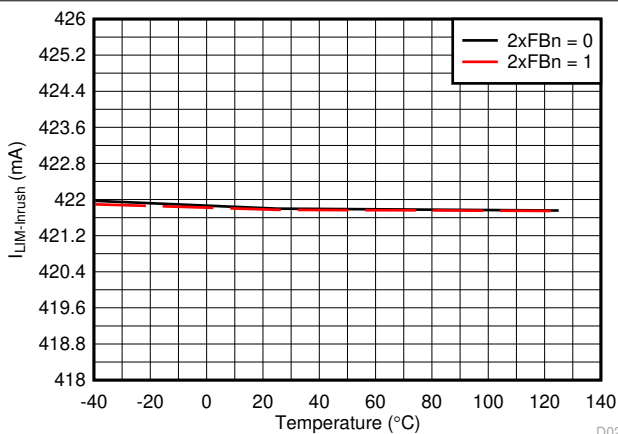


Figure 7-23. Inrush Current Limit vs Temperature

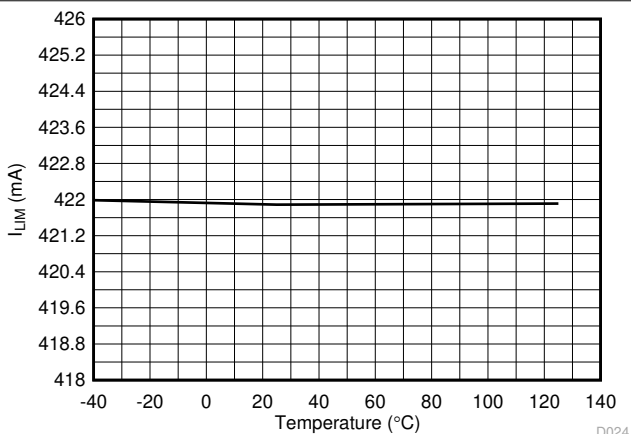


Figure 7-24. 1x Mode (2xFBn = 0) Current Limit vs Temperature

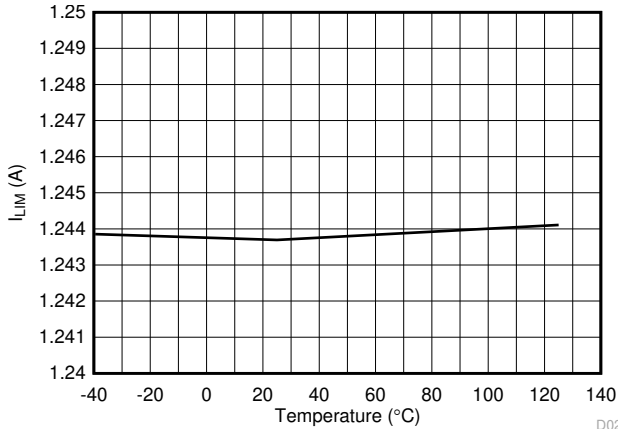


Figure 7-25. 2x Mode (2xFBn = 1) Current Limit vs Temperature

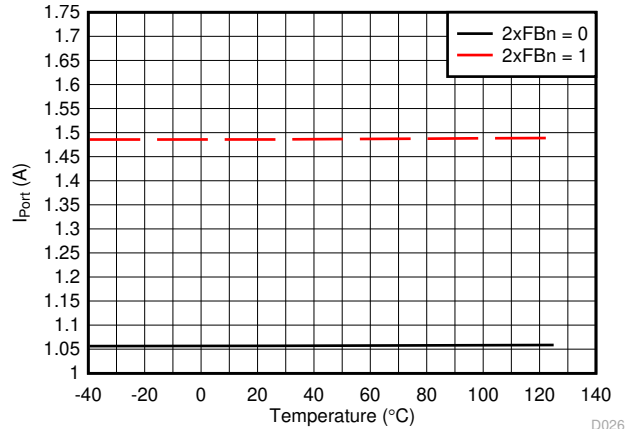


Figure 7-26. I_{SHORT} Threshold vs Temperature

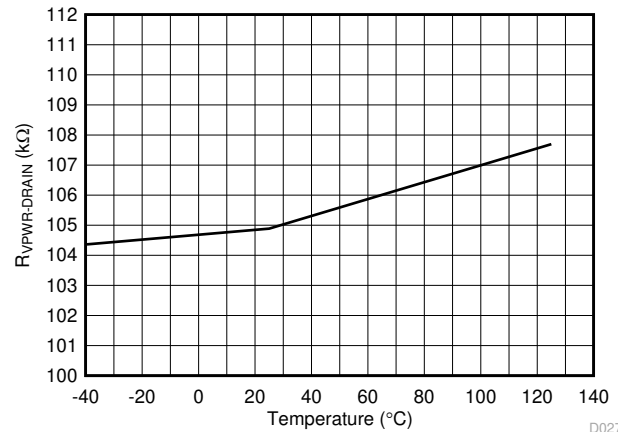


Figure 7-27. R_{OFF} (VPWR to DRAIN) vs Temperature

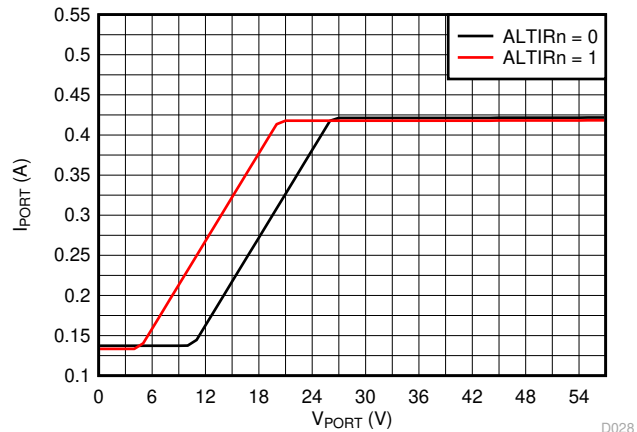


Figure 7-28. Inrush Current Foldback vs Port Voltage

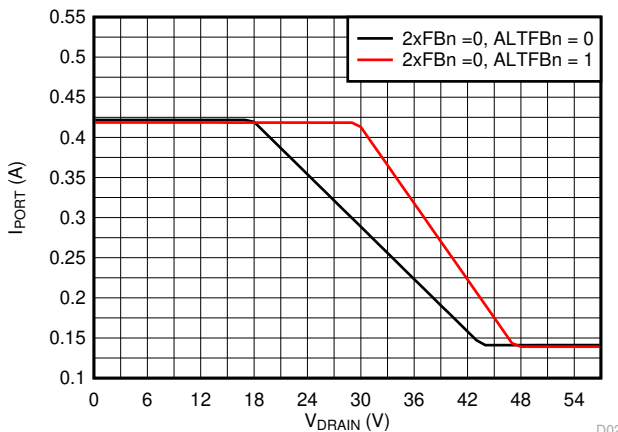


Figure 7-29. 1x Mode (2xFBn = 0) Current Foldback vs Drain Voltage

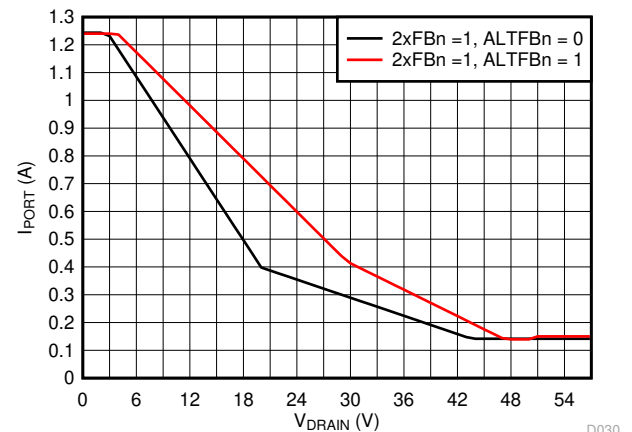


Figure 7-30. 2x Mode (2xFBn = 1) Current Foldback vs Drain Voltage

8 Parameter Measurement Information

8.1 Timing Diagrams

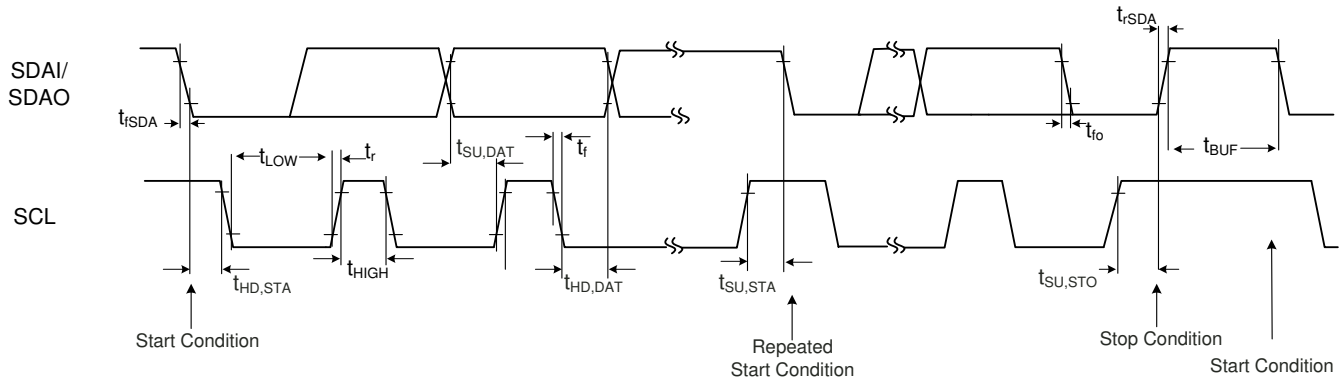


Figure 8-1. I²C Timings

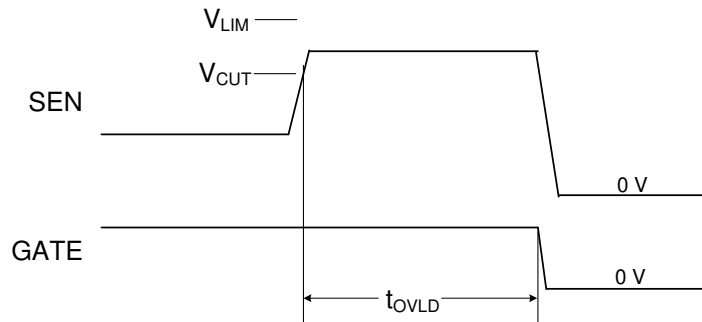


Figure 8-2. Overcurrent Fault Timing

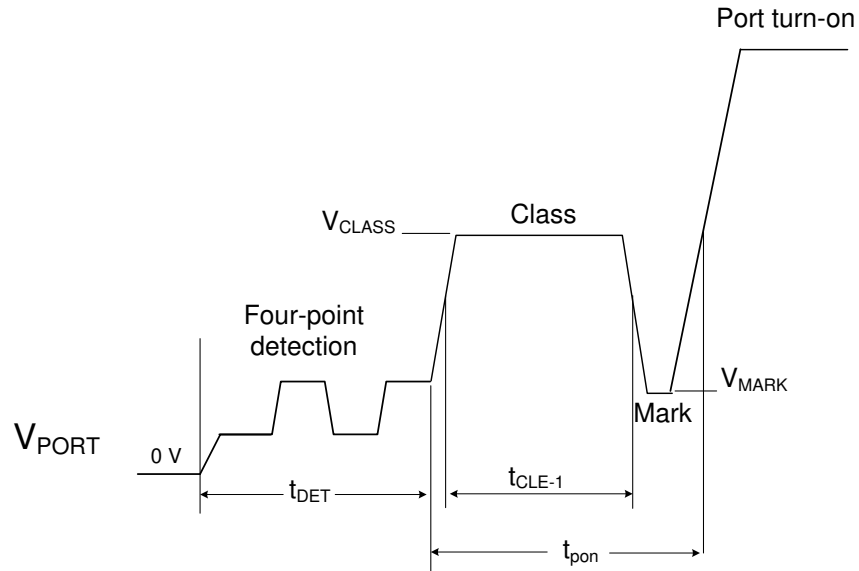


Figure 8-3. 2-Pair Detection, 1-Event Classification and Turn On

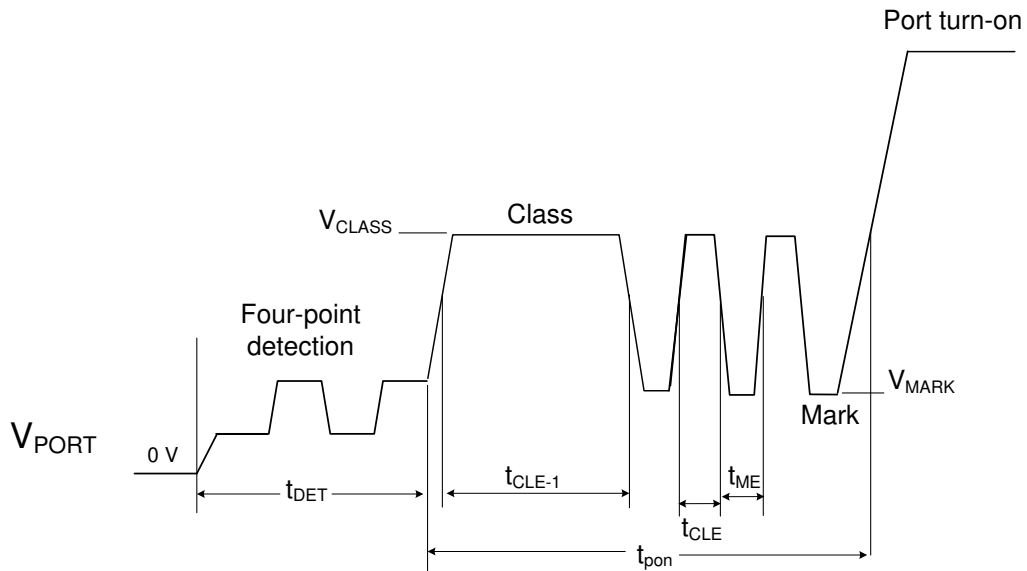


Figure 8-4. 2-Pair Detection, 3-Event Classification and Turn On

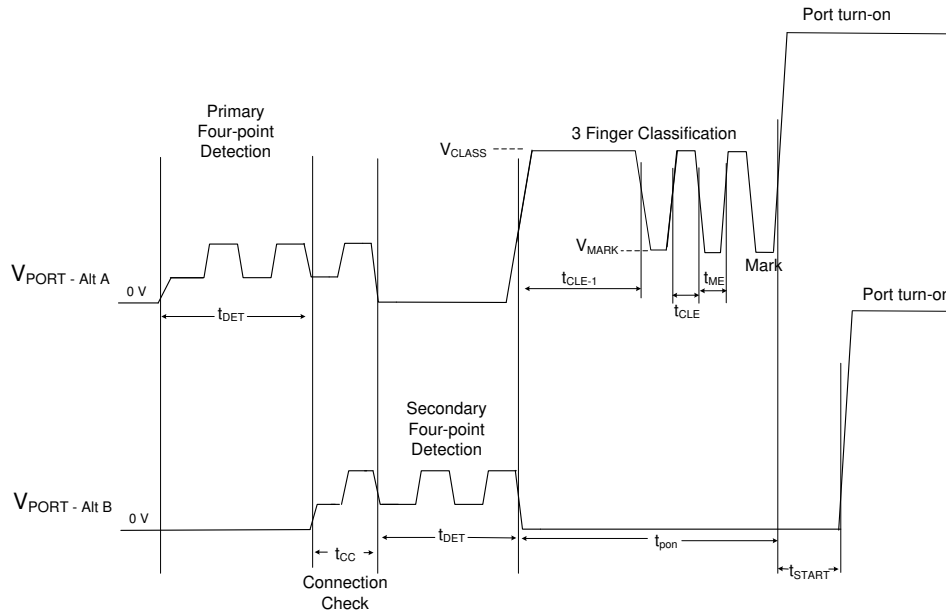


Figure 8-5. 4-Pair Single Signature Detection, 3-Event Classification and Turn On

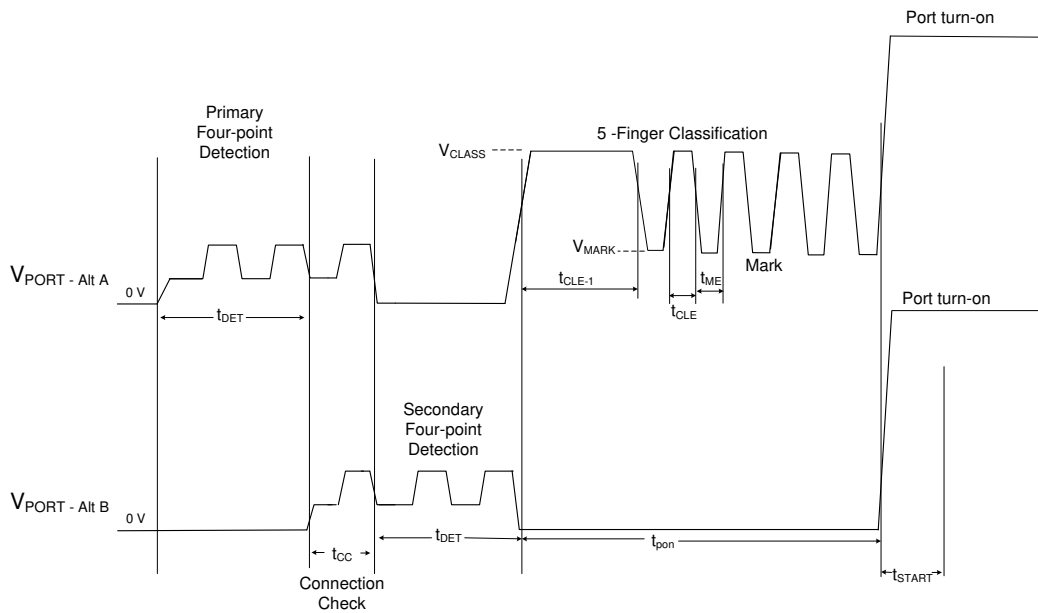


Figure 8-6. 4-Pair Single Signature Detection, 5-Event Classification and Turn On

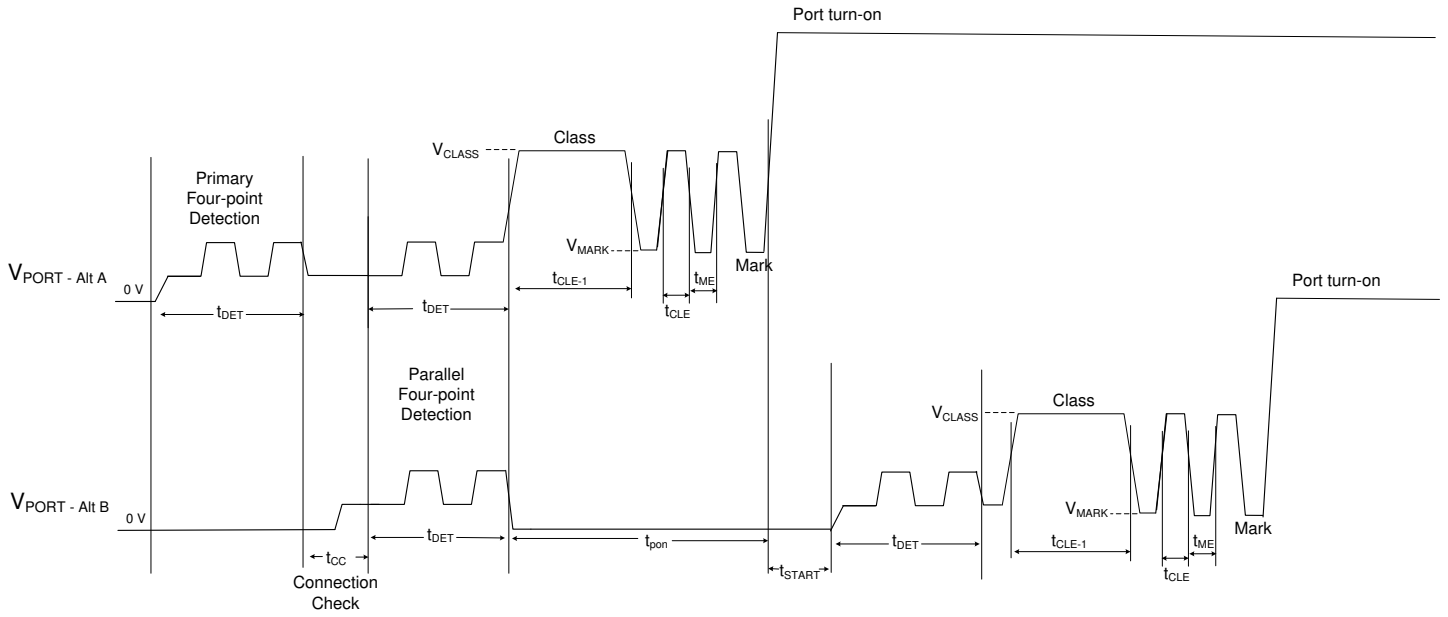


Figure 8-7. 4-Pair Dual Signature Detection, 3-Event Classification and Turn On

9 Detailed Description

9.1 Overview

The TPS23880 is an eight-channel PSE for Power over Ethernet applications. Each of the eight channels provides detection, classification, protection, and shutdown in compliance with the IEEE 802.3bt standard.

Basic PoE features include the following:

- Performs high-reliability 4-point load detection
- Performs mutual identification classification including PoE 2 type-3/4 (three, four or five -fingers) of up to Class 8 loads
- Recognizes single signature and dual signature PDs
- Enables power with protective fold-back current limiting, and an adjustable P_{CUT} threshold
- Shuts down during faults such as overcurrent or outputs shorts
- Performs a maintain power signature function to ensure power is removed if the load is disconnected
- Undervoltage lockout occurs if V_{PWR} falls below V_{PUV_F} (typical 26.5 V).

Enhanced features include the following:

- Programmable SRAM memory
- Dedicated 14-bit integrating current ADCs per port
- Port re-mapping capability
- 8- and 16-bit access mode selectable
- 1- and 3-bit port shutdown priority

9.1.1 Operating Modes

9.1.1.1 Auto

The port performs detection and classification (if valid detection occurs) continuously. Registers are updated each time a detection or classification occurs. The port power is automatically turned on based on the Power Allocation settings in register 0x29 if a valid classification is measured.

9.1.1.2 Semiauto

The port performs detection and classification (if valid detection occurs) continuously. Registers are updated each time a detection or classification occurs. The port power is not automatically turned on. A Power Enable command is required to turn on the port.

9.1.1.3 Manual/Diagnostic

The use of this mode is intended for system diagnostic purposes only in the event that ports cannot be powered in accordance with the IEEE 802.3bt standard from Semiauto or Auto modes.

The port performs the functions as configured in the registers. There is no automatic state change. Singular detection and classification measurements will be performed when commanded. Ports will be turned on immediately after a Power Enable command without any detection or classification measurements. Even though multiple classification events may be provided, the port voltage will reset immediately after the last finger, resetting the PD.

9.1.1.4 Power Off

The port is powered off and does not perform a detection, classification, or power-on. In this mode, Status and Enable bits for the associated port are reset.

9.1.2 PoE Compliance Terminology

With the release of the IEEE 802.3bt standard, compliant PoE equipment has expanded to include four different "Types" of devices that support power over 2-Pair or 4-Pair, in either Single or Dual signature configurations, with classifications ranging from 0 to 8. Different manufactures have used varying terminology over time to describe their equipment capabilities, and it can become difficult to identify how to correctly categorize and brand a particular piece of equipment. For this reason and in conjunction with the Ethernet Alliance (EA), the industry leading providers of PoE equipment and devices have agreed to transition to using the "PoE 1" and "PoE 2" banding per the table below [Table 9-1](#).

Table 9-1. Summary Table of PoE Compliance Terminology

| Brand / Acronym | IEEE Standard | Clause | Clause Title | Types | Classes | EA Certified Logo |
|-----------------|---------------|--------|----------------------------------|-------|---------------------------------|-------------------|
| PoE 1 | 802.3af | 33 | Power over Ethernet over 2-Pairs | 1 | 0 - 3 | Gen 1 Class 1-4 |
| | 802.3at | | | 2 | 0 - 4 | |
| PoE 2 | 802.3bt | 145 | Power over Ethernet | 3 | 1 - 6, or 1-4 DS ⁽¹⁾ | Gen 2 Class 1-8 |
| | | | | 4 | 7 - 8, or 5 DS ⁽¹⁾ | |

(1) "DS" is used to designate "Dual Signature" PDs

Note

By design PoE 2 PSEs are fully interoperable with any existing PoE 1 equipment, and although not all functionality may be enabled, PoE 2 PDs connected to PoE 1 PSEs are required to limit their power consumption to the PSE presented power capabilities see [Power Allocation and Power Demotion](#).

9.1.3 Channel versus Port Terminology

Throughout this document the use of the terms *port* and *channel* will be used regularly, but these terms are **not interchangeable**. Instead the term *port* will be used to refer to the PSE PI (Power Interface), which is most commonly associated with a RJ45 connector, whereas the term *channel* will be used to refer to the individual power path or paths associated with each *port*.

Previous PSE devices commonly equated the number of controlled outputs as *ports* as each output would be dedicated to providing power on either the ALT-A **or** Alt-B pair set of a RJ45 jack/Ethernet port. However, with the adoption of 4-Pair power delivery sending power down both the ALT-A **and** ALT-B pair sets, there is now a need to differentiate between 2-pair and 4-pair capable PoE *ports*. Even more so, with the requirement to provide individual current limiting per pair set, any 4-pair *port* will now use two *channels* per 4-pair *port* to ensure safe and reliable delivery of power down each pair set.

As the TPS23880 is an 8-*channel* PSE controller. It can be configured to support up to eight 2-pair PoE *ports* or four 4-pair PoE *ports*, or any combination thereof where each 2-pair *port* accounts for one *channel*, and each 4-pair *port* accounts for 2 *channels*.

9.1.4 Requested Class versus Assigned Class

The *requested* class is the classification the PSE measures during mutual identification prior to turnon, whereas the *assigned* class is the classification level the channel was powered on with based on the power allocation setting in register 0x29h. In most cases where the power allocation equals or exceeds the *requested* class, the *requested* and *assigned* classes will be the same. However, in the case of power demotion, these values will differ.

For example: If a Class 8 PD is connected to a 60 W (Class 6) limited PSE port, the *requested* class reports "Class 8", while the *assigned* class reports "Class 6".

The **requested** classification results are available in registers 0x0C-0F

The **assigned** classification results are available in registers 0x4C-4F

Note

There is no Assigned Class assigned for ports/channels powered out of Manual/Diagnostic mode.

9.1.5 Power Allocation and Power Demotion

The Power Allocation settings in register 0x29 sets the maximum power level a port will power on. Settings for each Class level from 2-pair 4 W (Class 1) up to 4-pair 90 W (Class 8) have been provided to maximize system design flexibility.

Note

The Power Allocation settings in register 0x29 do not set the power limit for a given port. The port and channel power limiting is configured with the 2P (registers 0x1E- x 21) and 4P (0x2A - x2B) policing registers

During a turn on attempt, if a PD presents a classification level greater than the power allocation setting for a port, the TPS23880 limits the number of classification fingers presented to the PD prior to turn on based on the power allocation settings in register 0x29. This behavior is called *Power Demotion* as it is the number of fingers presented to the PD that sets the maximum level of power the PD is allowed to draw before the PSE is allowed to disable it.

Note

The IEEE 802.3 standard requires PDs that are power demoted by a PSE to limit their total power draw below the Type/class level set by the number of fingers presented by the PSE during mutual identification.

Power Demotion on a port is limited to the Type boundaries as the only means of communication from the PSE to the PD is the number of classification fingers prior to turn on.

- 1 finger = 15.4 W, 3 fingers = 30 W, 4 fingers = 60 W, and 5 fingers = 90W
-

Table 9-2. Single Signature PD Power Demotion Table

| Power Allocation Register 0x29 | Assigned Class Value (based on the PD connected at the port) | | | | | |
|--------------------------------|--|------------|------------|----------------|----------------|----------------|
| | Class 3 PD | Class 4 PD | Class 5 PD | Class 6 PD | Class 7 PD | Class 8 PD |
| 4-Pair 15W | Class 3 | Class 3 | Class 3 | Class 3 | Class 3 | Class 3 |
| 4-Pair 30W | Class 3 | Class 4 | Class 4 | Class 4 | Class 4 | Class 4 |
| 4-Pair 45W | Class 3 | Class 4 | Class 5 | Class 4 | Class 4 | Class 4 |
| 4-Pair 60W | Class 3 | Class 4 | Class 5 | Class 6 | Class 6 | Class 6 |
| 4-Pair 75W | Class 3 | Class 4 | Class 5 | Class 6 | Class 7 | Class 6 |
| 4-Pair 90W | Class 3 | Class 4 | Class 5 | Class 6 | Class 7 | Class 8 |

Table 9-3. Dual Signature PD Power Demotion Table

| Power Allocation Register 0x29 | Assigned Class Value (based on the PD connected at the port) | | | | | |
|--------------------------------|--|--------------------------|-----------------------|--------------------------|-------------------------------|-------------------------------|
| | Class 3D PD | | Class 4D PD | | Class 5D PD | |
| | Odd Channel (Primary) | Even Channel (Secondary) | Odd Channel (Primary) | Even Channel (Secondary) | Odd Channel (Primary) | Even Channel (Secondary) |
| 4-Pair 15W | Class 3 | Insufficient Power | Class 3 | Insufficient Power | Class 3 | Insufficient Power |
| 4-Pair 30W | Class 3 | Class 3 | Class 4 | Insufficient Power | Class 4 | Insufficient Power |
| 4-Pair 45W | Class 3 | Class 3 | Class 4 | Class 3 | Class 4 ⁽¹⁾ | Class 3 ⁽¹⁾ |
| 4-Pair 60W | Class 3 | Class 3 | Class 4 | Class 4 | Class 4 ⁽¹⁾ | Class 4 ⁽¹⁾ |
| 4-Pair 75W | Class 3 | Class 3 | Class 4 | Class 4 | Class 5D | Class 4 |
| 4-Pair 90W | Class 3 | Class 3 | Class 4 | Class 4 | Class 5D | Class 5D |

- (1) To ensure IEEE 802.3bt compliance, Type-3 configured PSEs are not permitted to assign more than 30W (Class 4) of power over any individual pairset. Note: Changes were made in the SRAM release v05 to comply with this requirement.

Note

Class "X-D" Dual Signature PDs present as Class "X" on each alternative pairset. For example: a "Class 4D" PD would present as Class 4 on both the Alternative A and Alternative B pairsets.

9.1.6 Programmable SRAM

The TPS23880 device has been designed to include programmable SRAM that accommodates future firmware updates to support interoperability and/or compliance issues that may arise as new equipment is introduced in conjunction with the release of the IEEE 802.3bt standard.

Note

The latest version of firmware and SRAM release notes may be accessed from the [TI mySecure Software](#) webpage.

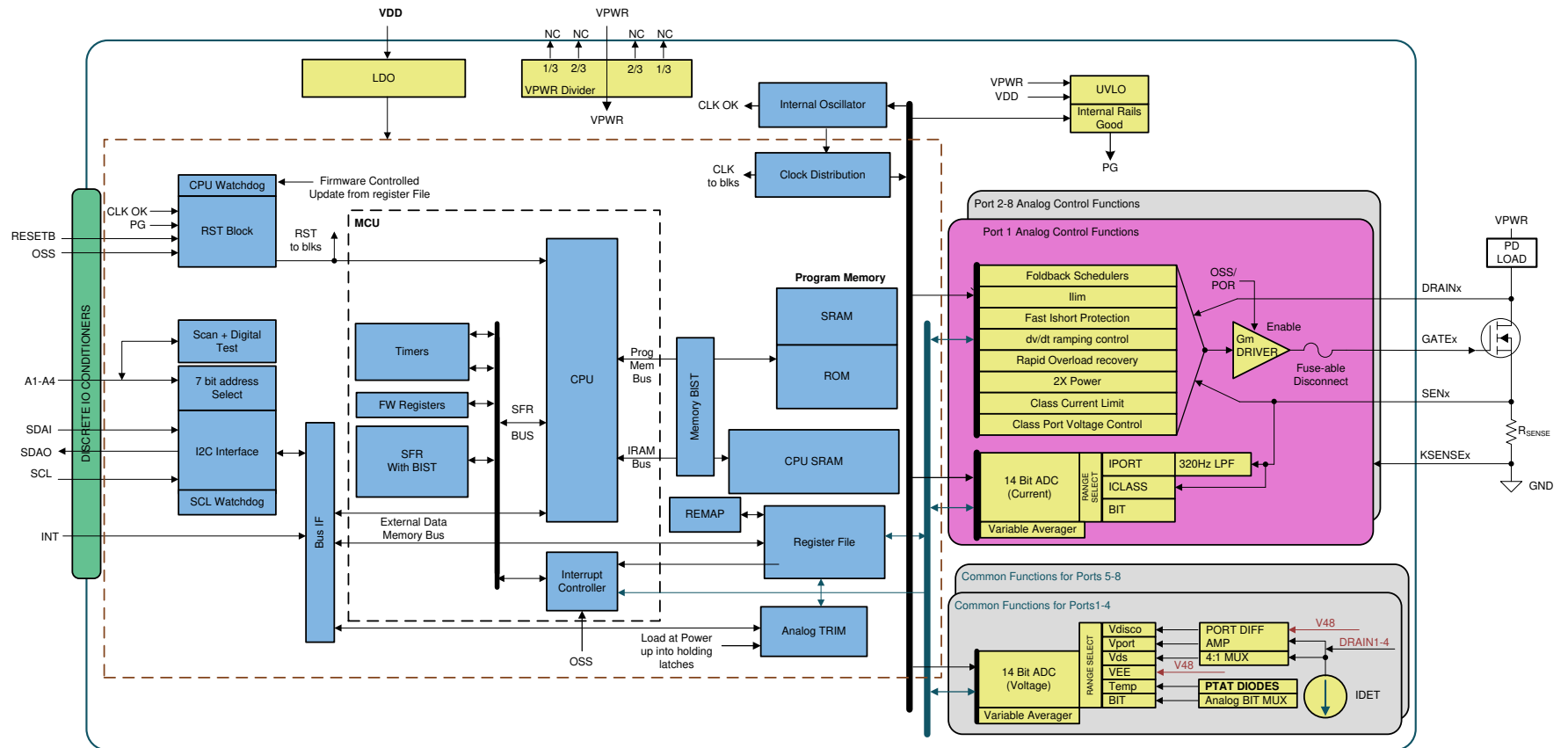
The SRAM Release Notes and ROM Advisory document includes more detailed information regarding any known issues and changes that were associated with each firmware release.

Upon power up, the TPS23880 device requires the SRAM to be programmed via I²C to ensure proper operation and IEEE complaint performance. All I²C traffic other than those commands required to program the SRAM should be deferred until after the SRAM programming sequences are completed.

For systems that include multiple TPS23880 devices, the 0x7F "global" broadcast I2C address may be used to programmed all of the devices at the same time.

For more detailed instructions on the SRAM programming procedures please refer to [Section 9.6.2.65](#) and the [How to Load TPS2388x SRAM Code](#) document on TI.com.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Port Remapping

The TPS23880 provides port remapping capability, from the logical ports to the physical channels and pins.

The remapping is between any channel of a 4-port group (1 to 4, 5 to 8).

The following example is applicable to 0x26 register = 00111001, 00111001b.

- Logical port 1 (5) ↔ Physical channel 2 (6)
- Logical port 2 (6) ↔ Physical channel 3 (7)
- Logical port 3 (7) ↔ Physical channel 4 (8)
- Logical port 4 (8) ↔ Physical channel 1 (5)

Note

The device ignores any remapping command unless all four ports are in off mode.

If the TPS23880 receives an incorrect configuration, it ignores the incorrect configuration and retains the previous configuration. The ACK is sent as usual at the end of communication. For example, if the same remapping code is received for more than one port, then a read back of the Re-Mapping register (0x26) would be the last valid configuration.

Note that if an IC reset command (1Ah register) is received, the port remapping configuration is kept unchanged. However, if there is a Power-on Reset or if the $\overline{\text{RESET}}$ pin is activated, the Re-Mapping register is reinitialized to a default value.

9.3.2 Port Power Priority

The TPS23880 supports 1- and 3-bit shutdown priority, which are selected with the MbitPrty bit of General Mask register (0x17).

The 1-bit shutdown priority works with the Port Power Priority (0x15) register. An OSSn bit with a value of 1 indicates that the corresponding port is treated as low priority, while a value of 0 corresponds to a high priority. As soon as the OSS input goes high, the low-priority ports are turned off.

The 3-bit shutdown priority works with the Multi Bit Power Priority (0x27/28) register, which holds the priority settings. A port with “000” code in this register has highest priority. Port priority reduces as the 3-bit value increases, with up to 8 priority levels. See [Figure 9-1](#).

The multi bit port priority implementation is defined as the following:

- OSS code ≤ Priority setting (0x27/28 register): Port is disabled
- OSS code > Priority setting (0x27/28 register): Port remains active

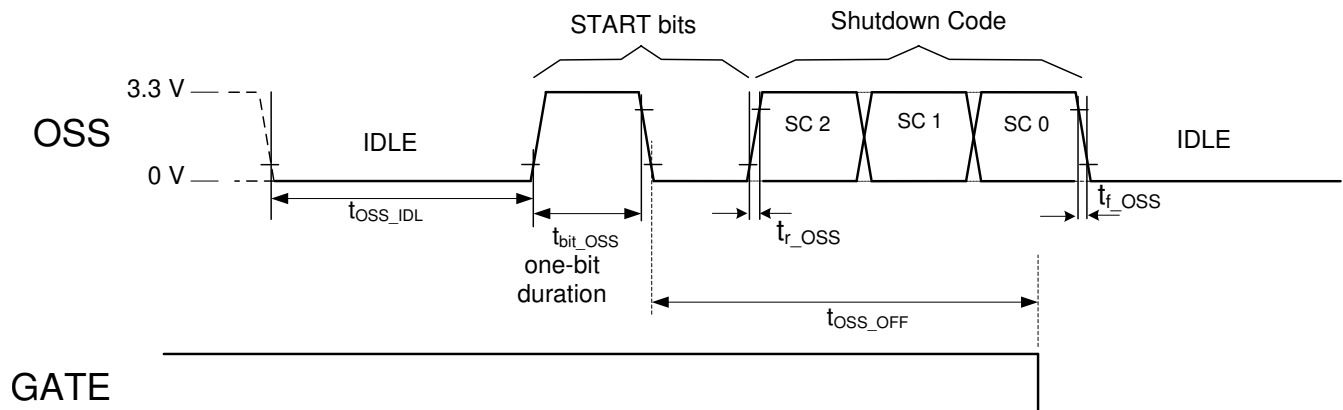


Figure 9-1. Multi Bit Priority Port Shutdown if Lower-Priority Port

Note

Prior to setting the MbitPrty bit from 0 to 1, make sure the OSS input is in the idle (low) state for a minimum of 200 μ s, to avoid any port misbehavior related to loss of synchronization with the OSS bit stream.

Note

The OSS input has an internal 1- μ s to 5- μ s deglitch filter. From the idle state, a pulse with a longer duration is interpreted as a valid start bit. Ensure that the OSS signal is noise free.

Note

To ensure both channels of a 4-pair port are disabled during an OSS event, make sure both channels have the same configurations in the 0x15 or 0x27/28 registers.

9.3.3 Analog-to-Digital Converters (ADC)

The TPS23880 features 10 multi-slope integrating converters. Each of the first eight converters is dedicated to current measurement for one channel and operate independently to perform measurements during classification and when the channel is powered on. When the channel is powered, the converter is used for current (100-ms averaged) monitoring, power policing, and DC disconnect. Each of the last two converters are shared within a group of four channels for discovery (16.6-ms averaged), port powered voltage monitoring, power-good status, and FET short detection. These converters are also used for general-purpose measurements including input voltage (1 ms) and die temperature.

The ADC type used in the TPS23880 differs from other similar types of converters in that the ADCs continuously convert while the input signal is sampled by the integrator, providing inherent filtering over the conversion period. The typical conversion time of the current converters is 800 μ s, while the conversion time is 1 ms for the other converters. Powered-device detection is performed by averaging 16 consecutive samples which provides significant rejection of noise at 50-Hz or 60-Hz line frequency. While a port is powered, digital averaging provides a channel current measurement integrated over a 100-ms time period. Note that an anti-aliasing filter is present for powered current monitoring.

Note

During powered mode, current conversions are performed continuously. Also, in powered mode, the t_{START} timer must expire before any current or voltage ADC conversion can begin.

9.3.4 I²C Watchdog

An I²C Watchdog timer is available on the TPS23880 device. The timer monitors the I²C, SCL line for clock edges. When enabled, a timeout of the watchdog resets the I²C interface along with any active ports. This feature provides protection in the event of a hung software situation or I²C bus hang-up by slave devices. In the latter case, if a slave is attempting to send a data bit of 0 when the master stops sending clocks, then the slave may drive the data line low indefinitely. Because the data line is driven low, the master cannot send a STOP to clean up the bus. Activating the I²C watchdog feature of the TPS23880 clears this deadlocked condition. If the timer of two seconds expires, the ports latch off and the WD status bit is set. Note that WD Status will be set even if the watchdog is not enabled. The WD status bit may only be cleared by a device reset or writing a 0 to the WDS status bit location. The 4-bit watchdog disable field shuts down this feature when a code of 1011b is loaded. This field is preset to 1011b whenever the TPS23880 is initially powered. See [I²C WATCHDOG Register](#) for more details.

9.3.5 Current Foldback Protection

The TPS23880 features two types of foldback mechanisms for complete MOSFET protection.

During inrush, at channel turn on, the foldback is based on the channel voltage as shown in [Figure 9-2](#). Note that the inrush current profile remains the same, regardless of the state of the 2xFBn bits in register 0x40.

After the channel is powered and the Power Good is valid, a dual-slope operational foldback is used, providing protection against partial and total short-circuit at port output, while still being able to maintain the PD powered during normal transients at the PSE input voltage. Note that setting the 2xFBn bit selects the 2x curve and clearing it selects the 1x curve. See [Figure 9-3](#).

In addition to the default foldback curves, the TPS23880 has individually enabled *alternative* foldback curves for both inrush and powered operation. These curves have been designed to accommodate certain loads that do not fully comply with the IEEE standard and requires additional power to be turned on or remain powered. See [Figure 9-2](#) and [Figure 9-3](#).

Note

If using the Alternative Foldback curves (ALTIRn or ALTFBn = 1), designers need to account for the additional power dissipation that can occur in the FETs under these conditions.

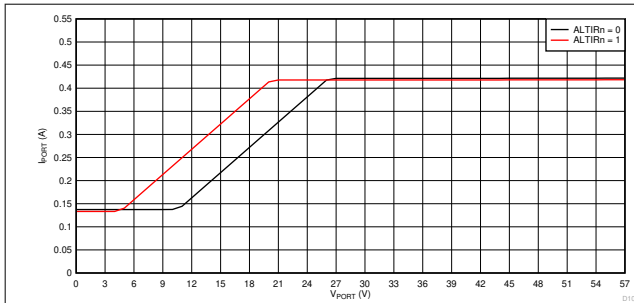


Figure 9-2. Foldback During Inrush (at Port Turn On): I_{LIM} vs V_{port}

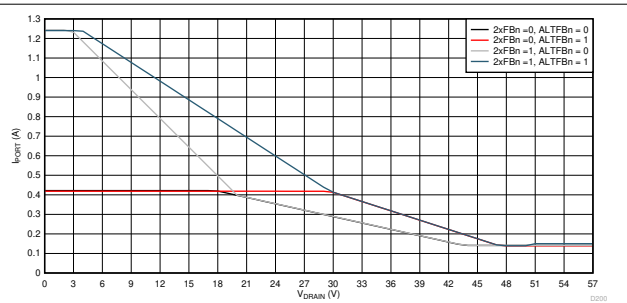


Figure 9-3. Foldback When the Port is Already ON: I_{LIM} vs V_{drain}

9.4 Device Functional Modes

9.4.1 Detection

To eliminate the possibility of false detection, the TPS23880 uses a TI proprietary 4-point detection method to determine the signature resistance of the PD device. A false detection of a valid 25-k Ω signature can occur with 2-point detection type PSEs in noisy environments or if the load is highly capacitive.

Detection 1 and Detection 2 are merged into a single detection function which is repeated. Detection 1 applies I1 (160 μ A) to a channel, waits approximately 60 ms, then measures the channel voltage (V_1) with the integrating ADC. Detection 2 then applies I2 (270 μ A) to the channel, waits another approximately 60 ms, then measures the channel voltage again (V_2). The process is then repeated a second time to capture a third (V_3) and fourth (V_4) channel voltage measurements. Multiple comparisons and calculations are performed on all four measurement point combinations to eliminate the effects of a nonlinear or hysteretic PD signature. The resulting channel signature is then sorted into the appropriate category.

Note

The detection resistance measurement result is also available in the Channel Detect Resistance registers (0x44 - 0x47).

9.4.2 Connection Check

For 4-pair configured ports, the TPS23880 performs a connection check immediately after it measures a valid detection on either channel. During connection check both channels are probed to determine if a single signature

or dual signature load is present on the port, and the results of this measurement are provided in the lower nibble (4 bits) of register 0x1C. The accurate determination of a single signature or dual signature is critical to the PSEs management of the port.

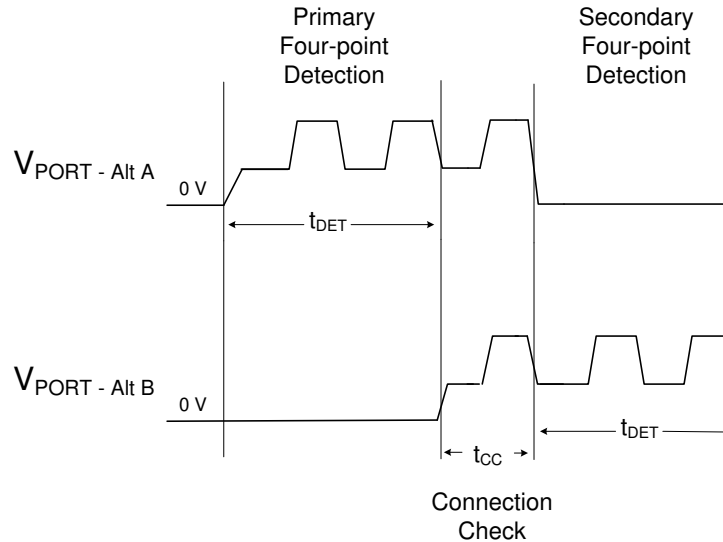


Figure 9-4. 4-Pair Port, Detection and Connection Check Waveforms with a Single Signature Load

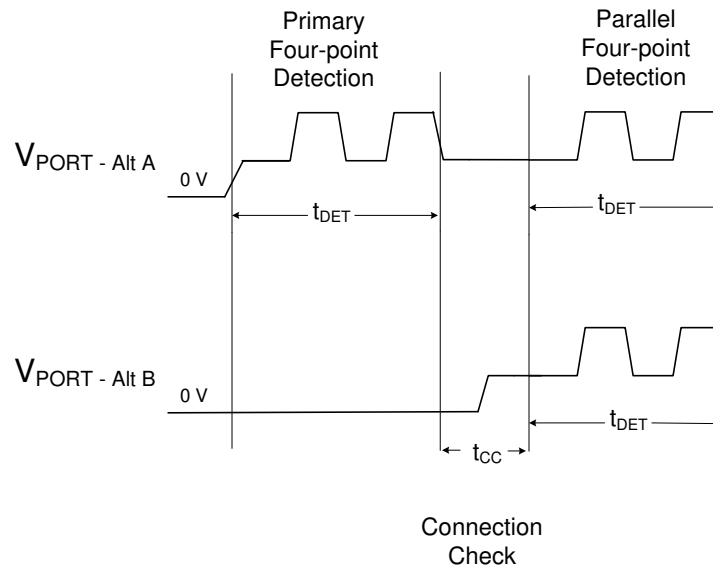


Figure 9-5. 4-Pair Port, Detection and Connection Check Waveforms with a Dual Signature Load

9.4.3 Classification

Hardware classification (class) is performed by supplying a voltage and sampling the resulting current. To eliminate the high power of a classification event from occurring in the power controller chip, the TPS23880 uses the external power FET for classification.

During classification, the voltage on the gate node of the external MOSFET is part of a linear control loop. The control loop applies the appropriate MOSFET drive to maintain a differential voltage between VPWR and DRAIN of 18.5 V. During classification the voltage across the sense resistor in the source of the MOSFET is measured and converted to a class level within the TPS23880. If a load short occurs during classification, the MOSFET gate voltage reduces to a linearly controlled, short-circuit value for the duration of the class event.

Classification results are read through the I²C Detection Event and Channel-n Discovery Registers. The TPS23880 also supports 1, 3, 4, or 5 finger classification for PDs ranging from Class 0 through Class 8, using the Power Enable and Port Power Allocation registers.

9.4.4 DC Disconnect

Disconnect is the automated process of turning off power to the port. When the port is unloaded or at least falls below minimum load, it is required to turn off power to the port and restart detection. In DC disconnect, the voltage across the sense resistors is measured. When enabled, the DC disconnect function monitors the sense resistor voltage of a powered port to verify the port is drawing at least the minimum current to remain active. The T_{DIS} timer counts up whenever the port current is below the disconnect threshold (6.5 mA or 4.5 mA depending on the port configuration). If a timeout occurs, the port is shut down and the corresponding disconnect bit in the Fault Event Register is set. In the case of a PD implementing MPS (maintain Power Signature) current pulsing, the T_{DIS} counter is reset each time the current goes continuously higher than the disconnect threshold for at least 3 ms.

The T_{DIS} duration is set by the T_{MPDO} Bits of the Timing Configuration register (0x16).

Note

If a Class 4 or lower 4-Pair Single Signature PD is connected, the TPS23880 will immediately power down one channel immediately after (no T_{MPDO} timeout) the current falls below the disconnect threshold while leaving the second channel powered. This channel will be re-powered if the current on the remaining channel exceed 75mA. Alternatively if the current on the remaining channel falls below the disconnect threshold for longer than the T_{MPDO} timeout, the port will be shut down and the corresponding disconnect bits in the Fault Event Register are set.

Note

If both channels of a 4-Pair Dual Signature PD are powered, the DCDTx bit in register 0x2D is automatically set after turn on to ensure the IEEE compliant 4.5mA threshold is used.

Note

If a 4-Pair Single Signature Class 5-8 PD is powered, the DCDTx bit in register 0x2D is automatically set after turn on to ensure the IEEE compliant 4.5mA threshold is used.

9.5 I²C Programming

9.5.1 I²C Serial Interface

The TPS23880 features a 3-wire I²C interface, using SDAI, SDAO, and SCL. Each transmission includes a START condition sent by the master, followed by the device address (7-bit) with R/W bit, a register address byte, then one or two data bytes and a STOP condition. The recipient sends an acknowledge bit following each byte transmitted. SDAI/SDAO is stable while SCL is high except during a START or STOP condition.

Figure 9-6 and Figure 9-7 show read and write operations through I²C interface, using configuration A or B (see Table 9-24 for more details). The parametric read operation is applicable to ADC conversion results. The TPS23880 features quick access to the latest addressed register through I²C bus. When a STOP bit is received, the register pointer is not automatically reset.

It is also possible to perform a write operation to many TPS23880 devices at the same time. The slave address during this broadcast access is 0x7F, as shown in Section 9.6.2.13. Depending on which configuration (A or B) is selected, a global write proceeds as following:

- Config A: Both 4-port devices (1 to 4 and 5 to 8) are addressed at same time.
- Config B: The whole device is addressed.

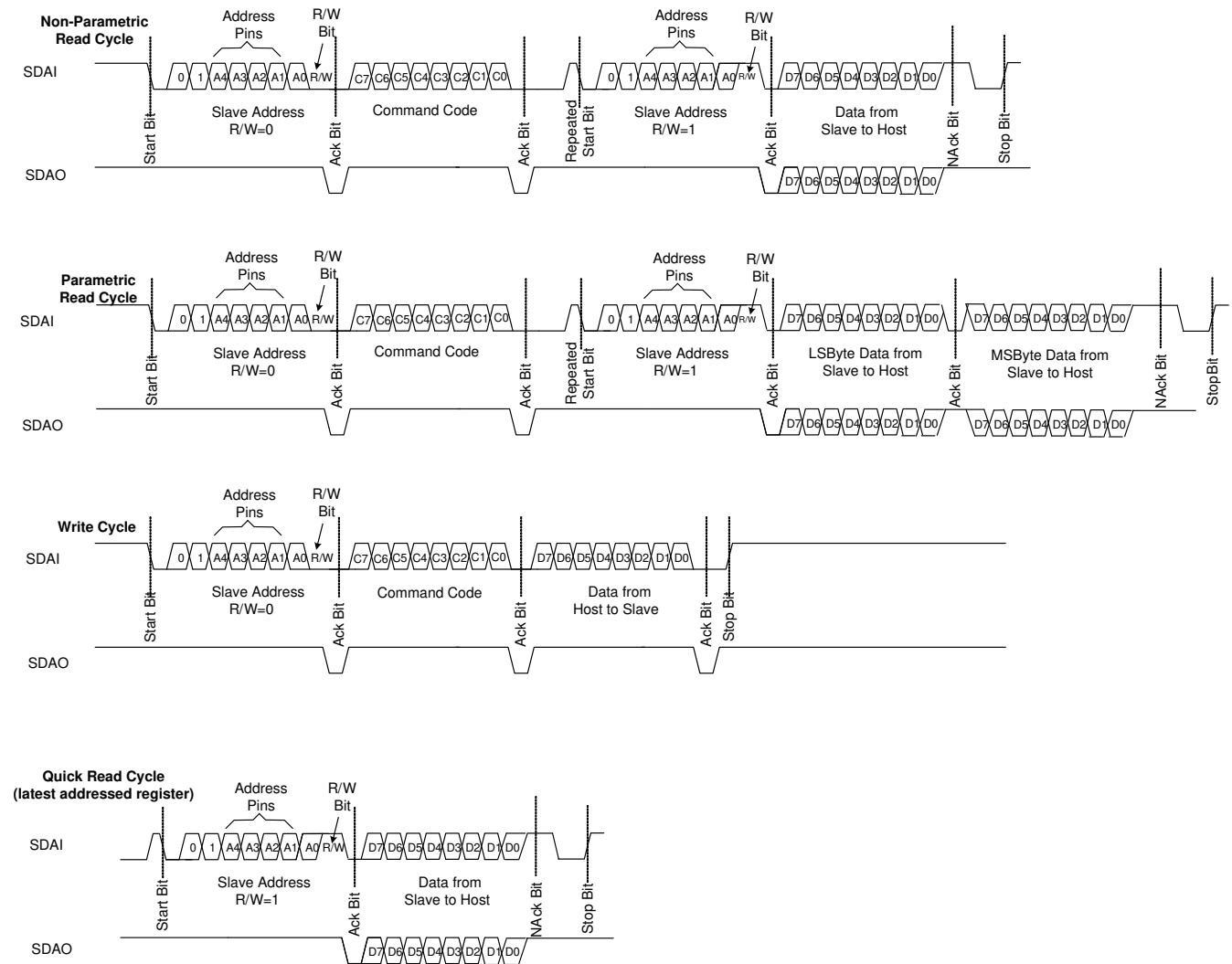


Figure 9-6. I²C interface Read and Write Protocol – Configuration A

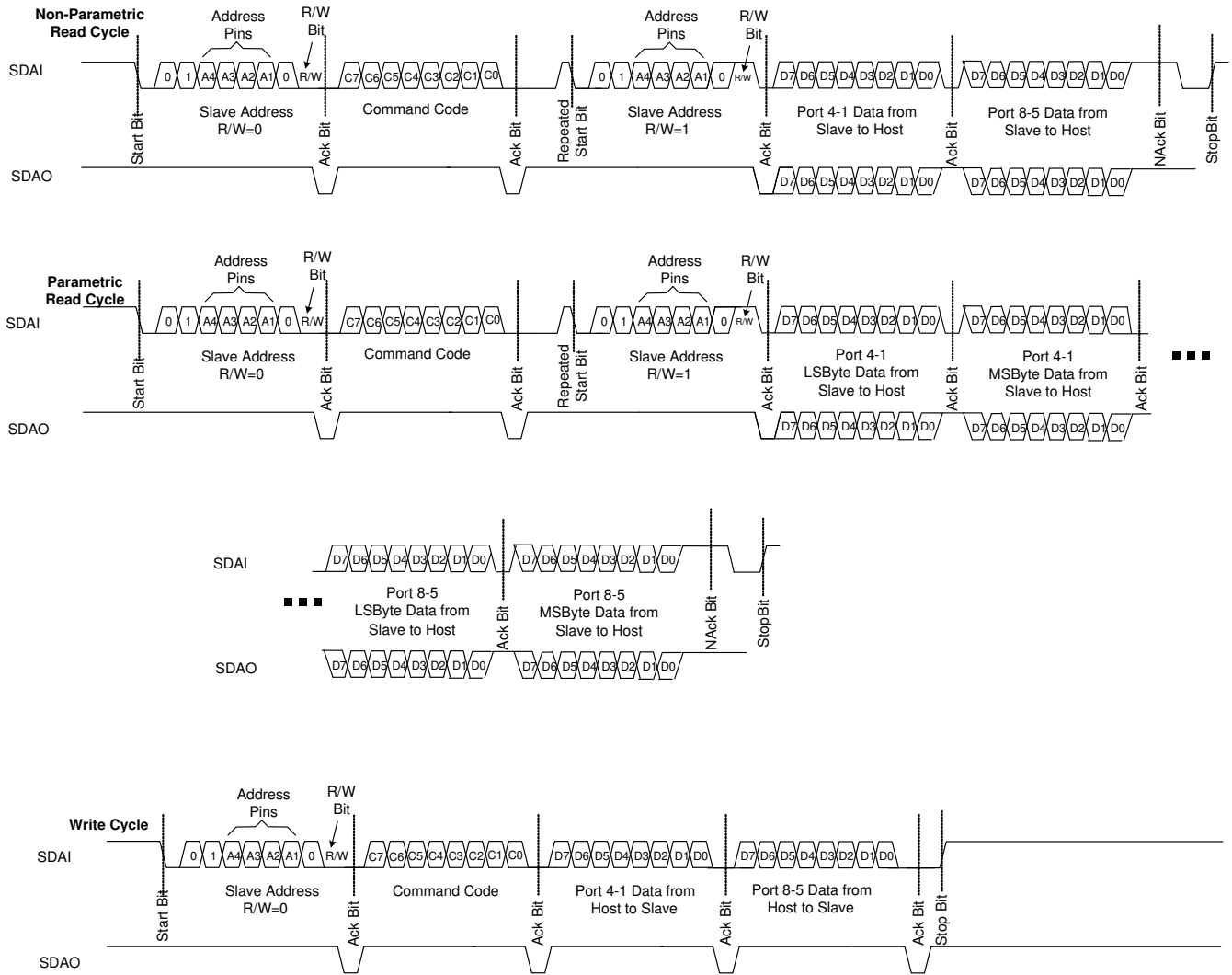


Figure 9-7. I²C interface Read and Write Protocol – Configuration B

9.6 Register Maps

9.6.1 Complete Register Set

Table 9-4. Main Registers

| Cmd Code | Register or Command Name | I ² C R/W | Data Byte | RST State | Bits Description | | | | | | | |
|----------------------|--------------------------|----------------------|-----------|---------------------------|---------------------------|-------|----------------|----------|----------------------------|--------|----------------|--------|
| INTERRUPTS | | | | | | | | | | | | |
| 00h | INTERRUPT | RO | 1 | 1000,0000b ⁽¹⁾ | SUPF | STRTF | IFAULT | CLASC | DETC | DISF | PGC | PEC |
| 01h | INTERRUPT MASK | R/W | 1 | 1000,0000b | SUMSK | STMSK | IFMSK | CLMSK | DEMSK | DIMSK | PGMSK | PEMSK |
| EVENT | | | | | | | | | | | | |
| 02h | POWER EVENT | RO | 1 | 0000,0000b | Power Good status change | | | | Power Enable status change | | | |
| 03h | | CoR | 1 | | PGC4 | PGC3 | PGC2 | PGC1 | PEC4 | PEC3 | PEC2 | PEC1 |
| 04h | DETECTION EVENT | RO | 1 | 0000,0000b | Classification | | | | Detection | | | |
| 05h | | CoR | 1 | | CLSC4 | CLSC3 | CLSC2 | CLSC1 | DETC4 | DETC3 | DETC2 | DETC1 |
| 06h | FAULT EVENT | RO | 1 | 0000,0000b | Disconnect occurred | | | | PCUT fault occurred | | | |
| 07h | | CoR | 1 | | DISF4 | DISF3 | DISF2 | DISF1 | PCUT4 | PCUT3 | PCUT2 | PCUT1 |
| 08h | START/ILIM EVENT | RO | 1 | 0000,0000b | ILIM fault occurred | | | | START fault occurred | | | |
| 09h | | CoR | 1 | | ILIM4 | ILIM3 | ILIM2 | ILIM1 | STR4 | STR3 | STR2 | STR1 |
| 0Ah | SUPPLY/FAULT EVENT | RO | 1 | 0111,0000b ⁽²⁾ | TSD | VDUV | VDWRN | VPUV | PCUT34 | PCUT12 | OSSE | RAMFLT |
| 0Bh | | CoR | 1 | | | | | | | | | |
| STATUS | | | | | | | | | | | | |
| 0Ch | CHANNEL 1 DISCOVERY | RO | 1 | 0000,0000b | Requested CLASS Channel 1 | | | | DETECT Channel 1 | | | |
| 0Dh | CHANNEL 2 DISCOVERY | RO | 1 | 0000,0000b | Requested CLASS Channel 2 | | | | DETECT Channel 2 | | | |
| 0Eh | CHANNEL 3 DISCOVERY | RO | 1 | 0000,0000b | Requested CLASS Channel 3 | | | | DETECT Channel 3 | | | |
| 0Fh | CHANNEL 4 DISCOVERY | RO | 1 | 0000,0000b | Requested CLASS Channel 4 | | | | DETECT Channel 4 | | | |
| 10h | POWER STATUS | RO | 1 | 0000,0000b | PG4 | PG3 | PG2 | PG1 | PE4 | PE3 | PE2 | PE1 |
| 11h | PIN STATUS | RO | 1 | 0,A[4:0],0,0 | Rsvd | SLA4 | SLA3 | SLA2 | SLA1 | SLA0 | Rsvd | Rsvd |
| CONFIGURATION | | | | | | | | | | | | |
| 12h | OPERATING MODE | R/W | 1 | 0000,0000b | Channel 4 Mode | | Channel 3 Mode | | Channel 2 Mode | | Channel 1 Mode | |
| 13h | DISCONNECT ENABLE | R/W | 1 | 0000,1111b | Rsvd | Rsvd | Rsvd | Rsvd | DCDE4 | DCDE3 | DCDE2 | DCDE1 |
| 14h | DETECT/CLASS ENABLE | R/W | 1 | 0000,0000b | CLE4 | CLE3 | CLE2 | CLE1 | DETE4 | DETE3 | DETE2 | DETE1 |
| 15h | PWRPR/PCUT DISABLE | R/W | 1 | 0000,0000b | OSS4 | OSS3 | OSS2 | OSS1 | DCUT4 | DCUT3 | DCUT2 | DCUT1 |
| 16h | TIMING CONFIG | R/W | 1 | 0000,0000b | TLIM | | TSTART | | TOVLD | | TMPDO | |
| 17h | GENERAL MASK | R/W | 1 | 1000,0000b | INTEN | Rsvd | nbitACC | MbitPrty | CLCHE | DECHE | Rsvd | |

Table 9-4. Main Registers (continued)

| Cmd Code | Register or Command Name | I ² C R/W | Data Byte | RST State | Bits Description | | | | | | | |
|---|--------------------------------|----------------------|-----------|------------|--------------------------------|-----------|--|-------|--------------------------------|---------|--------------------------------|--------|
| PUSH BUTTONS | | | | | | | | | | | | |
| 18h | DETECT/CLASS Restart | WO | 1 | 0000,0000b | RCL4 | RCL3 | RCL2 | RCL1 | RDET4 | RDET3 | RDET2 | RDET1 |
| 19h | POWER ENABLE | WO | 1 | 0000,0000b | POFF4 | POFF3 | POFF2 | POFF1 | PWON4 | PWON3 | PWON2 | PWON1 |
| 1Ah | RESET | WO | 1 | 0000,0000b | CLRRAIN | CLINP | Rsvd | RESAL | RESP4 | RESP3 | RESP2 | RESP1 |
| GENERAL/SPECIALIZED | | | | | | | | | | | | |
| 1Bh | ID | RO | 1 | 0101,0101b | MFR ID | | | | IC Version | | | |
| 1Ch | AUTOCLASS and CONNECTION CHECK | RO | 1 | 0000,0000b | AC4 | AC3 | AC2 | AC1 | CC34_2 | CC34_1 | CC12_2 | CC12_1 |
| 1Dh | RESERVED | R/W | 1 | 0000,0000b | Rsvd | | | | | | | |
| 1Eh | 2P POLICE 1 CONFIG | R/W | 1 | 1111,1111b | 2-Pair POLICE Channel 1 | | | | | | | |
| 1Fh | 2P POLICE 2 CONFIG | R/W | 1 | 1111,1111b | 2-Pair POLICE Channel 2 | | | | | | | |
| 20h | 2P POLICE 3 CONFIG | R/W | 1 | 1111,1111b | 2-Pair POLICE Channel 3 | | | | | | | |
| 21h | 2P POLICE 4 CONFIG | R/W | 1 | 1111,1111b | 2-Pair POLICE Channel 4 | | | | | | | |
| 22h | Reserved | R/W | 1 | 0000,0000b | Rsvd | Rsvd | Rsvd | Rsvd | Rsvd | Rsvd | Rsvd | Rsvd |
| 23h | Reserved | R/W | 1 | 0000,0000b | Rsvd | Rsvd | Rsvd | Rsvd | Rsvd | Rsvd | Rsvd | Rsvd |
| 24h | Power-on FAULT | RO | 1 | 0000,0000b | PF Channel 4 | | PF Channel 3 | | PF Channel 2 | | PF Channel 1 | |
| 25h | | CoR | 1 | | | | | | | | | |
| 26h | RE-MAPPING | R/W | 1 | 1110,0100b | Physical re-map Logical Port 4 | | Physical re-map Logical Port 3 | | Physical re-map Logical Port 2 | | Physical re-map Logical Port 1 | |
| 27h | Multi-Bit Priority 21 | R/W | 1 | 0000,0000b | Rsvd | Channel 2 | | Rsvd | Channel 1 | | | |
| 28h | Multi-Bit Priority 43 | R/W | 1 | 0000,0000b | Rsvd | Channel 4 | | Rsvd | Channel 3 | | | |
| 29h | Port Power Allocation | R/W | 1 | 0000,0000b | 4P34 | | MC34 | | 4P12 | | MC12 | |
| 2Ah | 4P POLICE 12 CONFIG | R/W | 1 | 1111,1111b | 4-Pair POLICE Channels 1 and 2 | | | | | | | |
| 2Bh | 4P POLICE 34 CONFIG | R/W | 1 | 1111,1111b | 4-Pair POLICE Channels 3 and 4 | | | | | | | |
| 2Ch | TEMPERATURE | RO | 1 | 0000,0000b | Temperature (bits 7 to 0) | | | | | | | |
| 2Dh | 4P FAULT CONFIG | R/W | 1 | 0000,0000b | NLM34 | NLM12 | NCT34 | NCT12 | 4PPCT34 | 4PPCT12 | DCDT34 | DCDT12 |
| 2Eh | INPUT VOLTAGE | RO | 2 | 0000,0000b | Input Voltage: LSByte | | | | | | | |
| 2Fh | | RO | | 0000,0000b | Rsvd | Rsvd | Input Voltage: MSByte (bits 13 to 8) | | | | | |
| EXTENDED REGISTER SET – PARAMETRIC MEASUREMENT | | | | | | | | | | | | |
| 30h | Channel 1 CURRENT | RO | 2 | 0000,0000b | Channel 1 Current: LSByte | | | | | | | |
| 31h | | RO | | 0000,0000b | Rsvd | Rsvd | Channel 1 Current: MSByte (bits 13 to 8) | | | | | |
| 32h | Channel 1 VOLTAGE | RO | 2 | 0000,0000b | Channel 1 Voltage: LSByte | | | | | | | |
| 33h | | RO | | 0000,0000b | Rsvd | Rsvd | Channel 1 Voltage: MSByte (bits 13 to 8) | | | | | |

- (1) SUPF bit reset state shown is at Power up only
- (2) VDUV, VPUV and VDWRN bits reset state shown is at Power up only

Table 9-5. Main Registers

| Cmd Code | Register or Command Name | I ² C R/W | Data Byte | RST State | Bits Description | | | | | | | |
|-------------------------------|--------------------------|----------------------|-----------|------------|---------------------------|-------|--|------------------|-------------------------|------|------|------|
| 34h | Channel 2 CURRENT | RO | 2 | 0000,0000b | Channel 2 Current: LSByte | | | | | | | |
| 35h | | RO | | 0000,0000b | Rsvd | Rsvd | Channel 2 Current: MSByte (bits 13 to 8) | | | | | |
| 36h | Channel 2 VOLTAGE | RO | 2 | 0000,0000b | Channel 2 Voltage: LSByte | | | | | | | |
| 37h | | RO | | 0000,0000b | Rsvd | Rsvd | Channel 2 Voltage: MSByte (bits 13 to 8) | | | | | |
| 38h | Channel 3 CURRENT | RO | 2 | 0000,0000b | Channel 3 current: LSByte | | | | | | | |
| 39h | | RO | | 0000,0000b | Rsvd | Rsvd | Channel 3 Current: MSByte (bits 13 to 8) | | | | | |
| 3Ah | Channel 3 VOLTAGE | RO | 2 | 0000,0000b | Channel 3 Voltage: LSByte | | | | | | | |
| 3Bh | | RO | | 0000,0000b | Rsvd | Rsvd | Channel 3 Voltage: MSByte (bits 13 to 8) | | | | | |
| 3Ch | Channel 4 CURRENT | RO | 2 | 0000,0000b | Channel 4 current: LSByte | | | | | | | |
| 3Dh | | RO | | 0000,0000b | Rsvd | Rsvd | Channel 4 Current: MSByte (bits 13 to 8) | | | | | |
| 3Eh | Channel 4 VOLTAGE | RO | 2 | 0000,0000b | Channel 4 Voltage: LSByte | | | | | | | |
| 3Fh | | RO | | 0000,0000b | Rsvd | Rsvd | Channel 4 Voltage: MSByte (bits 13 to 8) | | | | | |
| CONFIGURATION/OTHERS | | | | | | | | | | | | |
| 40h | CHANNEL FOLDBACK | R/W | 1 | 0000,0000b | 2xFB4 | 2xFB3 | 2xFB2 | 2xFB1 | Rsvd | Rsvd | Rsvd | Rsvd |
| 41h | FIRMWARE REVISION | RO | 1 | RRRR,RRRRb | Firmware Revision | | | | | | | |
| 42h | I2C WATCHDOG | R/W | 1 | 0001,0110b | Rsvd | Rsvd | Rsvd | Watchdog Disable | | | WDS | |
| 43h | DEVICE ID | RO | 1 | 0010,0001b | Device ID number | | | | Silicon Revision number | | | |
| SIGNATURE MEASUREMENTS | | | | | | | | | | | | |
| 44h | Ch1 DETECT RESISTANCE | RO | 1 | 0000,0000b | Channel 1 Resistance | | | | | | | |
| 45h | Ch2 DETECT RESISTANCE | RO | 1 | 0000,0000b | Channel 2 Resistance | | | | | | | |
| 46h | Ch3 DETECT RESISTANCE | RO | 1 | 0000,0000b | Channel 3 Resistance | | | | | | | |
| 47h | Ch4 DETECT RESISTANCE | RO | 1 | 0000,0000b | Channel 4 Resistance | | | | | | | |
| 48h-4Bh | RESERVED | RO | 1 | 0000,0000b | Rsvd | | | | | | | |

Table 9-5. Main Registers (continued)

| Cmd Code | Register or Command Name | I ² C R/W | Data Byte | RST State | Bits Description | | | | | | | |
|---|--------------------------|----------------------|-----------|------------|---|---------------------------|--------------------|--------|--------------------------|---------|--------|---------|
| ASSIGNED CHANNEL STATUS | | | | | | | | | | | | |
| 4Ch | ASSIGNED CLASS CHANNEL 1 | RO | 1 | 0000,0000b | Assigned CLASS Channel 1 | | | | Previous CLASS Channel 1 | | | |
| 4Dh | ASSIGNED CLASS CHANNEL 2 | RO | 1 | 0000,0000b | Assigned CLASS Channel 2 | | | | Previous CLASS Channel 2 | | | |
| 4Eh | ASSIGNED CLASS CHANNEL 3 | RO | 1 | 0000,0000b | Assigned CLASS Channel 3 | | | | Previous CLASS Channel 3 | | | |
| 4Fh | ASSIGNED CLASS CHANNEL 4 | RO | 1 | 0000,0000b | Assigned CLASS Channel 4 | | | | Previous CLASS Channel 4 | | | |
| AUTOCLASS CONFIGURATION/MEASUREMENTS | | | | | | | | | | | | |
| 50h | AUTOCLASS CONTROL | R/W | 1 | 0000,0000b | MAC4 | MAC3 | MAC2 | MAC1 | AAC4 | AAC3 | AAC2 | AAC1 |
| 51h | CHANNEL 1 AUTOCLASS PWR | RO | 1 | 0000,0000b | Rsrvd | Channel 1 AutoClass Power | | | | | | |
| 52h | CHANNEL 2 AUTOCLASS PWR | RO | 1 | 0000,0000b | Rsrvd | Channel 2 AutoClass Power | | | | | | |
| 53h | CHANNEL 3 AUTOCLASS PWR | RO | 1 | 0000,0000b | Rsrvd | Channel 3 AutoClass Power | | | | | | |
| 54h | CHANNEL 4 AUTOCLASS PWR | RO | 1 | 0000,0000b | Rsrvd | Channel 4 AutoClass Power | | | | | | |
| MISCELLANEOUS | | | | | | | | | | | | |
| 55h | ALTERNATIVE FOLDBACK | R/W | 1 | 0000,0000b | ALTFB4 | ALTFB3 | ALTFB ₂ | ALTFB1 | ALTIR4 | ALTIR3 | ALTIR2 | ALTIR1 |
| 56h - 5Fh | RESERVED | R/W | 1 | 0000,0000b | Rsrvd | Rsrvd | Rsrvd | Rsrvd | Rsrvd | Rsrvd | Rsrvd | Rsrvd |
| SRAM | | | | | | | | | | | | |
| 60h | SRAM CONTROL | R/W | 1 | 0000,0000b | PROG_SEL | CPU_RST | Rsrvd | PAR_EN | RAM_EN | PAR_SEL | RZ/W | CLR_PTR |
| 61h | SRAM DATA | R/W | - | - | SRAM DATA - Read and Write (continuous) | | | | | | | |
| 62h | START ADDRESS | R/W | 1 | 0000,0000b | Programming Start Address (LSB) | | | | | | | |
| 63h | | R/W | 1 | 0000,0000b | Programming Start Address (MSB) | | | | | | | |
| 64h - 6Fh | RESERVED | R/W | 1 | 0000,0000b | Rsrvd | Rsrvd | Rsrvd | Rsrvd | Rsrvd | Rsrvd | Rsrvd | Rsrvd |

9.6.2 Detailed Register Descriptions

9.6.2.1 INTERRUPT Register

COMMAND = 00h with 1 Data Byte, Read only

Active high, each bit corresponds to a particular event that occurred. Each bit can be individually reset by doing a read at the corresponding event register address, or by setting bit 7 of Reset register.

Any active bit of Interrupt register activates the $\overline{\text{INT}}$ output if its corresponding Mask bit in INTERRUPT Mask register (01h) is set, as well as the INTEN bit in the General Mask register.

Figure 9-8. INTERRUPT Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|-------|--------|-------|------|------|-----|-----|
| SUPF | STRTF | IFAULT | CLASC | DETC | DISF | PGC | PEC |
| R-1 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-6. INTERRUPT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|---|
| 7 | SUPF | R | 1 | Indicates that a Supply Event Fault or SRAM memory fault occurred SUPF = TSD VDUV VDWRN VPUV RAMFLT 1 = At least one Supply Event Fault or SRAM memory fault occurred 0 = No such event occurred |
| 6 | STRTF | R | 0 | Indicates that a t_{START} Fault occurred on at least one channel. STRTF = STRT1 STRT2 STRT3 STRT4 1 = t_{START} Fault occurred for at least one channel 0 = No t_{START} Fault occurred |
| 5 | IFAULT | R | 0 | Indicates that a $t_{\text{OVL D}}$ or t_{LIM} Fault occurred on at least one channel. IFAULT = PCUT1 PCUT2 PCUT3 PCUT4 PCUT34 PCUT12 ILIM1 ILIM2 ILIM3 ILIM4 1 = $t_{\text{OVL D}}$ and/or t_{LIM} Fault occurred for at least one channel 0 = No $t_{\text{OVL D}}$ nor t_{LIM} Fault occurred |
| 4 | CLASC | R | 0 | Indicates that at least one classification cycle occurred on at least one channel CLASC = CLSC1 CLSC2 CLSC3 CLSC4 1 = At least one classification cycle occurred for at least one channel 0 = No classification cycle occurred |
| 3 | DETC | R | 0 | Indicates that at least one detection cycle occurred on at least one channel DETC = DETC1 DETC2 DETC3 DETC4 1 = At least one detection cycle occurred for at least one channel 0 = No detection cycle occurred |
| 2 | DISF | R | 0 | Indicates that a disconnect event occurred on at least one channel. DISF = DISF1 DISF2 DISF3 DISF4 1 = Disconnect event occurred for at least one channel 0 = No disconnect event occurred |
| 1 | PGC | R | 0 | Indicates that a power good status change occurred on at least one channel. PGC = PGC1 PGC2 PGC3 PGC4 1 = Power good status change occurred on at least one channel 0 = No power good status change occurred |

Table 9-6. INTERRUPT Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 0 | PEC | R | 0 | Indicates that a power enable status change occurred on at least one channel PEC = PEC1 PEC2 PEC3 PEC4 1 = Power enable status change occurred on at least one channel 0 = No power enable status change occurred |

9.6.2.2 INTERRUPT MASK Register

COMMAND = 01h with 1 Data Byte, Read/Write

Each bit corresponds to a particular event or fault as defined in the Interrupt register.

Writing a 0 into a bit will mask the corresponding event/fault from activating the $\overline{\text{INT}}$ output.

Note that the bits of the Interrupt register always change state according to events or faults, regardless of the state of the state of the Interrupt Mask register.

Note that the INTEN bit of the General Mask register must also be set in order to allow an event to activate the $\overline{\text{INT}}$ output.

Figure 9-9. INTERRUPT MASK Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| SUMSK | STMSK | IFMSK | CLMSK | DEMSK | DIMSK | PGMSK | PEMSK |
| R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-7. INTERRUPT MASK Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 7 | SUMSK | R/W | 1 | Supply Event Fault mask bit. 1 = Supply Event Fault will activate the $\overline{\text{INT}}$ output. 0 = Supply Event Fault will have no impact on $\overline{\text{INT}}$ output. |
| 6 | STMSK | R/W | 0 | t_{START} Fault mask bit. 1 = t_{START} Fault will activate the $\overline{\text{INT}}$ output. 0 = t_{START} Fault will have no impact on $\overline{\text{INT}}$ output. |
| 5 | IFMSK | R/W | 0 | $t_{\text{OVL D}}$ or t_{LIM} Fault mask bit. 1 = $t_{\text{OVL D}}$ and/or t_{LIM} Fault occurrence will activate the $\overline{\text{INT}}$ output 0 = $t_{\text{OVL D}}$ and/or t_{LIM} Fault occurrence will have no impact on $\overline{\text{INT}}$ output |
| 4 | CLMSK | R/W | 0 | Classification cycle mask bit. 1 = Classification cycle occurrence will activate the $\overline{\text{INT}}$ output. 0 = Classification cycle occurrence will have no impact on $\overline{\text{INT}}$ output. |
| 3 | DEMSK | R/W | 0 | Detection cycle mask bit. 1 = Detection cycle occurrence will activate the $\overline{\text{INT}}$ output. 0 = Detection cycle occurrence will have no impact on $\overline{\text{INT}}$ output. |
| 2 | DIMSK | R/W | 0 | Disconnect event mask bit. 1 = Disconnect event occurrence will activate th $\overline{\text{INT}}$ output. 0 = Disconnect event occurrence will have no impact on $\overline{\text{INT}}$ output. |
| 1 | PGMSK | R/W | 0 | Power good status change mask bit. 1 = Power good status change will activate the $\overline{\text{INT}}$ output. 0 = Power good status change will have no impact on $\overline{\text{INT}}$ output. |
| 0 | PEMSK | R/W | 0 | Power enable status change mask bit. 1 = Power enable status change will activate the $\overline{\text{INT}}$ output. 0 = Power enable status change will have no impact on $\overline{\text{INT}}$ output. |

9.6.2.3 POWER EVENT Register

COMMAND = 02h with 1 Data Byte, Read only

COMMAND = 03h with 1 Data Byte, Clear on Read

Active high, each bit corresponds to a particular event that occurred.

Each bit xxx1-4 represents an individual channel.

A read at each location (02h or 03h) returns the same register data with the exception that the Clear on Read command clears all bits of the register.

If this register is causing the $\overline{\text{INT}}$ pin to be activated, this Clear on Read will release the $\overline{\text{INT}}$ pin.

Any active bit will have an impact on the Interrupt register as indicated in the Interrupt register description.

Figure 9-10. POWER EVENT Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|------|------|------|------|
| PGC4 | PGC3 | PGC2 | PGC1 | PEC4 | PEC3 | PEC2 | PEC1 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 |

LEGEND: R/W = Read/Write; R = Read only; ; CR = Clear on Read, -n = value after reset

Table 9-8. POWER EVENT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|---------|-------|--|
| 7–4 | PGC4–PGC1 | R or CR | 0 | Indicates that a power good status change occurred. 1 = Power good status change occurred 0 = No power good status change occurred |
| 3–0 | PEC4–PEC1 | R or CR | 0 | Indicates that a power enable status change occurred. 1 = Power enable status change occurred 0 = No power enable status change occurred |

Note

For 4-pair wired Ports, the PECn bits will be updated **individually** as status changes for each channel.

For 4-Pair **Single Signature** devices, the PGCn bits will be set only after the status has changed on both channels. This is done to prevent the possible scenario of dual interrupts as the second Channel completes processing shortly after the first.

For 4-Pair **Dual Signature** devices, the PECn and PGCn bits will be set as the status changes on each channel.

9.6.2.4 DETECTION EVENT Register

COMMAND = 04h with 1 Data Byte, Read only

COMMAND = 05h with 1 Data Byte, Clear on Read

Active high, each bit corresponds to a particular event that occurred.

Each bit xxx1-4 represents an individual channel.

A read at each location (04h or 05h) returns the same register data with the exception that the Clear on Read command clears all bits of the register. These bits are cleared when channel-n is turned off.

If this register is causing the $\overline{\text{INT}}$ pin to be activated, this Clear on Read will release the $\overline{\text{INT}}$ pin.

Any active bit will have an impact on the Interrupt register as indicated in the Interrupt register description.

Figure 9-11. DETECTION EVENT Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| CLSC4 | CLSC3 | CLSC2 | CLSC1 | DETC4 | DETC3 | DETC2 | DETC1 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 |

LEGEND: R/W = Read/Write; R = Read only; ; CR = Clear on Read, -n = value after reset

Table 9-9. DETECTION EVENT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|---------|-------|--|
| 7–4 | CLSC4–CLSC1 | R or CR | 0 | Indicates that at least one classification cycle occurred if the CLCHE bit in General Mask register is low. Conversely, it indicates when a change of class occurred if the CLCHE bit is set. 1 = At least one classification cycle occurred (if CLCHE = 0) or a change of class occurred (CLCHE = 1) 0 = No classification cycle occurred (if CLCHE = 0) or no change of class occurred (CLCHE = 1) |
| 3–0 | DETC4–DETC1 | R or CR | 0 | Indicates that at least one detection cycle occurred if the DECHE bit in General Mask register is low. Conversely, it indicates when a change in detection occurred if the DECHE bit is set. 1 = At least one detection cycle occurred (if DECHE = 0) or a change in detection occurred (DECHE = 1) 0 = No detection cycle occurred (if DECHE = 0) or no change in detection occurred (DECHE = 1) |

Note

For 4-Pair operated ports without a pending PWON command, these bits will be set only after the status is ready for **both** channels. This is done to prevent the possible scenario of dual interrupts as the second channel completes processing after the first.

The DETCn bits will only be set concurrently within 5ms of completing detection and connection check on **both** channels

For a 4-pair **single signature** device, the CLSCn bit will only be set for the pair set that classification was completed on even though the requested class will be given for both channels in registers 0x0C-0F.

For a 4-pair **dual signature** device only doing discovery in Semi-auto mode, the CLSCn bits will be set **concurrently** within 5ms of classification being completed on **both** channels. In manual mode, the CLSCn bits will be set **individually** within 5ms of classification being completed on **each** channels.

For 4-pair **dual signature** devices with a pending PWON command or in Auto mode, the DETCn and CLSCn bits will be set independently as each channel completes its portion of discovery during the dual-signature staggered turn on procedure.

9.6.2.5 FAULT EVENT Register

COMMAND = 06h with 1 Data Byte, Read only

COMMAND = 07h with 1 Data Byte, Clear on Read

Active high, each bit corresponds to a particular event that occurred.

Each bit xxx1-4 represents an individual channel.

A read at each location (06h or 07h) returns the same register data with the exception that the Clear on Read command clears all bits of the register. These bits are cleared when channel-n is turned off.

If this register is causing the $\overline{\text{INT}}$ pin to be activated, this Clear on Read will release the $\overline{\text{INT}}$ pin.

Any active bit will have an impact on the Interrupt register as indicated in the Interrupt register description.

Figure 9-12. FAULT EVENT Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| DISF4 | DISF3 | DISF2 | DISF1 | PCUT4 | PCUT3 | PCUT2 | PCUT1 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 |

LEGEND: R/W = Read/Write; R = Read only; ; CR = Clear on Read, -n = value after reset

Table 9-10. FAULT EVENT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|---------|-------|--|
| 7–4 | DISF4–DISF1 | R or CR | 0 | Indicates that a disconnect event occurred. 1 = Disconnect event occurred 0 = No disconnect event occurred |
| 3–0 | PCUT4–PCUT1 | R or CR | 0 | Indicates that a $t_{\text{OVL D}}$ Fault occurred. 1 = $t_{\text{OVL D}}$ Fault occurred 0 = No $t_{\text{OVL D}}$ Fault occurred |

Note

For 4-pair wired ports, the DISFn and PCUTn bits will be updated **individually** as status changes for each channel.

Disconnect events for 4-Pair single signature devices will set **both** corresponding bits, whereas 4-pair dual signature devices will have independent disconnect events per channel.

In the event a singular channel of a 4-pair dual signature device is turned off due to a Disconnect or 2-Pair PCut fault, power may be reapplied to that channel by setting the PWON bit in 0x19h provided the detection and classification are still valid and the Power Allocation settings in 0x29 are sufficient based on the assigned classification of the powered channel.

If PCUT is disabled for a channel, this channel will **not** be automatically turned off during a PCUT fault condition. However, the PCUT fault flag will still be operational, with a fault timeout equal to $t_{\text{OVL D}}$.

Clearing a PCUT event has no impact on the TLIM or TOVLD counters.

9.6.2.6 START/ILIM EVENT Register

COMMAND = 08h with 1 Data Byte, Read only

COMMAND = 09h with 1 Data Byte, Clear on Read

Active high, each bit corresponds to a particular event that occurred.

Each bit xxx1-4 represents an individual channel.

A read at each location (08h or 09h) returns the same register data with the exception that the Clear on Read command clears all bits of the register. These bits are cleared when channel-n is turned off.

If this register is causing the $\overline{\text{INT}}$ pin to be activated, this Clear on Read will release the $\overline{\text{INT}}$ pin.

Any active bit will have an impact on the Interrupt register as indicated in the Interrupt register description.

Figure 9-13. START/ILIM EVENT Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| ILIM4 | ILIM3 | ILIM2 | ILIM1 | STRT4 | STRT3 | STRT2 | STRT1 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 |

LEGEND: R/W = Read/Write; R = Read only; ; CR = Clear on Read, -n = value after reset

Table 9-11. START/ILIM EVENT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|---------|-------|--|
| 7–4 | ILIM4–ILIM1 | R or CR | 0 | Indicates that a t_{LIM} fault occurred, which means the channel has limited its output current to I_{LIM} or the folded back I_{LIM} for more than t_{LIM} . 1 = t_{LIM} fault occurred 0 = No t_{LIM} fault occurred |
| 3–0 | STRT4–STRT1 | R or CR | 0 | Indicates that a t_{START} fault occurred during turn on. 1 = t_{START} fault or class/detect error occurred 0 = No t_{START} fault or class/detect error occurred |

Note

For 4-pair wired Ports:

The ILIMn bits will be updated **individually** as the status changes for each channel.

The STRTn bits will be updated **individually** as the status changes for each channel

When a Start Fault is reported and the PECn bit in Power Event register is set, then there is an Inrush fault.

When a Start Fault is reported and the PECn bit is **not** set, then the Power-On Fault register (0x24h) will indicate the cause of the fault.

In AUTO mode, STRTn faults will not be reported and register 0x24h will not be updated due to invalid discovery results.

In the event a singular channel of a 4-pair dual signature PD is turned off due to a ILIM fault or STRT fault, power may be reapplied to that channel by setting the PWON bit in 0x19h provided the detection and classification are still valid and the Power Allocation settings in 0x29 are sufficient based on the assigned classification of the powered channel.

Inrush Fault (STRTn) Handling on 4-Pair wired ports:

For 4-pair wired ports with single signature PDs connected, the inrush behavior will vary based on assigned classification given during turn on:

For 4P SS PD with an assigned classification of Class 6 or lower:

One channel will go through inrush while the second channel remains idle

If no STRT fault is detected at the end of inrush, the second channel will immediately turn on, and the PGn bits will be set

If a STRT fault **is** detected at the end of inrush, the secondary channel will remain off and the primary will be disabled, and a 1 sec cool-down period will be initiated on **both** channels. Both STRTn bits will be set.

For 4P SS PD with an assigned classification of Class 7 or 8:

Both channels will go through inrush in parallel

If no STRT fault is detected at the end of inrush on either channel, the PGn bits will be set and the port will remain powered.

If a STRT fault **is** detected at the end of inrush on **either** channel, **both** channels will be disabled, and a 1 sec cool-down period will be initiated on both channels. Both STRTn bits will be set.

For 4-pair wired ports with dual signature PDs connected, both channel will operate independent of the other. Each will do perform inrush control during startup and if either channel faults, the remaining channel will be unaffected.

9.6.2.7 SUPPLY and FAULT EVENT Register

COMMAND = 0Ah with 1 Data Byte, Read only

COMMAND = 0Bh with 1 Data Byte, Clear on Read

Active high, each bit corresponds to a particular event that occurred.

A read at each location (0Ah or 0Bh) returns the same register data with the exception that the Clear on Read command clears all bits of the register.

If this register is causing the $\overline{\text{INT}}$ pin to be activated, this Clear on Read will release the $\overline{\text{INT}}$ pin.

Any active bit will have an impact on the Interrupt register as indicated in the Interrupt register description.

Figure 9-14. SUPPLY and FAULT EVENT Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|------|-------|------|--------|--------|------|--------|
| TSD | VDUV | VDWRN | VPUV | PCUT34 | PCUT12 | OSSE | RAMFLT |
| R | R | R | R | R | R | R | R |
| CR | CR | CR | CR | CR | CR | CR | CR |

LEGEND: R/W = Read/Write; R = Read only; ; CR = Clear on Read, -n = value after reset

Table 9-12. SUPPLY and FAULT EVENT Register Field Descriptions

| Bit | Field | Type | POR/R ST | Description |
|-----|--------|---------|-------------|--|
| 7 | TSD | R or CR | 0 / P | Indicates that a thermal shutdown occurred. When there is thermal shutdown, all channels are turned off and are put in OFF mode. The TPS23880 internal circuitry continues to operate however, including the ADCs. Note that as soon as the internal temperature has decreased below the low threshold, the channels can be turned back ON regardless of the status of the TSD bit. 1 = Thermal shutdown occurred 0 = No thermal shutdown occurred |
| 6 | VDUV | R or CR | 1 / P | Indicates that a VDD UVLO occurred. 1 = VDD UVLO occurred 0 = No VDD UVLO occurred |
| 5 | VDWRN | R or CR | 1 / P | Indicates that the VDD has fallen under the UVLO warning threshold. 1 = VDD UV Warning occurred 0 = No VDD UV warning occurred |
| 4 | VPUV | R or CR | 1 / P | Indicates that a VPWR undervoltage occurred. 1 = VPWR undervoltage occurred 0 = No VPWR undervoltage occurred |
| 3 | PCUT34 | R or CR | 0 / 0 | Indicates that a 4-Pair Summed PCUT fault occurred on channels 3 and 4. 1 = 4-Pair Summed PCUT fault occurred on channels 3 and 4 0 = No Summed PCUT fault occurred |
| 2 | PCUT12 | R or CR | 0 / 0 | Indicates that a 4-Pair Summed PCUT fault occurred on channels 1 and 2. 1 = 4-Pair Summed PCUT fault occurred on channels 1 and 2 0 = No Summed PCUT fault occurred |
| 1 | OSSE | R or CR | 0 / 0 | Indicates that an OSS Event occurred 1 = one or more channels with a group of 4 were disabled due to the assertion of the OSS pin or provided 3-bit OSS code 0 = No OSS events occurred |

Table 9-12. SUPPLY and FAULT EVENT Register Field Descriptions (continued)

| Bit | Field | Type | POR/R ST | Description |
|-----|--------|---------|-------------|---|
| 0 | RAMFLT | R or CR | 0 / 0 | Indicates that a SRAM fault has occurred 1 = SRAM fault occurred 0 = No SRAM fault occurred |

Note

The RST condition of "P" indicates that the previous state of these bits will be preserved following a device reset using the $\overline{\text{RESET}}$ pin. Thus, pulling the $\overline{\text{RESET}}$ input low will not clear the TSD, VDUV, VDWRN, or VPUV bits.

Note

While the VPUV bit is set, any PWONn commands will be ignored until $V_{\text{VPWR}} > 30 \text{ V}$.

During VPUV undervoltage condition, the Detection Event register (CLSCn, DETCn) is not cleared, unless VPWR also falls below the VPWR UVLO falling threshold (approximately 18 V).

A clear on Read will not effectively clear VDUV bit as long as the VPWR undervoltage condition is maintained.

Note

In 1-bit mode (MbitPrty = 0 in reg 0x17), the OSSE bit will be set anytime a channel within a group of 4 has OSS enabled and the OSS pin is asserted.

In 3-bit mode (MbitPrty = 1 in reg 0x17), the OSSE bit will be set anytime a 3-bit priority code is sent that is equal to or greater than the MBPn settings in registers 0x27 and 0x28 channel for a group of 4 channels.

For a 4-pair wired port, if 4P PCUT is disabled (4PPCTxx = 0 in 0x2D), the port will not be automatically turned off during a 4P-PCUT fault condition. However, the PCUTnn fault bits will still be operational, with a fault timeout equal to t_{OVLd} . Also, if a Clear on Read is done at the Fault Event register, the PCUTnn bit is reset, and the associated summed PCUT counter is reset. Only the Channels reporting such interrupt have their counter cleared by the CoR operation. Also, clearing a PCUT fault has no impact on TLIM counter.

9.6.2.7.1 Detected SRAM Faults and "Safe Mode"

The TPS23880 is configured with internal SRAM memory fault monitoring, and in the event that an error is detected with the SRAM memory, the device will enter "safe mode". While in "Safe mode" the FW Revision value in register 0x41 will be set to 0xFFh.

Any channels that are currently powered will remain powered, but the majority of the operation will be disabled until the SRAM can be reloaded. The device UVLO and Thermal Shutdown features in addition to the disconnect and current foldback functions for the powered channels will be preserved in "safe mode".

Any channels that were not powered prior to the SRAM fault detection will be set to OFF mode (see register 0x12h description for additional changes that will occur as a result of the change to OFF mode). Port Remapping (0x26h) and any other channel configuration settings (ie Power Allocation 0x29h) will be preserved.

Upon detection of a SRAM fault the "RAM_EN" bit in 0x60 will be cleared and the RAMFLT bit will be set in register 0x0A. The internal firmware will continue to run in "safe mode" until this bit is set again by the host after the SRAM is reloaded or a POR (Power on Reset) event occurs. In order to ensure a smooth transition into and out of "safe mode", any I2C commands other than those to reprogram the SRAM need to be deferred until after the SRAM is reloaded and determined to be "valid" (see register 0x60 SRAM programming descriptions).

Note

Once set, the RAMFLT bit will remain set even after the device is removed from safe mode. it is recommend that this bit be cleared prior to setting the RAM_EN bit in register 0x60 following the SRAM reload.

Note

The PAR_EN bit in reg 0x60 must be set and the corresponding SRAM_Parity code (available for download from the [TI mySecure Software](#) webpage) must be loaded into the device in order for the SRAM fault monitoring to be active.

Please refer to the [How to Load TPS2388x SRAM Code](#) document for more information on the recommended SRAM programming procedure.

9.6.2.8 CHANNEL 1 DISCOVERY Register

COMMAND = 0Ch with 1 Data Byte, Read Only

Figure 9-15. CHANNEL 1 DISCOVERY Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------------|-----|-----|-----|------------|-----|-----|-----|
| REQUESTED CLASS Ch1 | | | | DETECT Ch1 | | | |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.6.2.9 CHANNEL 2 DISCOVERY Register

COMMAND = 0Dh with 1 Data Byte, Read Only

Figure 9-16. CHANNEL 2 DISCOVERY Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------------|-----|-----|-----|------------|-----|-----|-----|
| REQUESTED CLASS Ch2 | | | | DETECT Ch2 | | | |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.6.2.10 CHANNEL 3 DISCOVERY Register

COMMAND = 0Eh with 1 Data Byte, Read Only

Figure 9-17. CHANNEL 3 DISCOVERY Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------------|-----|-----|-----|------------|-----|-----|-----|
| REQUESTED CLASS Ch3 | | | | DETECT Ch3 | | | |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.6.2.11 CHANNEL 4 DISCOVERY Register

COMMAND = 0Fh with 1 Data Byte, Read Only

Figure 9-18. CHANNEL 4 DISCOVERY Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------------|-----|-----|-----|------------|-----|-----|-----|
| REQUESTED CLASS Ch4 | | | | DETECT Ch4 | | | |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Bit Descriptions: These bits represent the most recent **"requested"** classification and detection results for channel n. These bits are cleared when channel n is turned off.

Table 9-13. CHANNEL n DISCOVERY Register Field Descriptions

| Bit | Field | Type | Reset | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------|-------------|------|-------|--|-------------|--|--|--|------------------|---|---|---|---|---------|---|---|---|---|---------------|---|---|---|---|----------|---|---|---|---|---------|---|---|---|---|---------|---|---|---|---|----------------------------|---|---|---|---|--------------|---|---|---|---|-------------------|---|---|---|---|-----------------------------------|---|---|---|---|-----------------------------------|---|---|---|---|-----------------------------------|---|---|---|---|-----------------------------------|---|---|---|---|---------------------------|---|---|---|---|---------------------------------|---|---|---|---|----------|---|---|---|---|----------------|
| 7-4 | RCLASS Ch-n | R | 0 | <p>Most recent classification result on channel n. The selection is as following:</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th colspan="4">RCLASS Ch-n</th> <th>Requested Class</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Unknown</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Class 1</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>Class 2</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Class 3</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Class 4</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Reserved – read as Class 0</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Class 0</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Class Overcurrent</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Class 5 - 4-Pair Single Signature</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Class 6 - 4-Pair Single Signature</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>Class 7 - 4-Pair Single Signature</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>Class 8 - 4-Pair Single Signature</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>Class 4+ - Type-1 Limited</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>Class 5 - 4-Pair Dual Signature</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>Reserved</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Class Mismatch</td></tr> </tbody> </table> | RCLASS Ch-n | | | | Requested Class | 0 | 0 | 0 | 0 | Unknown | 0 | 0 | 0 | 1 | Class 1 | 0 | 0 | 1 | 0 | Class 2 | 0 | 0 | 1 | 1 | Class 3 | 0 | 1 | 0 | 0 | Class 4 | 0 | 1 | 0 | 1 | Reserved – read as Class 0 | 0 | 1 | 1 | 0 | Class 0 | 0 | 1 | 1 | 1 | Class Overcurrent | 1 | 0 | 0 | 0 | Class 5 - 4-Pair Single Signature | 1 | 0 | 0 | 1 | Class 6 - 4-Pair Single Signature | 1 | 0 | 1 | 0 | Class 7 - 4-Pair Single Signature | 1 | 0 | 1 | 1 | Class 8 - 4-Pair Single Signature | 1 | 1 | 0 | 0 | Class 4+ - Type-1 Limited | 1 | 1 | 0 | 1 | Class 5 - 4-Pair Dual Signature | 1 | 1 | 1 | 0 | Reserved | 1 | 1 | 1 | 1 | Class Mismatch |
| RCLASS Ch-n | | | | Requested Class | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | Unknown | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1 | Class 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 0 | Class 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1 | Class 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 0 | Class 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 1 | Reserved – read as Class 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 0 | Class 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 1 | Class Overcurrent | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | Class 5 - 4-Pair Single Signature | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 1 | Class 6 - 4-Pair Single Signature | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 0 | Class 7 - 4-Pair Single Signature | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 1 | Class 8 - 4-Pair Single Signature | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 0 | Class 4+ - Type-1 Limited | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 1 | Class 5 - 4-Pair Dual Signature | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 0 | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | Class Mismatch | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 3-0 | DETECT Ch-n | R | 0 | <p>Most recent detection result on channel n. The selection is as following:</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th colspan="4">DETECT Ch-n</th> <th>Detection Status</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Unknown</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Short-circuit</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>Reserved</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Too Low</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Valid</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Too High</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Open Circuit</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>MOSFET fault</td></tr> </tbody> </table> | DETECT Ch-n | | | | Detection Status | 0 | 0 | 0 | 0 | Unknown | 0 | 0 | 0 | 1 | Short-circuit | 0 | 0 | 1 | 0 | Reserved | 0 | 0 | 1 | 1 | Too Low | 0 | 1 | 0 | 0 | Valid | 0 | 1 | 0 | 1 | Too High | 0 | 1 | 1 | 0 | Open Circuit | 0 | 1 | 1 | 1 | Reserved | 1 | 1 | 1 | 0 | MOSFET fault | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| DETECT Ch-n | | | | Detection Status | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | Unknown | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1 | Short-circuit | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 0 | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 1 | Too Low | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 0 | Valid | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 1 | Too High | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 0 | Open Circuit | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 1 | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 0 | MOSFET fault | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

“Requested” vs. “Assigned” Classification: The “requested” class is the classification the PSE measures during Mutual Identification prior to turn on, whereas the “assigned” class is the classification level the channel was powered on with based on the Power Allocation setting in register 0x29h. The “assigned” classification values are available in registers 0x4C-4F

Note

Due to the need to power on after 1 class finger, the "Class 4+ - Type 1 Limited" Requested Class is reported anytime a Class 4 or higher PD is powered with register 0x29 configured for 15.5W.

Upon being powered, devices that present a class 0 signature during discovery will be given an assigned class of "Class 3"

9.6.2.12 POWER STATUS Register

COMMAND = 10h with 1 Data Byte, Read only

Each bit represents the actual power status of a channel.

Each bit xx1-4 represents an individual channel.

These bits are cleared when channel-n is turned off, including if the turn off is caused by a fault condition.

Figure 9-19. POWER STATUS Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|-----|-----|-----|-----|-----|-----|-----|
| PG4 | PG3 | PG2 | PG1 | PE4 | PE3 | PE2 | PE1 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-14. POWER STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|--|
| 7–4 | PG4–PG1 | R | 0 | Each bit, when at 1, indicates that the channel is on and that the voltage at DRAINn pin has gone below the power good threshold during turn on. These bits are latched high once the turn on is complete and can only be cleared when the channel is turned off or at RESET/POR. 1 = Power is good 0 = Power is not good |
| 3–0 | PE4–PE1 | R | 0 | Each bit indicates the ON/OFF state of the corresponding channel. 1 = Channel is on 0 = Channel is off |

For 4-pair wired ports, these bits will be updated individually as the status changes for each channel

For 4-Pair Single Signature devices, the PGN bits will be set only after the status has changed on both channels. This is done to prevent the possible scenario of dual interrupts as the second channel completes processing after the first.

For 4-Pair Dual Signature devices, the PECn and PGCn bits will be set as the status changes on each channel.

9.6.2.13 PIN STATUS Register

COMMAND = 11h with 1 Data Byte, Read Only

Figure 9-20. PIN STATUS Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|--------|--------|--------|--------|--------------------|---|---|
| 0 | SLA4 | SLA3 | SLA2 | SLA1 | SLA0 | 0 | 0 |
| 0 | A4 pin | A3 pin | A2 pin | A1 pin | 0/1 ⁽¹⁾ | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

(1) If Configuration A, it can be 0 or 1. If configuration B, it is 0.

Table 9-15. PIN STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|--------|-----------|------|-----------|---|
| 6-3 | SLA4-SLA1 | R | See above | I ² C device address, as defined while using pins A4-A1. |
| 2 | SLA0 | R | | SLA0 bit is internally defined to 0 or 1 0 = Channel 1-4 1 = Channels 5-8 |
| 7, 1-0 | - | R | | Reserved |

| DESCRIPTION | BINARY DEVICE ADDRESS | | | | | | | ADDRESS PINS | | | |
|------------------|-----------------------|---|---|---|---|---|-----|--------------|------|------|------|
| | 6 | 5 | 4 | 3 | 2 | 1 | 0 | A4 | A3 | A2 | A1 |
| Broadcast access | 1 | 1 | 1 | 1 | 1 | 1 | 1 | X | X | X | X |
| Slave 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0/1 | GND | GND | GND | GND |
| | 0 | 1 | 0 | 0 | 0 | 1 | 0/1 | GND | GND | GND | HIGH |
| | 0 | 1 | 0 | 0 | 1 | 0 | 0/1 | GND | GND | HIGH | GND |
| | 0 | 1 | 0 | 0 | 1 | 1 | 0/1 | GND | GND | HIGH | HIGH |
| | 0 | 1 | 0 | 1 | 0 | 0 | 0/1 | GND | HIGH | GND | GND |
| | 0 | 1 | 0 | 1 | 0 | 1 | 0/1 | GND | HIGH | GND | HIGH |
| | 0 | 1 | 0 | 1 | 1 | 0 | 0/1 | GND | HIGH | HIGH | GND |
| | 0 | 1 | 0 | 1 | 1 | 1 | 0/1 | GND | HIGH | HIGH | HIGH |
| | 0 | 1 | 1 | 0 | 0 | 0 | 0/1 | HIGH | GND | GND | GND |
| | 0 | 1 | 1 | 0 | 0 | 1 | 0/1 | HIGH | GND | GND | HIGH |
| | 0 | 1 | 1 | 0 | 1 | 0 | 0/1 | HIGH | GND | HIGH | GND |
| | 0 | 1 | 1 | 0 | 1 | 1 | 0/1 | HIGH | GND | HIGH | HIGH |
| | 0 | 1 | 1 | 1 | 0 | 0 | 0/1 | HIGH | HIGH | GND | GND |
| | 0 | 1 | 1 | 1 | 0 | 1 | 0/1 | HIGH | HIGH | GND | HIGH |
| | 0 | 1 | 1 | 1 | 1 | 0 | 0/1 | HIGH | HIGH | HIGH | GND |
| Slave 15 | 0 | 1 | 1 | 1 | 1 | 1 | 0/1 | HIGH | HIGH | HIGH | HIGH |

9.6.2.14 OPERATING MODE Register

COMMAND = 12h with 1 Data Byte, Read/Write

Figure 9-21. OPERATING MODE Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| C4M1 | C4M0 | C3M1 | C3M0 | C2M1 | C2M0 | C1M1 | C1M0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-16. OPERATING MODE Register Field Descriptions

| Bit | Field | Type | Reset | Description | | | | | | | | | | | | | | | |
|-----|-----------|-------------------|-------|--|----|----|----------------|---|---|-----|---|---|-------------------|---|---|----------|---|---|------|
| 7-0 | CnM1–CnM0 | R/W | 0 | <p>Each pair of bits configures the operating mode per channel. The selection is as following:</p> <table border="1"> <thead> <tr> <th>M1</th> <th>M0</th> <th>Operating Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>OFF</td> </tr> <tr> <td>0</td> <td>1</td> <td>Diagnostic/Manual</td> </tr> <tr> <td>1</td> <td>0</td> <td>Semiauto</td> </tr> <tr> <td>1</td> <td>1</td> <td>Auto</td> </tr> </tbody> </table> <p>For a 4-pair wired port, both channels must be set to the same operating mode. Otherwise, the port will not conduct discovery, and any turn on commands will be ignored.</p> | M1 | M0 | Operating Mode | 0 | 0 | OFF | 0 | 1 | Diagnostic/Manual | 1 | 0 | Semiauto | 1 | 1 | Auto |
| M1 | M0 | Operating Mode | | | | | | | | | | | | | | | | | |
| 0 | 0 | OFF | | | | | | | | | | | | | | | | | |
| 0 | 1 | Diagnostic/Manual | | | | | | | | | | | | | | | | | |
| 1 | 0 | Semiauto | | | | | | | | | | | | | | | | | |
| 1 | 1 | Auto | | | | | | | | | | | | | | | | | |

OFF MODE:

In OFF mode, the Channel is OFF and neither detection nor classification is performed independent of the DETE, CLSE or PWON bits.

The table below depicts what bits will be cleared when a channel is changed to OFF mode from any other operating mode:

Table 9-17. Transition to OFF Mode

| Register | Bits to be reset |
|-----------|--|
| 0x04 | CLSCn and DETCn |
| 0x06 | DISFn and PCUTn |
| 0x08 | STRTn and ILIMn |
| 0x0A/B | PCUTnn |
| 0x0C-0F | Requested Class and Detection |
| 0x10 | PGn and PEn |
| 0x14 | CLEn and DETEn |
| 0x1C | ACn and CCnn |
| 0x1E-21 | 2P Policing set to 0xFFh |
| 0x24 | PFn |
| 0x2A-2B | 4P Policing set to 0xFFh |
| 0x2D | NLMnn, NCTnn, 4PPCTnn, and DCDTnn |
| 0x30-3F | Channel Voltage and Current Measurements |
| 0x40 | 2xFBn |
| 0x44 - 47 | Detection Resistance Measurements |
| 0x4C-4F | Assigned Class and Previous Class |
| 0x51-54 | Autoclass Measurement |

Note

it may take upwards of 5 ms before all of the registers are cleared following a change to OFF mode.

Only the bits associated with the channel/port ("n") being set into OFF mode will be cleared. Those bits associated with channels/ports remaining in operation will not be changed.

In the event either the PGn or PEn bits were changed from a 1 to a zero, the corresponding PGCn and PECn bits will be set in the POWER EVENT register 0x02h.

Also, a change of mode from semiauto to manual/diagnostic mode or OFF mode will cancel any ongoing cooldown time period.

DIAGNOSTIC/MANUAL MODE:

In Manual/Diagnostic mode, there is no automatic state change. The channel remains idle until DETE, CLSE (0x14h or 0x18h), or PWON command is provided. Upon the setting of the DETE and/or CLSE bits, the channel will perform a singular detection and/or classification cycle on the corresponding channel.

Note

Setting a PWONn bit in register 0x19 results in the immediate turn on of that channel.

There is no Assigned Class assigned for ports/channels powered out of Manual/Diagnostic mode. Any settings such as the port power policing and 1x/2x foldback selection that are typically configured based on the assigned class result need to be manually configured by the user.

For 4-Pair wired ports (4PWnn bit in 0x29 = 1):

Setting the DETE or CLSE bits on only one channel will result in detection and/or classification only being done on that channel, and Connection Check will not be performed.

Setting the DETE bits for **both** channels during the same I²C operation will result in detection cycles being completed on both channels, and if the detection results are valid, connection check will also be completed.

Setting the CLSE bits for **both** channels during the same I²C operation will result in staggered classification measurements being done on both channels

Note

Setting a PWONn bit in register 0x19 results in the immediate turn on of that channel.

Note

DC Disconnect for 4-Pair ports power on in Manual/Diagnostic mode will behave as independent channels. Thus, if either channel current falls below V_{IMIN} for longer than t_{MPDO} , that channel will be disabled and a disconnect fault will be set (DISFn bits in register 0x06/7).

SEMI AUTO MODE:

In Semi Auto mode, as long as the Channel is unpowered, detection and classifications may be performed continuously depending if the corresponding class and detect enable bits are set (register 0x14h).

Table 9-18. Channel Behavior in Semi Auto Mode

| CLEn | DETN | Channel Operation |
|------|------|---|
| 0 | 0 | Idle |
| 0 | 1 | Cycling Detection Measurements only |
| 1 | 0 | Idle |
| 1 | 1 | Cycling Detection and Classification Measurements |

Note

If two channels are configured as a 4-pair wired port, a connection check measurement will be performed once a valid detection result is seen on one of the channel

For a 4-Pair Dual Signature PD that has only one channel powered, the unpowered channel will resume detect and class provided the DETE and CLE bits are set for that channel in 0x14h.

AUTO MODE:

In **Auto mode**, channels will automatically power on any valid detection and classification signature based on the Port Power Allocation settings in 0x29. The channels will remain idle until DETE and CLSE (0x14 or 0x18) are set, or a PWON command is given.

Prior to setting DETE and CLE or sending a PWON command in AUTO mode, the following registers need to be configured according to the system requirements and configuration:

| Register | Bits |
|----------|--|
| 0x26 | Port Re-mapping |
| 0x29 | 4-Pair Wired and Port Power Allocation |
| 0x50 | Auto AC Enable |
| 0x55 | Alternative Inrush and Powered Foldback Enable |

Note

Changes to these registers after the DETE and CLE bits are set in Auto mode may result in undesired or non IEEE complaint operation.

The following registers may be configured or changed after turn on if changes to the default operation are desired as these values are internally set during power on based on the port configuration and resulting assigned PD class:

| Register | Bits |
|----------|---|
| 0x1E-21 | 2-Pair Policing |
| 0x2A-2B | 4-Pair Policing |
| 0x2D | 4P Pcut Enable and DC Disconnect Threshold bits |
| 0x40 | 2x Foldback Enable |

9.6.2.15 DISCONNECT ENABLE Register

COMMAND = 13h with 1 Data Byte, Read/Write

Bit Descriptions: Defines the disconnect detection mechanism for each channel.

Figure 9-22. DISCONNECT ENABLE Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| – | – | – | – | DCDE4 | DCDE3 | DCDE2 | DCDE1 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-19. DISCONNECT ENABLE Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|--|
| 7–4 | — | R/W | 0 | |
| 3–0 | DCDE4–DCDE1 | R/W | 1 | DC disconnect enable 1 = DC Disconnect Enabled 0 = DC Disconnect Disabled Look at the TIMING CONFIGURATION register for more details on how to define the TDIS time period. |

DC disconnect consists in measuring the Channel DC current at SENn, starting a timer (T_{DIS}) if this current is below a threshold and turning the Channel off if a time-out occurs. Also, the corresponding disconnect bit (DISFn) in the FAULT EVENT register is set accordingly. The T_{DIS} counter is reset each time the current rises above the disconnect threshold for at least 3 msec. The counter does not decrement below zero.

Note

For 4P Single signature devices, if either DCDEx bit is set, both channels will be shut off when the disconnect timer expires.

In the event a singular channel of a 4-pair dual signature PD is turned off due to a disconnect fault or other reason, power may be reapplied to that channel by setting the PWON bit in 0x19h provided the detection and classification are still valid and the Power Allocation settings in 0x29 are sufficient based on the assigned classification of the powered channel.

Note

The DCDTnn bits in 0x2D set the disconnect threshold.

The DCDTnn bits are automatically configured during turn on based on the 4PWnn bits in 0x29 and the Assigned classification results (0x4C-4F) based on IEEE compliance requirements.

9.6.2.16 DETECT/CLASS ENABLE Register

COMMAND = 14h with 1 Data Byte, Read/Write

During t_{OVLD} , t_{LIM} or t_{START} cool down cycle, any Detect/Class Enable command for that channel will be delayed until end of cool-down period. Note that at the end of cool down cycle, one or more detection/class cycles are automatically restarted as described previously, if the class and/or detect enable bits are set.

Figure 9-23. DETECT/CLASS ENABLE Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| CLE4 | CLE3 | CLE2 | CLE1 | DETE4 | DETE3 | DETE2 | DETE1 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-20. DETECT/CLASS ENABLE Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|-----------------------------|
| 7-4 | CLE4-CLE1 | R/W | 0 | Classification enable bits. |
| 3-0 | DETE4-DETE1 | R/W | 0 | Detection enable bits. |

Bit Descriptions:

Detection and classification enable for each channel.

When in Manual mode, setting a bit means that only one cycle (detection or classification) is performed for the corresponding channel. The bit is automatically cleared by the time the cycle has been completed.

Note that similar result can be obtained by writing to the Detect/Class Restart register 0x18.

It is also cleared if a turn off (Power Enable register) command is issued.

When in semiauto mode, as long as the port is kept off, detection and classification are performed continuously, as long as the class and detect enable bits are kept set, but the class will be done only if the detection was valid. A Detect/Class Restart PB command can also be used to set the CLEn and DETEn bits, if in semiauto mode.

Note

For 4-pair wired Ports in Semi-Auto or Auto mode, **both** DETEn and CLEn bits need to be set on **both** channels in order for Detection or Classification to be enabled

Note

In Manual/Diagnostic mode, it is recommended that a Port Reset command (see register 0x1A [Section 9.6.2.22](#)) be completed prior to enabling discovery (DETEn or CLEn).

9.6.2.17 Power Priority / 2Pair PCUT Disable Register Name

COMMAND = 15h with 1 Data Byte, R/W

Figure 9-24. Power Priority / 2P-PCUT Disable Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| OSS4 | OSS3 | OSS2 | OSS1 | DCUT4 | DCUT3 | DCUT2 | DCUT1 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-21. Power Priority / 2P-PCUT Disable Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|--|
| 7–4 | OSS4-OSS1 | R/W | 0 | <p>Power priority bits:</p> <p>When the MBitPrty bit in 0x17 =0:</p> <p>1 = When the OSS signal is asserted, the corresponding channel is powered off.</p> <p>0 = OSS signal has no impact on the channel.</p> <p>For 4-pair wired Ports, these bits control the individual Channel response. In order for both channels of a 4-pair wired port to be disabled, both channels need to be set to 1.</p> |
| 3–0 | DCUT4-DCUT1 | R/W | 0 | <p>2-Pair PCUT disable for each channel. Used to prevent removal of the associated channel's power due to a 2-Pair PCUT fault, regardless of the programming status of the Timing Configuration register. Note that there is still monitoring of ILIM faults.</p> <p>1: Channel's PCUT is disabled. This means that an PCUT fault alone will not turn off this channel.</p> <p>0: Channel's PCUT is enabled. This enables channel turn off if there is PCUT fault.</p> |

Note

If the MbitPrty bit = 1 (0x17h): The OSSn bits must be cleared to ensure proper operation. Refer to registers 0x27/28h for more information on the Multi-bit priority shutdown feature.

Note

If DCUT = 1 for a channel, the channel will not be automatically turned off during a PCUT fault condition. However, the PCUT fault flag will still be operational, with a fault timeout equal to $t_{OVL D}$.

Any change in the state of DCUTn bits will result in the resetting of the $T_{OVL D}$ timer for that channel.

Note

For 4-pair wired Ports:

These bits control the **individual** Channel response to a 2-Pair PCUT fault.

If the NCTnn bit in 0x2D = 1 and the 2-Pair PCut is enabled, **both** channel will be turned off if the overload condition exceeds the $t_{OVL D}$ timeout.

The response to a summed 4-pair PCUT fault is configured in register 0x2Dh.

The OSSn bits are used to determine which channels are shut down in response to an external assertion of the OSS fast shutdown signal.

The turn off procedure due to OSS is similar to a channel reset or change to OFF mode, with the exception that OSS does not cancel any ongoing fault cool down timers. the table below includes the bits that will be cleared when a channel is disabled due to OSS:

Table 9-22. Channel Turn Off with OSS

| Register | Bits to be reset |
|-----------|--|
| 0x04 | CLSCn and DETCn |
| 0x06 | DISFn and PCUTn |
| 0x08 | STRn and ILIMn |
| 0x0A/B | PCUTnn |
| 0x0C-0F | Requested Class and Detection |
| 0x10 | PGn and PEn |
| 0x14 | CLEn and DETEn |
| 0x1C | ACn and CCnn |
| 0x1E-21 | 2P Policing set to 0xFFh |
| 0x24 | PFn |
| 0x2A-2B | 4P Policing set to 0xFFh |
| 0x2D | NLMnn, NCTnn, 4PPCTnn, and DCdTnn |
| 0x30-3F | Channel Voltage and Current Measurements |
| 0x40 | 2xFBn |
| 0x44 - 47 | Detection Resistance Measurements |
| 0x4C-4F | Assigned Class and Previous Class |
| 0x51-54 | Autoclass Measurement |

Note

it may take upwards of 5 ms before all of the registers are cleared following an OSS event.

Only the bits associated with the channel/port ("n") with OSS enabled will be cleared. Those bits associated with channels/ports remaining in operation will not be changed.

In the event a singular channel of a 4-pair dual signature PD is turned off due to OSS or PCUT fault, power may be reapplied to that channel by setting the PWON bit in 0x19h provided the detection and classification are still valid and the Power Allocation settings in 0x29 are sufficient based on the assigned classification of the powered channel.

9.6.2.18 TIMING CONFIGURATION Register

COMMAND = 16h with 1 Data Byte, Read/Write

Bit Descriptions: These bits define the timing configuration for **all four** channels.

Figure 9-25. TIMING CONFIGURATION Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|--------|-------|-------|-------|-------|-------|
| TLIM | | TSTART | | TOVLD | | TMPDO | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-23. TIMING CONFIGURATION Register Field Descriptions

| Bit | Field | Type | Reset | Description | | | | | | | | | | |
|--------|---------------------------|------|-------|---|--------|--------------------------|-----|----|-----|----|-----|-----|-----|----------|
| 7–6 | TLIM | R/W | 0 | <p>ILIM fault timing, which is the output current limit time duration before channel turn off. When a 2xFBn bit in register 0x40 = 0, the t_{LIM} used for the associated channel is always the nominal value (about 60 ms).</p> <p>This timer is active and increments to the settings defined below after expiration of the TSTART time window and when the channel is limiting its output current to I_{LIM}. If the ILIM counter is allowed to reach the programmed time-out duration specified below, the channel will be powered off. The 1-second cool down timer is then started, and the channel can not be turned-on until the counter has reached completion.</p> <p>In other circumstances (ILIM time-out has not been reached), while the channel current is below I_{LIM}, the same counter decrements at a rate 1/16th of the increment rate. The counter does not decrement below zero. The ILIM counter is also cleared in the event of a turn off due to a Power Enable or Reset command, a DC disconnect event or the OSS input.</p> <p>Note that in the event the TLIM setting is changed while this timer is already active for a channel, this timer is automatically reset then restarted with the new programmed time-out duration.</p> <p>Note that at the end of cool down cycle, when in semiauto mode, a detection cycle is automatically restarted if the detect enable bit is set. Also note that the cool down time count is immediately canceled with a reset command, or if the OFF or Manual mode is selected.</p> <p>If 2xFBn bit is asserted in register 0x40, then t_{LIM} for associated channel is programmable with the following selection:</p> <table border="1"> <thead> <tr> <th>TLIM</th> <th>Minimum t_{LIM} (ms)</th> </tr> </thead> <tbody> <tr> <td>0 0</td> <td>58</td> </tr> <tr> <td>0 1</td> <td>15</td> </tr> <tr> <td>1 0</td> <td>10</td> </tr> <tr> <td>1 1</td> <td>6</td> </tr> </tbody> </table> | TLIM | Minimum t_{LIM} (ms) | 0 0 | 58 | 0 1 | 15 | 1 0 | 10 | 1 1 | 6 |
| TLIM | Minimum t_{LIM} (ms) | | | | | | | | | | | | | |
| 0 0 | 58 | | | | | | | | | | | | | |
| 0 1 | 15 | | | | | | | | | | | | | |
| 1 0 | 10 | | | | | | | | | | | | | |
| 1 1 | 6 | | | | | | | | | | | | | |
| 5-4 | TSTART (or TINRUSH) | R/W | 0 | <p>START fault timing, which is the maximum allowed overcurrent time during inrush. If at the end of TSTART period the current is still limited to I_{Inrush}, the channel is powered off.</p> <p>This is followed by a 1-second cool down period, during which the channel can not be turned-on</p> <p>Note that at the end of cool down cycle, when in semiauto mode, a detection cycle is automatically restarted if the class and detect enable bits are set.</p> <p>Note that in the event the TSTART setting is changed while this timer is already active for a channel, this new setting is ignored and will be applied only next time the channel is turned ON.</p> <p>The selection is as following:</p> <table border="1"> <thead> <tr> <th>TSTART</th> <th>Nominal t_{START} (ms)</th> </tr> </thead> <tbody> <tr> <td>0 0</td> <td>60</td> </tr> <tr> <td>0 1</td> <td>30</td> </tr> <tr> <td>1 0</td> <td>120</td> </tr> <tr> <td>1 1</td> <td>Reserved</td> </tr> </tbody> </table> | TSTART | Nominal t_{START} (ms) | 0 0 | 60 | 0 1 | 30 | 1 0 | 120 | 1 1 | Reserved |
| TSTART | Nominal t_{START} (ms) | | | | | | | | | | | | | |
| 0 0 | 60 | | | | | | | | | | | | | |
| 0 1 | 30 | | | | | | | | | | | | | |
| 1 0 | 120 | | | | | | | | | | | | | |
| 1 1 | Reserved | | | | | | | | | | | | | |

Table 9-23. TIMING CONFIGURATION Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description | | | | | | | | | | | | | | | |
|-------|-------|-------------------------|-------|--|-------|--|-------------------------|---|---|-----|---|---|----|---|---|-----|---|---|-----|
| 3–2 | TOVLD | R/W | 0 | <p>PCUT fault timing, which is the overcurrent time duration before turn off. This timer is active and increments to the settings defined below after expiration of the TSTART time window and when the current meets or exceeds P_{CUT}, or when it is limited by the current foldback. If the PCUT counter is allowed to reach the programmed time-out duration specified below, the channel will be powered off. The 1-second cool down timer is then started, and the channel can not be turned-on until the counter has reached completion.</p> <p>In other circumstances (PCUT time-out has not been reached), while the current is below P_{CUT}, the same counter decrements at a rate 1/16th of the increment rate. The counter does not decrement below zero. The PCUT counter is also cleared in the event of a turn off due to a Power Enable or Reset command, a DC disconnect event or the OSS input</p> <p>Note that in the event the TOVLD setting is changed while this timer is already active for a channel, this timer is automatically reset then restarted with the new programmed time-out duration.</p> <p>Note that at the end of cool down cycle, when in semiauto mode, a detection cycle is automatically restarted if the detect enable bit is set. Also note that the cool down time count is immediately canceled with a reset command, or if the OFF or Manual mode is selected.</p> <p>Note that if a DCUTn bit is high in the Power Priority/PCUT Disable register, the PCUT fault timing for the associated channel is still active. However, even though the channel will not be turned off when the tOVLD time expires, the PCUT fault bits will still be set.</p> <p>The selection is as following:</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="2">TOVLD</th> <th>Nominal t_{OVLD} (ms)</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>60</td> </tr> <tr> <td>0</td> <td>1</td> <td>30</td> </tr> <tr> <td>1</td> <td>0</td> <td>120</td> </tr> <tr> <td>1</td> <td>1</td> <td>240</td> </tr> </tbody> </table> | TOVLD | | Nominal t_{OVLD} (ms) | 0 | 0 | 60 | 0 | 1 | 30 | 1 | 0 | 120 | 1 | 1 | 240 |
| TOVLD | | Nominal t_{OVLD} (ms) | | | | | | | | | | | | | | | | | |
| 0 | 0 | 60 | | | | | | | | | | | | | | | | | |
| 0 | 1 | 30 | | | | | | | | | | | | | | | | | |
| 1 | 0 | 120 | | | | | | | | | | | | | | | | | |
| 1 | 1 | 240 | | | | | | | | | | | | | | | | | |
| 1–0 | TMPDO | R/W | 0 | <p>Disconnect delay, which is the time to turn off a channel once there is a disconnect condition, and if the dc disconnect detect method has been enabled.</p> <p>The TDIS counter is reset each time the current goes continuously higher than the disconnect threshold for nominally 15 ms.</p> <p>The counter does not decrement below zero.</p> <p>The selection is as following:</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="2">TMPDO</th> <th>Nominal t_{MPDO} (ms)</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>360</td> </tr> <tr> <td>0</td> <td>1</td> <td>90</td> </tr> <tr> <td>1</td> <td>0</td> <td>180</td> </tr> <tr> <td>1</td> <td>1</td> <td>180</td> </tr> </tbody> </table> | TMPDO | | Nominal t_{MPDO} (ms) | 0 | 0 | 360 | 0 | 1 | 90 | 1 | 0 | 180 | 1 | 1 | 180 |
| TMPDO | | Nominal t_{MPDO} (ms) | | | | | | | | | | | | | | | | | |
| 0 | 0 | 360 | | | | | | | | | | | | | | | | | |
| 0 | 1 | 90 | | | | | | | | | | | | | | | | | |
| 1 | 0 | 180 | | | | | | | | | | | | | | | | | |
| 1 | 1 | 180 | | | | | | | | | | | | | | | | | |

Note

The PGN and PEn bits (Power Status register) are cleared when there is a TLIM, TOVLD, TMPDO, or TSTART fault condition.

Note

The settings for t_{LIM} set the minimum timeout based on the IEEE compliance requirements.

9.6.2.19 GENERAL MASK Register

COMMAND = 17h with 1 Data Byte, Read/Write

Figure 9-26. GENERAL MASK Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|---------|----------|-------|-------|-------|-------|
| INTEN | – | nbitACC | MbitPrty | CLCHE | DECHE | – | – |
| R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-24. GENERAL MASK Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7 | INTEN | R/W | 1 | <p>$\overline{\text{INT}}$ pin mask bit. Writing a 0 will mask any bit of Interrupt register from activating the $\overline{\text{INT}}$ output, whatever the state of the Interrupt Mask register. Note that activating INTEN has no impact on the event registers.</p> <p>1 = Any unmasked bit of Interrupt register can activate the $\overline{\text{INT}}$ output</p> <p>0 = $\overline{\text{INT}}$ output cannot be activated</p> |
| 6 | – | R/W | 0 | |
| 5 | nbitACC | R/W | 0 | <p>I²C Register Access Configuration bit.</p> <p>1 = Configuration B. This means 16-bit access with a single device address (A0 = 0).</p> <p>0 = Configuration A. This means 8-bit access, while the 8-channel device is treated as 2 separate 4-channel devices with 2 consecutive slave addresses.</p> <p>See register 0x11 for more information on the I2C address programming</p> |
| 4 | MbitPrty | R/W | 0 | <p>Multi Bit Priority bit. Used to select between 1-bit shutdown priority and 3-bit shutdown priority.</p> <p>1 = 3-bit shutdown priority. Register 0x27 and 0x28 need to be followed for priority and OSS action.</p> <p>0 = 1-bit shutdown priority. Register 0x15 needs to be followed for priority and OSS action</p> |
| 3 | CLCHE | R/W | 0 | <p>Class change Enable bit. When set, the CLSCn bits in Detection Event register only indicates when the result of the most current classification operation differs from the result of the previous one.</p> <p>1 = CLSCn bit is set only when a change of class occurred for the associated channel.</p> <p>0 = CLSCn bit is set each time a classification cycle occurred for the associated channel.</p> |
| 2 | DECHE | R/W | 0 | <p>Detect Change Enable bit. When set, the DETCn bits in Detection Event register only indicates when the result of the most current detection operation differs from the result of the previous one.</p> <p>1 = DETCn bit is set only when a change in detection occurred for the associated channel.</p> <p>0 = DETCn bit is set each time a detection cycle occurred for the associated channel.</p> |
| 1 | – | R/W | 0 | |
| 0 | – | R/W | 0 | |

Note

If the MbitPrty bit needs to be changed from 0 to 1, make sure the OSS input pin is in the idle (low) state for a minimum of 200 μsec prior to setting the MbitPrty bit, to avoid any misbehavior related to loss of synchronization with the OSS bit stream.

Note

Only the nbitACC bit for channels 1-4 needs to be set to enable 16-bit I²C operation.

Table 9-25. nbitACC = 1: Register Operations in 8-Bit (Config A) and 16-bit (Config B) I²C Mode

| Cmd Code | Register or Command Name | Bits Description | Configuration A (8-bit) | Configuration B (16-bit) |
|----------|--------------------------------|--|--|--|
| 00h | INTERRUPT | INT bits P1-4, P5-8 | Separate mask and interrupt result per group of 4 channels. | |
| 01h | INTERRUPT MASK | MSK bits P1-4, P5-8 | The Supply event bit is repeated twice. | |
| 02h | POWER EVENT | PGC_PEC P4-1, P8-5 | Separate event byte per group of 4 channels. | |
| 03h | | | | |
| 04h | DETECTION EVENT | CLS_DET P4-1, P8-5 | | |
| 05h | | | | |
| 06h | FAULT EVENT | DIS_PCUT P4-1, P8-5 | | |
| 07h | | | | |
| 08h | START/ILIM EVENT | ILIM_STR P4-1, P8-5 | | |
| 09h | | | | |
| 0Ah | SUPPLY/FAULT EVENT | TSD, VDUV, VDUW, VPUV, RAMFLT PCUT34, PCUT12, PCUT78, PCUT56, OSSE4-1, OSSE8-5 | Both 8-bit registers (channel 1 to 4 and channel 5 to 8) will show the same results for TSD, VDUV, VPUV and RAMFLT. The PCUTxx and OSSEx bits will. have separate status per group of 4 channels. Clearing at least one VPUV/VDUV also clears the other one. | |
| 0Bh | | | | |
| 0Ch | CHANNEL 1 DISCOVERY | CLS&DET1_CLS&DET5 | Separate Status byte per channel | |
| 0Dh | CHANNEL 2 DISCOVERY | CLS&DET2_CLS&DET6 | | |
| 0Eh | CHANNEL 3 DISCOVERY | CLS&DET3_CLS&DET7 | | |
| 0Fh | CHANNEL 4 DISCOVERY | CLS&DET4_CLS&DET8 | | |
| 10h | POWER STATUS | PG_PE P4-1, P8-5 | Separate status byte per group of 4 channels | |
| 11h | PIN STATUS | A4-A1,A0 | Both 8-bit registers (channel 1 to 4 and channel 5 to 8) will show the same result, except that A0 = 0 (channel 1 to 4) or 1 (channel 5 to 8). | Both 8-bit registers (channel 1 to 4 and channel 5 to 8) will show the same result, including A0 = 0. |
| 12h | OPERATING MODE | MODE P4-1, P8-5 | Separate Mode byte per group of 4 channels. | |
| 13h | DISCONNECT ENABLE | DCDE P4-1, P8-5 | Separate DC disconnect enable byte per group of 4 channels. | |
| 14h | DETECT/CLASS ENABLE | CLE_DETE P4-1, P8-5 | Separate Detect/Class Enable byte per group of 4 channels. | |
| 15h | PWRPR/2P-PCUT DISABLE | OSS_DCUT P4-1, P8-5 | Separate OSS/DCUT byte per group of 4 channels. | |
| 16h | TIMING CONFIG | TLIM_TSTRT_TOVLD_TMPD O P4-1, P8-5 | Separate Timing byte per group of 4 channels. | |
| 17h | GENERAL MASK | P4-1, P8-5 including n-bit access | Separate byte per group of 4 channels. n-bit access: Setting this in at least one of the virtual quad register space is enough to enter Config B mode. To go back to config A, clear both. MbitPrty: Setting this in at least one of the virtual quad register space is enough to enter 3-bit shutdown priority. To go back to 1-bit shutdown, clear both MbitPrty bits. | |
| 18h | DETECT/CLASS Restart | RCL_RDET P4-1, P8-5 | Separate DET/CL RST byte per group of 4 channels | |
| 19h | POWER ENABLE | POF_PWON P4-1, P8-5 | Separate POF/PWON byte per group of 4 channels | |
| 1Ah | RESET | P4-1, P8-5 | Separate byte per group of 4 channels, Clear Int pin and Clear All int. | Separate byte per group of 4 channels. |
| 1Bh | ID | | Both 8-bit registers (channel 1 to 4 and channel 5 to 8) will show the same result unless modified through I ² C. | |
| 1Ch | Autoclass and Connection Check | AC4-1, CC34 - 12, AC8-5, CC78-56 | Separate byte per group of 4 channels. | |

Table 9-25. nbitACC = 1: Register Operations in 8-Bit (Config A) and 16-bit (Config B) I²C Mode (continued)

| Cmd Code | Register or Command Name | Bits Description | Configuration A (8-bit) | Configuration B (16-bit) |
|----------|----------------------------|--|---|---|
| 1Eh | 2P POLICE 1/5 CONFIG | POL1, POL5 | Separate Policing byte per channel. | |
| 1Fh | 2P POLICE 2/6 CONFIG | POL2, POL6 | | |
| 20h | 2P POLICE 3/7 CONFIG | POL3, POL7 | | |
| 21h | 2P POLICE 4/8 CONFIG | POL4, POL8 | | |
| 24h | Power-on FAULT | PF P4-1, P8-5 | Separate Power-on FAULT byte per group of 4 channels | |
| 25h | | | | |
| 26h | PORT REMAPPING | Logical P4-1, P8-5 | Separate Remapping byte per group of 4 channels. Reinitialized only if POR or RESET pin. Kept unchanged if 0x1A IC reset or CPU watchdog reset. | |
| 27h | Multi-Bit Priority 21 / 65 | MBP2-1, MBP6-5 | Separate MBP byte per group of 2 channels | |
| 28h | Multi-Bit Priority 43 / 87 | MBP4-3, MBP8-7 | Separate MBP byte per group of 2 channels | |
| 29h | PORT POWER ALLOCATION | 4PW34-12, MC34-12, 4PW78-56, MC78-56 | Separate 4Pnn, MCnn byte per group of 4 channels | |
| 2Ah | 4P POLICE 12 / 56 CONFIG | POL12, POL56 | Separate 4P Policing byte per channel | |
| 2Bh | 4P POLICE 34 / 78CONFIG | POL34, POL78 | Separate 4P Policing byte per channel | |
| 2Ch | TEMPERATURE | TEMP P1-4, P5-8 | Both 8-bit registers (channel 1 to 4 and channel 5 to 8) must show the same result. | |
| 2Dh | 4P FAULT CONFIG | NLM4-1, NCT4-1, 4PPCT4-1,DCDT4-1, NLM8-5, NCT8-5, 4PPCT8-5,DCDT8-5 | Separate fault handling byte per group of 4 channels | |
| 2Eh | INPUT VOLTAGE | VPWR P1-4, P5-8 | Both 8-bit registers (channel 1 to 4 and channel 5 to 8) must show the same result. | |
| 2Fh | | | | |
| 30h | CHANNEL 1 CURRENT | I1, I5 | Separate 2-byte per group of 4 channels | Separate 2-byte per group of 4 channels. 2-byte Read at 0x30 gives I1 4-byte Read at 0x30 gives I1, I5. |
| 31h | | | N/A | |
| 32h | CHANNEL 1 VOLTAGE | V1, V5 | Separate 2-byte per group of 4 channels | 2-byte Read at 0x32 gives V1 4-byte Read at 0x32 gives V1, V5. |
| 33h | | | N/A | |
| 34h | CHANNEL 2 CURRENT | I2, I6 | Separate 2-byte per group of 4 channels | 2-byte Read at 0x34 gives I2 4-byte Read at 0x34 gives I2, I6. |
| 35h | | | N/A | |
| 36h | CHANNEL 2 VOLTAGE | V2, V6 | Separate 2-byte per group of 4 channels | 2-byte Read at 0x36 gives V2 4-byte Read at 0x36 gives V2, V6. |
| 37h | | | N/A | |
| 38h | CHANNEL 3 CURRENT | I3, I7 | Separate 2-byte per group of 4 channels | 2-byte Read at 0x38 gives I3 4-byte Read at 0x38 gives I3, I7. |
| 39h | | | N/A | |
| 3Ah | CHANNEL 3 VOLTAGE | V3, V7 | Separate 2-byte per group of 4 channels | 2-byte Read at 0x3A gives V3 4-byte Read at 0x3A gives V3, V7. |
| 3Bh | | | N/A | |
| 3Ch | CHANNEL 4 CURRENT | I4, I8 | Separate 2-byte per group of 4 channels | 2-byte Read at 0x3C gives I4 4-byte Read at 0x3C gives I4, I8. |
| 3Dh | | | N/A | |
| 3Eh | CHANNEL 4 VOLTAGE | V4, V8 | Separate 2-byte per group of 4 channels | 2-byte Read at 0x3E gives V4 4-byte Read at 0x3E gives V4, V8. |
| 3Fh | | | N/A | |
| 40h | OPERATIONAL FOLDBACK | 2xFB4-1, 2xFB8-5 | Separate 2xFBn config byte per group of 4 channels. | |
| 41h | FIRMWARE REVISION | FRV P1-4, P5-8 | Both 8-bit registers (channel 1 to 4 and channel 5 to 8) must show the same result. | |
| 42h | I2C WATCHDOG | P1-4, P5-8 | IWD3-0: if at least one of the two 4-port settings is different than 1011b, the watchdog is enabled for all 8 channels. WDS: Both 8-bit registers (channel 1 to 4 and channel 5 to 8) must show the same WDS result. Each WDS bit needs to be cleared individually through I ² C. | |

Table 9-25. nbitACC = 1: Register Operations in 8-Bit (Config A) and 16-bit (Config B) I²C Mode (continued)

| Cmd Code | Register or Command Name | Bits Description | Configuration A (8-bit) | Configuration B (16-bit) |
|----------|--------------------------|--|---|--------------------------|
| 43h | DEVICE ID | DID_SR P1-4, P5-8 | Both 8-bit registers (channel 1 to 4 and channel 5 to 8) will show the same result . | |
| 44h | CHANNEL 1 RESISTANCE | RDET1, RDET5 | Separate byte per channel. Detection resistance always updated, detection good or bad. | |
| 45h | CHANNEL 2 RESISTANCE | RDET2, RDET6 | | |
| 46h | CHANNEL 3 RESISTANCE | RDET3, RDET7 | | |
| 47h | CHANNEL 4 RESISTANCE | RDET4, RDET8 | | |
| 4Ch | CHANNEL 1 ASSIGNED CLASS | ACLS&PCLS1_ACLS&PCLS5 | Separate Status byte per channel | |
| 4Dh | CHANNEL 2 ASSIGNED CLASS | ACLS&PCLS2_ACLS&PCLS6 | | |
| 4Eh | CHANNEL 3 ASSIGNED CLASS | ACLS&PCLS3_ACLS&PCLS7 | | |
| 4Fh | CHANNEL 4 ASSIGNED CLASS | ACLS&PCLS4_ACLS&PCLS8 | | |
| 50h | AUTOCLASS CONTROL | MAC4-1, AAC4-1, MAC8-5, AAC8-5 | Separate Auto Class control bytes per 4 channels | |
| 51h | AUTOCLASS POWER 1/5 | PAC1, PAC5 | Separate Auto Class Power Measurement byte per channel | |
| 52h | AUTOCLASS POWER 2/6 | PAC2, PAC6 | | |
| 53h | AUTOCLASS POWER 3/7 | PAC3, PAC7 | | |
| 54h | AUTOCLASS POWER 4/8 | PAC4, PAC8 | | |
| 55h | ALTERNATIVE FOLDBACK | ALTFB4-1, ALTIR4-1, ALTFN8-5, ALTIR8-5 | Separate Alternative Foldback byte per group of 4 channels | |
| 60h | SRAM CONTROL | SRAM CNTRL BITS | These bits must be configured for the lower virtual quad (A0=0, CH 1-4)). These bits have no functionality for the upper virtual quad (A0=1, Ch 5-8) device | |
| 61h | SRAM DATA | | Streaming data input is independent of I ² C configuration | |
| 62h | START ADDRESS (LSB) | | These bits must be configured for the lower virtual quad (A0=0, CH 1-4)). These bits have no functionality for the upper virtual quad (A0=1, Ch 5-8) device | |
| 63h | START ADDRESS (MSB) | | These bits must be configured for the lower virtual quad (A0=0, CH 1-4)). These bits have no functionality for the upper virtual quad (A0=1, Ch 5-8) device | |

9.6.2.20 DETECT/CLASS RESTART Register

COMMAND = 18h with 1 Data Byte, Write Only

Push button register.

Each bit corresponds to a particular cycle (detect or class restart) per channel. Each cycle can be individually triggered by writing a 1 at that bit location, while writing a 0 does not change anything for that event.

In Diagnostic/Manual mode, a single cycle (detect or class restart) will be triggered when these bits are set while in Semi Auto mode, it sets the corresponding bit in the Detect/Class Enable register 0x14.

A Read operation will return 00h.

During $t_{OVL D}$, t_{LIM} or t_{START} cool down cycle, any Detect/Class Restart command for that channel will be accepted but the corresponding action will be delayed until end of cool-down period.

Figure 9-27. DETECT/CLASS RESTART Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|-------|-------|-------|-------|
| RCL4 | RCL3 | RCL2 | RCL1 | RDET4 | RDET3 | RDET2 | RDET1 |
| W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 9-26. DETECT/CLASS RESTART Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|----------------------------|
| 7–4 | RCL4–RCL1 | W | 0 | Restart classification bit |
| 3–0 | RDET4–RDET1 | W | 0 | Restart detection bits |

These bits may be used in place of completing a "Read-Modify-Write" sequence in register 0x14 to enable detection and classification on a per channel basis.

For 4-pair wired ports in Semi Auto or Auto mode, both bits need to be set in order for Detection or Classification to be enabled

9.6.2.21 POWER ENABLE Register

COMMAND = 19h with 1 Data Byte, Write Only

Push button register.

Used to initiate a channel(s) turn on or turn off in any mode except OFF mode.

Figure 9-28. POWER ENABLE Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| POFF4 | POFF3 | POFF2 | POFF1 | PWON4 | PWON3 | PWON2 | PWON1 |
| W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 9-27. POWER ENABLE Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|------------------------|
| 7–4 | POFF4–POFF1 | W | 0 | Channel power off bits |
| 3–0 | PWON4–PWON1 | W | 0 | Channel power on bits |

Note

Writing a “1” at POFFn and PWONn on same Channel during the same write operation turns the Channel off.

Note

The t_{OVLD} , t_{LIM} , t_{START} and disconnect events have priority over the PWON command. During t_{OVLD} , t_{LIM} or t_{START} , cool down cycle, any channel turn on using Power Enable command will be ignored and the Channel will be kept off.

Note

For 4-Pair wired ports:

These bits control the individual Channel response of each Channel. Thus it is recommended that for 4-pair wire ports, the bits for both channels be set simultaneously.

In Semi Auto mode with DETE = CLE = 1 on both channels, it is permissible to set only one PWON bit to attempt to turn on only that singular channel.

For 4P Single Signature devices that classify as class 5-8, a singular PWON command will fail and a STRT fault set with the “insufficient power” code written to 0x24.

If the PD presents itself as class 4 or below, then only that pair set will be powered.

Setting the alternate PWON bit for the secondary channel of a single signature device after the primary is already powered will result in the immediate turn on of the channel without completing DET or CLS.

For a 4-Pair Dual Signature device that has only one channel powered, setting the PWON bit for the unpowered channel will result in a turn on attempt on that channel based on the assigned classification of the other channel and the Power Allocation settings in 0x29h at the time of the new PWON command.

PWONn in Diagnostic/Manual Mode:

If the PSE controller is configured in Diagnostic mode, writing a “1” at that PWONn bit location will immediately turn on the associated Channel.

PWONn in Semi Auto Mode:

While in Semi Auto mode, writing a “1” at a PWONn bit will attempt to turn on the associated Channel. If the detection or class results are invalid, the Channel is not turned on, and there will be no additional attempts to turn on the Channel until this push button is reasserted and the channel will resume its configured semi auto mode operation.

Note

In Semi Auto mode, the Power Allocation (0x29h) value needs to be set prior to issuing a PWON command. Any changes to the Power Allocation value after a PWON command is given may be ignored.

Table 9-28. Channel Response to PWONn Command in Semi Auto Mode

| CLEn | DETEn | Channel Operation | Result of PWONn Command |
|------|-------|-------------------|--|
| 0 | 0 | Idle | Singular Turn On attempted with Full DET and CLS cycle |

Table 9-28. Channel Response to PWONn Command in Semi Auto Mode (continued)

| CLEn | DETEn | Channel Operation | Result of PWONn Command |
|------|-------|---|--|
| 0 | 1 | Cycling Detection Measurements only | Singular Turn On attempted with Full DET and CLS cycle |
| 1 | 0 | Idle | Singular Turn On attempted with Full DET and CLS cycle |
| 1 | 1 | Cycling Detection and Classification Measurements | Singular Turn On attempted after next (or current) DET and CLS cycle |

In semi auto mode with DETE and CLE set, as long as the PWONx command is received prior to the start of classification, the Channel will be powered immediately after classification is complete provided the classification result is valid and the power allocations settings (see register 0x29h) are sufficient to enable power on.

PWONn in Auto Mode:

In Auto mode with DETE or CLE set to 0, a PWONx command will initiate a singular detection and classification cycle and the port/channel will be powered immediately after classification is complete provided the classification result is valid and the power allocations settings (see register 0x29h) are sufficient to enable power on.

In Auto mode with DETE and CLE = 1, there is no need for a PWON command. The port/channel will automatically attempt to turn on after each detection and classification cycle.

Note

In Auto mode, the Power Allocation (0x29h) value needs to be set prior to issuing a PWON command. Any changes to the Power Allocation value after a PWON command is given may be ignored.

A singular PWONn command will be ignored for a 4-Pair wired port in Auto mode.

Table 9-29. Channel Response to PWONn Command in Auto Mode

| CLEn | DETEn | Channel Operation | Result of PWONn Command |
|------|-------|---|--|
| 0 | 0 | Idle | Singular Turn On attempted with Full DET and CLS cycle |
| 0 | 1 | Cycling Detection Measurements only | Singular Turn On attempted with Full DET and CLS cycle |
| 1 | 0 | Idle | Singular Turn On attempted with Full DET and CLS cycle |
| 1 | 1 | Cycling Detection and Classification Measurements | NA - Channel will power automatically after a valid detection and classification |

PWOFFn in any Mode:

The channel is immediately disabled and the following registers are cleared:

Table 9-30. Channel Turn Off with PWOFFn Command

| Register | Bits to be Reset |
|-----------|--|
| 0x04 | CLSCn and DETCn |
| 0x06 | DISFn and PCUTn |
| 0x08 | STRn and ILIMn |
| 0x0A/B | PCUTnn |
| 0x0C-0F | Requested Class and Detection |
| 0x10 | PGn and PEn |
| 0x14 | CLEn and DETEn |
| 0x1C | ACn and CCnn |
| 0x1E-21 | 2P Policing set to 0xFFh |
| 0x24 | PFn |
| 0x2A-2B | 4P Policing set to 0xFFh |
| 0x2D | NLMnn, NCTnn, 4PPCTnn, and DCdTnn |
| 0x30-3F | Channel Voltage and Current Measurements |
| 0x40 | 2xFBn |
| 0x44 - 47 | Detection Resistance Measurements |
| 0x4C-4F | Assigned Class and Previous Class |
| 0x51-54 | Autoclass Measurement |

Note

It may take upwards of 5ms after PWOFFn command for all register values to be updated.

Only the bits associated with the channel/port ("n") with PWOFFn set will be cleared. Those bits associated with channels/ports remaining in operation will not be changed.

These bits control the response of each channel **individually**. Thus, it is recommended that for 4-pair wire ports, the bits for both channels be set simultaneously.

Note

If only one channel of a 4-pair single signature load with a Class 5 or higher assigned class is given a PWOFFn command, **both** channels will be disabled.

In the event a singular channel of a 4-pair dual signature PD is turned off due to a PWOFFn command, the power may be reapplied to that channel by setting the PWON bit in 0x19h provided the detection and classification are still valid and the Power Allocation settings in 0x29 are sufficient based on the assigned classification of the powered channel.

9.6.2.22 RESET Register

COMMAND = 1Ah with 1 Data Byte, Write Only

Push button register.

Writing a 1 at a bit location triggers an event while a 0 has no impact. Self-clearing bits.

Figure 9-29. RESET Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-------|-----|-------|-------|-------|-------|-------|
| CLRAIN | CLINP | – | RESAL | RESP4 | RESP3 | RESP2 | RESP1 |
| W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 9-31. RESET Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|---|
| 7 | CLRAIN | W | 0 | Clear all interrupts bit. Writing a 1 to CLRAIN clears all event registers and all bits in the Interrupt register. It also releases the INT pin |
| 6 | CLINP | W | 0 | When set, it releases the $\overline{\text{INT}}$ pin without any impact on the Event registers nor on the Interrupt register. |
| 5 | – | W | 0 | |
| 4 | RESAL | W | 0 | Reset all bits when RESAL is set. Results in a state similar to a power-up reset. Note that the VDUV and VPUV bits (Supply Event register) follow the state of VDD and VPWR supply rails. |
| 3–0 | RESP4–RESP1 | W | 0 | Reset channel bits. Used to force an immediate channel(s) turn off in any mode, by writing a 1 at the corresponding RESPn bit location(s). Note: For a 4-pair wired port, setting a RESPn bit for either channel will result in both channels being reset. |

Setting the RESAL bit will result in all of the I2C register being restored to the RST condition with the exception of those in the following table:

| Register | Bits | RESAL Result |
|---------------|----------------------------|-----------------------------|
| 0x00 | All | Pre RESAL value will remain |
| 0x0A/B | TSD, VPUV, VDWRN, and VPUV | |
| 0x26 | All | |
| 0x2C and 0x2E | All | |
| 0x41 | All | |

Note

Setting the RESAL bit for only one group of four channels (1-4 or 5-8) will result in only those four channels being reset.

Note

After using the CLINP command, the $\overline{\text{INT}}$ pin will not be reasserted for any interrupts until all existing interrupts have been cleared.

Setting the RESPn bit will immediate turn off the associated channel and clear the registers according to the following table:

Table 9-32. Channel Turn Off with RESPn Command

| Register | Bits to be Reset |
|-----------|--|
| 0x04 | CLSCn and DETCn |
| 0x06 | DISFn and PCUTn |
| 0x08 | STRTn and ILIMn |
| 0x0A/B | PCUTnn |
| 0x0C-0F | Requested Class and Detection |
| 0x10 | PGn and PEn |
| 0x14 | CLEn and DETEn |
| 0x1C | ACn and CCnn |
| 0x1E-21 | 2P Policing set to 0xFFh |
| 0x24 | PFn |
| 0x2A-2B | 4P Policing set to 0xFFh |
| 0x2D | NLMnn, NCTnn, 4PPCTnn, and DCDTnn |
| 0x30-3F | Channel Voltage and Current Measurements |
| 0x40 | 2xFBn |
| 0x44 - 47 | Detection Resistance Measurements |
| 0x4C-4F | Assigned Class and Previous Class |
| 0x51-54 | Autoclass Measurement |

Note

Only the bits associated with the channel/port ("n") with RESPn set will be cleared. Those bits associated with channels/ports remaining in operation will not be changed.

it may take upwards of 5 ms before all of the registers are cleared following a RESPn command.

The RESPn command will cancel any ongoing cool down cycles .

Users need to wait at least 3ms before trying to reenable discovery or power on ports following a RESPn command.

9.6.2.23 ID Register

COMMAND = 1Bh with 1 Data Byte, Read/Write

Figure 9-30. ID Register Format

| | | | | | | | |
|--------|-------|-------|-------|-------|-------|-------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MFR ID | | | | | ICV | | |
| R/W-0 | R/W-1 | R/W-0 | R/W-1 | R/W-0 | R/W-1 | R/W-0 | R/W-1 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-33. ID Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------|------|------------|--|
| 7–3 | MFR ID | R/W | 01010 b | Manufacture Identification number (0101,0) |
| 2–0 | ICV | R/W | 101b | IC version number (011) |

9.6.2.24 Connection Check and Auto Class Status Register

COMMAND = 1Ch with 1 Data Byte, Read Only

Figure 9-31. Connection Check and Auto Class Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|-----|-----|-----|--------|--------|--------|--------|
| AC4 | AC3 | AC2 | AC1 | CC34_2 | CC34_1 | CC12_2 | CC12_1 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-34. Connection Check and Auto Class Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|---|
| 7–4 | ACn | R | 0000b | Auto Class Detection Status 1 = PD supports Auto Class 0 = PD does not support Auto Class |
| 3–2 | CC34_2/1 | R | 00b | Connection Check result for 4-Pair port (channels 3 and 4) |
| 1-0 | CC12_2/1 | R | 00b | Connection Check result for 4-Pair port (channels 1 and 2) |

Auto Class:

The auto class detection measurement is completed at the end of the long classification finger, and if a PD is determined to support auto class, an auto class power measurement will be automatically completed after turn on in accordance with the IEEE auto class timing requirements.

Note

The auto class function is operational regardless if a port is wired for 2-Pair or 4-Pair operation.

For 4-Pair single signature devices, both ACn bits will report the same result even though the classification measurement was completed on one channel.

An Auto Class power measurement will be completed shortly after power on for all channels that are found to support auto class during classification.

These measurement results are available in registers (0x51h – 0x54h), and the auto class power measurements are provide per individual channel.

Connection Check:

A connection check measurement will only be performed on 4-pair wired ports after at least one channel is found to have a valid detection result.

The results of connection check

| CCnn_2 | CCnn_1 | CC Result |
|--------|--------|-------------------------|
| 0 | 0 | "unknown" or incomplete |
| 0 | 1 | Single Signature |
| 1 | 0 | Dual Signature |
| 1 | 1 | Reserved |

These bits will be set following the completion of a connection check and prior to the setting of the Detection Event bits in the Detection Event register (0x04h).

9.6.2.25 2-Pair Police Ch-1 Configuration Register

COMMAND = 1Eh with 1 Data Byte, Read/Write

Figure 9-32. 2-Pair Police Ch-1 Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| POL1_7 | POL1_6 | POL1_5 | POL1_5 | POL1_3 | POL1_2 | POL1_1 | POL1_0 |
| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W1 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.6.2.26 2-Pair Police Ch-2 Configuration Register

COMMAND = 1Fh with 1 Data Byte, Read/Write

Figure 9-33. 2-Pair Police Ch-2 Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| POL2_7 | POL2_6 | POL2_5 | POL2_4 | POL2_3 | POL2_2 | POL2_1 | POL2_0 |
| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W1 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.6.2.27 2-Pair Police Ch-3 Configuration Register

COMMAND = 20h with 1 Data Byte, Read/Write

Figure 9-34. 2-Pair Police Ch-3 Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| POL3_7 | POL3_6 | POL3_5 | POL3_5 | POL3_3 | POL3_2 | POL3_1 | POL3_0 |
| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W1 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.6.2.28 2-Pair Police Ch-4 Configuration Register

COMMAND = 21h with 1 Data Byte, Read/Write

Figure 9-35. 2-Pair Police Ch-4 Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| POL4_7 | POL4_6 | POL4_5 | POL4_4 | POL4_3 | POL4_2 | POL4_1 | POL4_0 |
| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W1 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-35. 2-Pair Policing Register Fields Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|---|
| 7–0 | POLn_7- POLn_0 | R/W | 1 | 1-byte defining 2-Pair P_{CUT} minimum threshold. The equation defining the P_{CUT} is: $P_{CUT} = (N \times PC_{STEP})$ Where, when assuming 0.255-Ω Rsense resistor is used: $PC_{STEP} = 0.5 W$ |

Note

These bits set the minimum threshold for the design. Internally, the typical PCUT threshold is set slightly above this value to ensure that the device does not trip a Pcut fault at or below the set value in this register due to part to part or temperature variation.

For 4-pair wired ports, the 2P Policing values are still applied to the individual channels. See the description for registers 0x2Ah and 0x2Bh for more information on 4-Pair Policing.

The contents of this register is reset to 0xFFh anytime the port is turned off or disabled either due to fault condition or user command

Power Policing:

The TPS23880 implements a true Power Policing limit, where the device will adjust the policing limit based on both voltage and current variation in order to ensure a reliable power limit.

In Semi Auto and Auto modes, these bits are automatically set during power on based on the assigned class (see tables below). If an alternative value is desired, it needs to be set after the PEn bit is set in 0x10h.

Table 9-36. 2-Pair Policing Settings for 2-Pair Wired Ports and 4-Pair Dual Signature Devices

| Assigned Class | POLn7-0 Settings | Minimum Power |
|------------------------|------------------|---------------|
| Class 1 | 0000 1000 | 4W |
| Class 2 | 0000 1110 | 7W |
| Class 3 | 0001 1111 | 15.5W |
| Class 4 | 0011 1100 | 30W |
| Class 5 Dual Signature | 0101 1010 | 45W |

Table 9-37. 2-Pair Policing Settings for 4-Pair Wired Port with Single Signature Devices

| Assigned Class | POLn7-0 Settings | Minimum Power |
|----------------|------------------|----------------------|
| Class 1 | 0000 1000 | 4W ⁽¹⁾ |
| Class 2 | 0000 1110 | 7W ⁽¹⁾ |
| Class 3 | 0001 1111 | 15.5W ⁽¹⁾ |
| Class 4 | 0011 1100 | 30W ⁽¹⁾ |
| Class 5 | 0100 0000 | 32W ⁽²⁾ |
| Class 6 | 0100 1110 | 39W ⁽²⁾ |
| Class 7 | 0101 1001 | 44.5W ⁽²⁾ |
| Class 8 | 0110 1011 | 53.5W ⁽²⁾ |

- (1) Both channels of a 4-Pair port with a single signature device and an assigned class of 1-4 are required to support the full classification current per pair set.
- (2) 4-Pair ports with a single signature device and an assigned class of 5-8 are required to satisfy the IEEE load imbalance requirements for 4-Pair powered devices.

9.6.2.29 Power-on Fault Register

COMMAND = 24h with 1 Data Byte, Read Only

COMMAND = 25h with 1 Data Byte, Clear on Read

Figure 9-36. Power-on Fault Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|------|------|------|------|
| PF4 | | PF3 | | PF2 | | PF1 | |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 | CR-0 |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; CR = Clear on Read; -n = value after reset

Table 9-38. Power-on Fault Register Field Descriptions

| Bit | Field | Type | Reset | Description | | | | | | | | | | |
|------------|----------------------------|---------|-------|---|------------|----------------------------|-----|----------|-----|-------------------|-----|----------------------|-----|--------------------|
| 7–0 | PF4–PF1 | R or CR | 0 | <p>Represents the fault status of the classification and detection for channel n, following a failed turn on attempt with the PWONn command. These bits are cleared when channel n is turned off. PFn: the selection is as follows:</p> <table border="1"> <thead> <tr> <th>Fault Code</th> <th>Power-on Fault Description</th> </tr> </thead> <tbody> <tr> <td>0 0</td> <td>No fault</td> </tr> <tr> <td>0 1</td> <td>Invalid detection</td> </tr> <tr> <td>1 0</td> <td>Classification Error</td> </tr> <tr> <td>1 1</td> <td>Insufficient Power</td> </tr> </tbody> </table> | Fault Code | Power-on Fault Description | 0 0 | No fault | 0 1 | Invalid detection | 1 0 | Classification Error | 1 1 | Insufficient Power |
| Fault Code | Power-on Fault Description | | | | | | | | | | | | | |
| 0 0 | No fault | | | | | | | | | | | | | |
| 0 1 | Invalid detection | | | | | | | | | | | | | |
| 1 0 | Classification Error | | | | | | | | | | | | | |
| 1 1 | Insufficient Power | | | | | | | | | | | | | |

Note

When a Start Fault occurs and the PECn bit is not set, then this register will indicate the cause of the fault.

An insufficient power fault is reported anytime the reg 0x29 configuration will not allow a channel to be powered. See the section describing [Section 9.1.5](#).

For 4-pair wired Ports:

These bits will be updated **individually** for dual signature connected devices

These bits will be updated **concurrently** for single signature connected devices

9.6.2.30 PORT RE-MAPPING Register

COMMAND = 26h with 1 Data Byte, Read/Write

Figure 9-37. PORT RE-MAPPING Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|-------|---|-------|---|-------|---|-------|
| Physical Channel # of Logical Channel 4 | | Physical Channel # of Logical Channel 3 | | Physical Channel # of Logical Channel 2 | | Physical Channel # of Logical Channel 1 | |
| R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; CR = Clear on Read; -n = value after reset

Table 9-39. PORT RE-MAPPING Register Field Descriptions

| Bit | Field | Type | POR / RST | Description | | | | | | | | | | | | | | | |
|-------------|---|--------------|----------------------|--|-------------|------------------|--------------|---|---|---|---|---|---|---|---|---|---|---|---|
| 7-0 | Physical Channel # of Logical Channel n | R/W | 1110 0100b / P | <p>Used to re-map channels logically due to physical board constraints. Re-mapping is between any channel within 4-channel group (1-4 or 5-8). All channels of a group of four must be in OFF mode prior to receiving the port re-mapping command, otherwise the command will be ignored. By default there is no re-mapping.</p> <p>Each pair of bits corresponds to the logical port assigned.</p> <p>The selection per port is as follows:</p> <table border="1" style="margin-left: 20px; border-collapse: collapse; text-align: center;"> <thead> <tr> <th style="width: 10%;">Re-Map Code</th> <th style="width: 10%;">Physical Channel</th> <th style="width: 10%;">Package Pins</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>2</td> </tr> <tr> <td>1</td> <td>0</td> <td>3</td> </tr> <tr> <td>1</td> <td>1</td> <td>4</td> </tr> </tbody> </table> <p>When there is no re-mapping the default value of this register is 1110,0100. The 2 MSbits with a value 11 indicate that logical channel 4 is mapped onto physical channel #4, the next 2 bits, 10, suggest logical channel 3 is mapped onto physical channel #3 and so on.</p> <p>Note: Code duplication is not allowed – that is, the same code cannot be written into the remapping bits of more than one port – if such a value is received, it will be ignored and the chip will stay with existing configuration.</p> <p>Note: Port remapping configuration is kept unchanged if 0x1A IC reset command is received.</p> | Re-Map Code | Physical Channel | Package Pins | 0 | 0 | 1 | 0 | 1 | 2 | 1 | 0 | 3 | 1 | 1 | 4 |
| Re-Map Code | Physical Channel | Package Pins | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | | | | | | | | | | | | | | | | | |
| 0 | 1 | 2 | | | | | | | | | | | | | | | | | |
| 1 | 0 | 3 | | | | | | | | | | | | | | | | | |
| 1 | 1 | 4 | | | | | | | | | | | | | | | | | |

Note

The RST condition of "P" indicates that the previous state of these bits will be preserved following a device reset using the $\overline{\text{RESET}}$ pin. Thus, pulling the $\overline{\text{RESET}}$ input low will not overwrite any user changes to this register.

Note

Only logical Channels 3 and 4 and 1 and 2 may be wired as 4-pair Ports. Unpredictable behavior will occur if any other combinations of logical Channels are wired in a 4-pair configuration.

Note

After port remapping, TI recommends to do at least one detection-classification cycle before turn on.

9.6.2.31 Channels 1 and 2 Multi Bit Priority Register

COMMAND = 27h with 1 Data Byte, Read/Write .

Figure 9-38. Channels 1 and 2 MBP Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|--------|--------|--------|-------|--------|--------|--------|
| – | MBP2_2 | MBP2_1 | MBP2_0 | – | MBP1_2 | MBP1_1 | MBP1_0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.6.2.32 Channels 3 and 4 Multi Bit Priority Register

COMMAND = 28h with 1 Data Byte, Read/Write

Figure 9-39. Channels 3 and 4 MBP Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|--------|--------|--------|-------|--------|--------|--------|
| – | MBP4_2 | MBP4_1 | MBP4_0 | – | MBP3_2 | MBP3_1 | MBP3_0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-40. Channels n MBP Register Field Descriptions

| Bit | Field | Type | Reset | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------------|----------|------|--------------------|---|---------------------------|--|--|--------------------|--------------------------|---|---|---|---------|-------------|---|---|---|---|----------------------|---|---|---|---|-------------|---|---|---|---|-------------|---|---|---|---|-------------|---|---|---|---|-----------------------------|---|---|---|--------|----------------|
| 7-0 | MBPn_2-0 | R/W | 0 | <p>MBPn_2-0: Multi Bit Priority bits, three bits per channel, if 3-bit shutdown priority has been selected (MbitPrty in General Mask register is high). It is used to determine which channel(s) is (are) shut down in response to a serial shutdown code received at the OSS shutdown input.</p> <p>The turn off procedure (including register bits clearing) is similar to a channel reset using Reset command (1Ah register), except that it does not cancel any ongoing fault cool down time count.</p> <p>The priority is defined as followings:</p> <p>OSS code ≤ MBPn_2-0 : when the OSS code is received, the corresponding channel is powered off.</p> <p>OSS code > MBPn_2-0 : OSS code has no impact on the channel</p> <table border="1" data-bbox="571 1209 1365 1530"> <thead> <tr> <th colspan="3">MBPn_2-0 0x27/28 Register</th> <th>Multi Bit Priority</th> <th>OSS Code for Channel Off</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Highest</td> <td>OSS = '000'</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>2</td> <td>OSS = '000' or '001'</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>3</td> <td>OSS ≤ '010'</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>4</td> <td>OSS ≤ '011'</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>4</td> <td>OSS ≤ '100'</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>6</td> <td>OSS = any code except '111'</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Lowest</td> <td>OSS = any code</td> </tr> </tbody> </table> | MBPn_2-0 0x27/28 Register | | | Multi Bit Priority | OSS Code for Channel Off | 0 | 0 | 0 | Highest | OSS = '000' | 0 | 0 | 1 | 2 | OSS = '000' or '001' | 0 | 1 | 0 | 3 | OSS ≤ '010' | 0 | 1 | 1 | 4 | OSS ≤ '011' | 1 | 0 | 0 | 4 | OSS ≤ '100' | 1 | 0 | 1 | 6 | OSS = any code except '111' | 1 | 1 | 1 | Lowest | OSS = any code |
| MBPn_2-0 0x27/28 Register | | | Multi Bit Priority | OSS Code for Channel Off | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | Highest | OSS = '000' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 2 | OSS = '000' or '001' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 3 | OSS ≤ '010' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 4 | OSS ≤ '011' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 4 | OSS ≤ '100' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 6 | OSS = any code except '111' | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | Lowest | OSS = any code | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

The priority reduces as the 3-bit value increases. Thus, a channel with a "000" setting has the highest priority, while one with a "111" setting has the lowest.

It is permissible to apply the same settings to multiple channels. Doing so will result in all channels with the same setting will be disabled when the appropriate OSS code is presented.

For 4-pair wired Ports, these bits control the individual Channel response. In order for both pair sets of a 4-pair wire Port to be disabled, both channels need to have the same MBP setting otherwise it is possible for only one pair set to be disabled.

In the event a singular channel of a 4-pair dual signature PD is turned off due to OSS or other reason, power may be reapplied to that channel by setting the PWON bit in 0x19h provided the detection and classification

are still valid and the Power Allocation settings in 0x29 are sufficient based on the assigned classification of the powered channel.

The turn off procedure due to OSS is similar to a channel reset or change to OFF mode, with the exception that OSS does not cancel any ongoing fault cool down timers. the table below includes the bits that will be cleared when a channel is disabled due to OSS:

Table 9-41. Channel Turn Off with MBP OSS

| Register | Bits to be Reset |
|-----------|--|
| 0x04 | CLSCn and DETCn |
| 0x06 | DISFn and PCUTn |
| 0x08 | STRTn and ILIMn |
| 0x0A/B | PCUTnn |
| 0x0C-0F | Requested Class and Detection |
| 0x10 | PGn and PEn |
| 0x14 | CLEn and DETEn |
| 0x1C | ACn and CCnn |
| 0x1E-21 | 2P Policing set to 0xFFh |
| 0x24 | PFn |
| 0x2A-2B | 4P Policing set to 0xFFh |
| 0x2D | NLMnn, NCTnn, 4PPCTnn, and DCDTnn |
| 0x30-3F | Channel Voltage and Current Measurements |
| 0x40 | 2xFBn |
| 0x44 - 47 | Detection Resistance Measurements |
| 0x4C-4F | Assigned Class and Previous Class |
| 0x51-54 | Autoclass Measurement |

Note

There is no memory of any preceding 3-bit OSS commands. Each 3-bit OSS command is processed immediately (prior to the end of the last OSS MBP pulse) based on the MBPn settings for each Channel. Any attempt to shutdown additional Channels thereafter will require additional 3-bit OSS commands.

9.6.2.33 4-Pair Wired and Port Power Allocation Register

COMMAND = 29h with 1 Data Byte, Read/Write

Figure 9-40. 4-Pair Wired and Power Allocation Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|--------|--------|--------|-------|--------|--------|--------|
| 4PW34 | MC34_2 | MC34_1 | MC34_0 | 4PW12 | MC12_2 | MC12_1 | MC12_0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-42. 4-Pair Wired and Power Allocation Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------------------|----------|------|-------|---|
| 7, 3 | 4PWnn | R/W | 0 | 4-Pair wired configuration bits 4PWnn = 1: Channels 3/4 or 1/2 are wired in a 4-pair configuration 4PWnn = 0: Channels 3/4 or 1/2 are wired in 2-pair configurations |
| 6 - 4 , 2 - 0 | MCnn_2-0 | R/W | 0 | MCnn_2-0: Port Power Allocation bits. These bits set the maximum power classification level that a given Port (2-Pair or 4-Pair) is allowed to power on In Semi Auto mode these bits need to be set prior to issuing a PWONn command, while in Auto mode these bits need to be set prior to setting the DETE and CLE bits in 0x14. |

Table 9-43. 4-Pair Wired and Power Allocation Settings

| 4PWnn | MCnn_2 | MCnn_1 | MCnn_0 | Power Allocation |
|-------|--------|--------|--------|----------------------|
| 0 | 0 | 0 | 0 | 2-Pair 15.4W |
| 0 | 0 | 0 | 1 | Reserved |
| 0 | 0 | 1 | 0 | Reserved |
| 0 | 0 | 1 | 1 | 2-Pair 30W |
| 0 | 1 | x | x | Reserved |
| 1 | 0 | 0 | 0 | 4-Pair 15.4W |
| 1 | 0 | 0 | 1 | Reserved |
| 1 | 0 | 1 | 0 | Reserved |
| 1 | 0 | 1 | 1 | 4-Pair 30W (Class 4) |
| 1 | 1 | 0 | 0 | 4-Pair 45W (Class 5) |
| 1 | 1 | 0 | 1 | 4-Pair 60W (Class 6) |
| 1 | 1 | 1 | 0 | 4-Pair 75W (Class 7) |
| 1 | 1 | 1 | 1 | 4-Pair 90W (Class 8) |

Refer to [Table 9-2](#) and [Table 9-3](#) for more details on the application of Power Demotion and the relationship between the Power Allocation settings and the resulting Assigned Class.

Note

In order to prevent any unexpected behavior the setting the 4PWnn bits should only be done immediately following a Power On Reset (POR) event while the ports are still in OFF mode.

Note

The Power Allocation (0x29h) value needs to be set prior to issuing a PWON command in Semi Auto or Auto modes, and prior to setting the DETE and CLE bits in Auto mode. Any changes to the Power Allocation value after a PWON command is given may be ignored.

Note

For 4-pair dual signature PDs, the odd numbered Channels takes priority over the even numbered Channels. Thus, an even numbered Channel will be powered based on the difference between the total power allocated and what the odd Channel classified as.

For example if a dual signature PD contained two 45W PDs and the PSEs power allocation was set to 60W, the odd numbered Channel will be powered at 45W while the even numbered Channel will be limited to 15W.

Note

For 2-Pair wired ports, the MCnn_2-0 bits set the power allocation settings for both channels 1 and 2 and 3 and 4 concurrently.

It is possible to have channels 3 and 4 set to 15.4W while channels 1 and 2 are set to 30W, but it is not possible to have different power allocation settings between channels 1 and 2 or 3 and 4

9.6.2.34 4-Pair Police Ch-1 and 2 Configuration Register

COMMAND = 2Ah with 1 Data Byte, Read/Write

Figure 9-41. 4-Pair Police Ch-1 and 2 Configuration Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| POL12_7 | POL12_6 | POL12_5 | POL12_4 | POL12_3 | POL12_2 | POL12_1 | POL12_0 |
| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W1 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.6.2.35 4-Pair Police Ch-3 and 4 Configuration Register

COMMAND = 2Bh with 1 Data Byte, Read/Write

Figure 9-42. 4-Pair Police Ch-3 and 4 Configuration Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| POL34_7 | POL34_6 | POL34_5 | POL34_4 | POL34_3 | POL34_2 | POL34_1 | POL34_0 |
| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W1 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-44. 4-Pair Police Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|-------|---|
| 7–0 | POLnn_7- POLnn_0 | R/W | 1 | 1-byte defining the summed 4-Pair P _{CUT} minimum threshold. The equation defining the P _{CUT} is: $P_{CUT} = (N \times PC_{STEP})$ Where, when assuming 0.255-Ω R _{sense} resistor is used: $PC_{STEP} = 0.5 W$ |

Note

These bits set the minimum threshold for the design. Internally, the typical PCUT threshold is set slightly above this value to ensure that the device does not trip a Pcut fault at or below the set value in this register due to part to part or temperature variation.

For 4-pair wired, the 2P Policing values are still applied to the individual Channels. See the description for registers 0x1Eh through 0x21h for more information on 2-Pair Policing.

The contents of this register is reset to 0xFFh anytime the port is turned off or disabled either due to fault condition or user command

4-Pair Power Policing:

The TPS23880 implements a true Power Policing limit, where the device will adjust the policing limit based on both voltage and sum of current variation in order to ensure a reliable power limit.

In Semi Auto and Auto modes, these bits are automatically set during power on based on the assigned class (see [Table 9-45](#)). If an alternative value is desired, it needs to be set after the PEn bit is set in register 0x10h.

Table 9-45. 4-Pair Policing Settings for 4-Pair Wired Port with Single Signature Devices

| Assigned Class | POLnn7-0 Settings | Minimum Power |
|----------------|-------------------|---------------|
| Class 1 | 0000 1000 | 4W |
| Class 2 | 0000 1110 | 7W |
| Class 3 | 0001 1111 | 15.5W |
| Class 4 | 0011 1100 | 30W |
| Class 5 | 0101 1010 | 45W |
| Class 6 | 0111 1000 | 60W |
| Class 7 | 1001 0110 | 75W |
| Class 8 | 1011 0100 | 90W |

For a 4-pair dual signature devices, these values will be set based on the sum of the assigned classes of both channels, but 4P PCut will be disabled (4PPCTnn bit in 0x2D = 0) by default as the primary policing method for dual signature devices will be the 2-Pair values defined in registers 0x1Eh - 0x21h.

Setting the 4PPCTnn bit in 0x2D will enable 4P Policing if desired.

9.6.2.36 TEMPERATURE Register

COMMAND = 2Ch with 1 Data Byte, Read Only

Figure 9-43. TEMPERATURE Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TEMP7 | TEMP6 | TEMP5 | TEMP4 | TEMP3 | TEMP2 | TEMP1 | TEMP0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-46. TEMPERATURE Register Field Descriptions

| Bit | Field | Type | Reset | Description | | | | | | |
|------|------------------|-------------------|-------|--|------|------------------|-------------------|-----|---------|---------|
| 7-0 | TEMP7-TEMP0 | R | 0 | <p>Bit Descriptions: Data conversion result. The I²C data transmission is a 1-byte transfer. 8-bit Data conversion result of temperature, from -20°C to 125°C. The update rate is around once per second.</p> <p>The equation defining the temperature measured is:</p> $T = -20 + N \times T_{STEP}$ <p>Where T_{STEP} is defined below as well as the full scale value:</p> <table border="1" data-bbox="659 821 1198 894"> <thead> <tr> <th>Mode</th> <th>Full Scale Value</th> <th>T_{STEP}</th> </tr> </thead> <tbody> <tr> <td>Any</td> <td>146.2°C</td> <td>0.652°C</td> </tr> </tbody> </table> | Mode | Full Scale Value | T _{STEP} | Any | 146.2°C | 0.652°C |
| Mode | Full Scale Value | T _{STEP} | | | | | | | | |
| Any | 146.2°C | 0.652°C | | | | | | | | |

9.6.2.37 4-Pair Fault Configuration Register

COMMAND = 2Dh with 1 Data Byte, Read/Write

Figure 9-44. 4-Pair Fault Configuration Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|-------|---------|---------|--------|--------|
| NLM34 | NLM12 | NCT34 | NCT12 | 4PPCT34 | 4PPCT12 | DCDT34 | DCDT12 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-47. 4-Pair Fault Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|---------|------|-------|--|
| 7, 6 | NLMnn | R/W | 0 | <p>4-Pair ILIM Fault Management bits</p> <p>1 = Both channels on a 4-Pair wired port will be disabled if an ILIM fault occurs on either channel</p> <p>0 = Only the channel on which the ILIM fault occurred will be disabled. The alternative channel will remain powered.</p> <p>In Auto mode these bits will be automatically set after turn on if a 4-Pair Single Signature device is powered</p> |
| 5, 4 | NCTnn | R/W | 0 | <p>4-Pair PCUT Fault Management bits</p> <p>1 = Both channels on a 4-Pair wired port will be disabled if a 2-Pair P_{CUT} fault occurs on either channel</p> <p>0 = Only the channel on which the 2-Pair P_{CUT} fault occurred will be disabled. The alternative channel will remain powered.</p> <p>In Auto mode these bits will be automatically set after turn on if a 4-Pair Single Signature device is powered</p> |
| 3, 2 | 4PPCTnn | R/W | 0 | <p>4-Pair Summed PCUT Enable bits</p> <p>1 = Summed 4-Pair PCut is enabled</p> <p>0 = Summed 4-Pair PCut is disabled</p> <p>The hardware continue to monitor for ILIM faults independent of these bits</p> <p>In either Auto and Semi Auto modes, these bits will be automatically set to a "1" after turn on if a 4-Pair Single Signature device is powered</p> |
| 1, 0 | DCDTnn | R/W | 0 | <p>DC Disconnect Threshold bits</p> <p>1 = DC disconnect Threshold set to 4.5mA typical</p> <p>0 = DC disconnect Threshold set to 6.5mA typical</p> <p>For 4-pair Dual Signature PDs, the DCDTxx bit will be set to "1" during turn on and the disconnect threshold will be applied independently per Channel. Thus, if either channel falls below the 4.5mA threshold for the duration of TMPDO + TMPS, only that channel will be disabled while the alternative channel remains powered as long it it satisfies.</p> <p>For 4-pair single signature PDs (see register 0x1Ch), these bits are internally set during power on based on the assigned class (0x4C-4F):</p> <p>Assigned Classes 1-4: DCDTxx = 0</p> <p>Assigned Classes 5-8: DCDTxx = 1</p> |

Note

Partial Disconnect: For 4-pair single signature PDs with DCDTxx = 0 and an Assigned Class = 0-4, one pair set/channel will be immediately disabled when either channel falls below the DC Disconnect threshold to improve the low current measurement accuracy. The second channel will remain powered as long as the current drawn by the load satisfies the MPS timing and current requirements. The disabled channel will be re-enabled when the single channel current increases above 75 mA.

Note

4-pair Pcut is disabled whenever a 4-pair port is either in a partial disconnect state or one or both channel currents are below 30mA (typ).

Note

For 4-pair single signature PDs with DCDTxx = 1 and an Assigned Class = 5-8, **both** channels will remain powered until the current on both channels fall below the 4.5mA threshold for the duration of TMPDO + TMPS.

Note

Setting DCDTxx = "0" for a 4P Dual Signature PD or 4P Single Signature PD with assigned class = 5-8 after turn on will result in the use of the 6.5mA threshold per channel which is **non-compliant** to the 802.3bt standard.

Note

For 4-pair Dual Signature PDs, the disconnect threshold will be applied independently per channel. Thus, if either channel falls below the disconnect threshold for the duration of TMPDO + TMPS, only that channel will be disabled while the alternative channel remains powered as long it continues to satisfy the MPS timing and current requirements.

Note

DC Disconnect for 4-Pair ports power on in Manual/Diagnostic mode will behave as independent channels. Thus, if either channel current falls below V_{IMIN} for longer than t_{MPDO} , that channel will be disabled and a disconnect fault will be set (DISFn bits in register 0x06/7).

9.6.2.38 INPUT VOLTAGE Register

COMMAND = 2Eh with 2 Data Byte (LSByte first, MSByte second), Read only

Figure 9-45. INPUT VOLTAGE Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------|--------|--------|--------|--------|-------|-------|
| LSB: | | | | | | | |
| VPWR7 | VPWR6 | VPWR5 | VPWR4 | VPWR3 | VPWR2 | VPWR1 | VPWR0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| MSB: | | | | | | | |
| – | – | VPWR13 | VPWR12 | VPWR11 | VPWR10 | VPWR9 | VPWR8 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-48. INPUT VOLTAGE Register Field Descriptions

| Bit | Field | Type | Reset | Description | | | | | | |
|------|------------------|-------------------|-------|--|------|------------------|-------------------|-----|------|----------|
| 13–0 | VPWR13- VPWR0 | R | 0 | <p>Bit Descriptions: Data conversion result. The I²C data transmission is a 2-byte transfer. 14-bit Data conversion result of input voltage.</p> <p>The equation defining the voltage measured is:</p> $V = N \times V_{STEP}$ <p>Where V_{STEP} is defined below as well as the full scale value:</p> <table border="1" style="margin-left: 20px; border-collapse: collapse; text-align: center;"> <thead> <tr> <th style="width: 15%;">Mode</th> <th style="width: 35%;">Full Scale Value</th> <th style="width: 50%;">V_{STEP}</th> </tr> </thead> <tbody> <tr> <td>Any</td> <td>60 V</td> <td>3.662 mV</td> </tr> </tbody> </table> <p>Note that the measurement is made between VPWR and AGND.</p> | Mode | Full Scale Value | V _{STEP} | Any | 60 V | 3.662 mV |
| Mode | Full Scale Value | V _{STEP} | | | | | | | | |
| Any | 60 V | 3.662 mV | | | | | | | | |

9.6.2.39 CHANNEL 1 CURRENT Register

COMMAND = 30h with 2 Data Byte, (LSByte First, MSByte second), Read Only

Figure 9-46. CHANNEL 1 CURRENT Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------|-------|-------|-------|-------|------|------|
| LSB: | | | | | | | |
| I1_7 | I1_6 | I1_5 | I1_4 | I1_3 | I1_2 | I1_1 | I1_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| MSB: | | | | | | | |
| – | – | I1_13 | I1_12 | I1_11 | I1_10 | I1_9 | I1_8 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.6.2.40 CHANNEL 2 CURRENT Register

COMMAND = 34h with 2 Data Byte, (LSByte First, MSByte second), Read Only

Figure 9-47. CHANNEL 2 CURRENT Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------|-------|-------|-------|-------|------|------|
| LSB: | | | | | | | |
| I2_7 | I2_6 | I2_5 | I2_4 | I2_3 | I2_2 | I2_1 | I2_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| MSB: | | | | | | | |
| – | – | I2_13 | I2_12 | I2_11 | I2_10 | I2_9 | I2_8 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.6.2.41 CHANNEL 3 CURRENT Register

COMMAND = 38h with 2 Data Byte, (LSByte First, MSByte second), Read Only

Figure 9-48. CHANNEL 3 CURRENT Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------|-------|-------|-------|-------|------|------|
| LSB: | | | | | | | |
| I3_7 | I3_6 | I3_5 | I3_4 | I3_3 | I3_2 | I3_1 | I3_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| MSB: | | | | | | | |
| – | – | I3_13 | I3_12 | I3_11 | I3_10 | I3_9 | I3_8 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.6.2.42 CHANNEL 4 CURRENT Register

COMMAND = 3Ch with 2 Data Byte, (LSByte First, MSByte second), Read Only

Figure 9-49. CHANNEL 4 CURRENT Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------|------|------|------|------|------|------|
| LSB: | | | | | | | |
| I4_7 | I4_6 | I4_5 | I4_4 | I4_3 | I4_2 | I4_1 | I4_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| MSB: | | | | | | | |

Figure 9-49. CHANNEL 4 CURRENT Register Format (continued)

| | | | | | | | |
|-----|-----|-------|-------|-------|-------|------|------|
| – | – | I4_13 | I4_12 | I4_11 | I4_10 | I4_9 | I4_8 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-49. CHANNEL n CURRENT Register Field Descriptions

| Bit | Field | Type | Reset | Description | | | | | | |
|----------------------------|---|-------------------|-------|---|------|------------------|-------------------|----------------------------|---|----------|
| 13-0 | In_13- In_0 | R | 0 | <p>Bit Descriptions: Data conversion result. The I²C data transmission is a 2-byte transfer. Note that the conversion is done using a TI proprietary multi-slope integrating converter. 14-bit Data conversion result of current for channel n. The update rate is around once per 100 ms in powered state.</p> <p>The equation defining the current measured is:</p> $I = N \times I_{STEP}$ <p>Where I_{STEP} is defined below as well as the full scale value, according to the operating mode:</p> <table border="1" style="margin-left: 20px; border-collapse: collapse; text-align: center;"> <thead> <tr> <th style="width: 30%;">Mode</th> <th style="width: 35%;">Full Scale Value</th> <th style="width: 35%;">I_{STEP}</th> </tr> </thead> <tbody> <tr> <td>Powered and Classification</td> <td>1.15 A (with 0.255-Ω R_{sense})</td> <td>70.19 μA</td> </tr> </tbody> </table> <p>Note: in any of the following cases, the result through I²C interface is automatically 0000</p> <ul style="list-style-type: none"> channel is in OFF mode channel is OFF while in semiauto mode and detect/class is not enabled channel is OFF while in semiauto mode and detection result is incorrect <p>In diagnostic/manual mode, if detect/class has been enabled at least once, the register retains the result of the last measurement</p> | Mode | Full Scale Value | I _{STEP} | Powered and Classification | 1.15 A (with 0.255-Ω R _{sense}) | 70.19 μA |
| Mode | Full Scale Value | I _{STEP} | | | | | | | | |
| Powered and Classification | 1.15 A (with 0.255-Ω R _{sense}) | 70.19 μA | | | | | | | | |

Note

1.15A is the theoretical full scale range of the ADC based on 14bits * Istep. However, due to performance variation between individual channels, devices, and over temperature, it may be possible that some channels will have a minimum full scale value of 1.05A

Note

For 4-Pair wired ports, these registers still only provide the individual per channel current measurements. The value from both channels need to be added together in order to get the total 4-pair port current reading.

Class Current Reading

Following the completion of any classification measurement on a channel, the measured classification current is reported in these registers until either a port current reading is completed following a port turn on or the port is disabled.

Note

Only the current measurement for the last classification finger is reported. Thus, for a single signature Class 5, 6, 7, and 8 PDs, the reported classification current will report a Class 0, 1, 2, & 3 current level respectively.

9.6.2.43 CHANNEL 1 VOLTAGE Register

COMMAND = 32h with 2 Data Byte, (LSByte First, MSByte second), Read Only

Figure 9-50. CHANNEL 1 VOLTAGE Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------|-------|-------|-------|-------|------|------|
| LSB: | | | | | | | |
| V1_7 | V1_6 | V1_5 | V1_4 | V1_3 | V1_2 | V1_1 | V1_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| MSB: | | | | | | | |
| – | – | V1_13 | V1_12 | V1_11 | V1_10 | V1_9 | V1_8 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.6.2.44 CHANNEL 2 VOLTAGE Register

COMMAND = 36h with 2 Data Byte, (LSByte First, MSByte second), Read Only

Figure 9-51. CHANNEL 2 VOLTAGE Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------|-------|-------|-------|-------|------|------|
| LSB: | | | | | | | |
| V2_7 | V2_6 | V2_5 | V2_4 | V2_3 | V2_2 | V2_1 | V2_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| MSB: | | | | | | | |
| – | – | V2_13 | V2_12 | V2_11 | V2_10 | V2_9 | V2_8 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.6.2.45 CHANNEL 3 VOLTAGE Register

COMMAND = 3Ah with 2 Data Byte, (LSByte First, MSByte second), Read Only

Figure 9-52. CHANNEL 3 VOLTAGE Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------|-------|-------|-------|-------|------|------|
| LSB: | | | | | | | |
| V3_7 | V3_6 | V3_5 | V3_4 | V3_3 | V3_2 | V3_1 | V3_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| MSB: | | | | | | | |
| – | – | V3_13 | V3_12 | V3_11 | V3_10 | V3_9 | V3_8 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.6.2.46 CHANNEL 4 VOLTAGE Register

COMMAND = 3Eh with 2 Data Byte, (LSByte First, MSByte second), Read Only

Figure 9-53. CHANNEL 4 VOLTAGE Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|------|------|------|------|------|------|------|
| LSB: | | | | | | | |
| V4_7 | V4_6 | V4_5 | V4_4 | V4_3 | V4_2 | V4_1 | V4_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| MSB: | | | | | | | |

Figure 9-53. CHANNEL 4 VOLTAGE Register Format (continued)

| | | | | | | | |
|-----|-----|-------|-------|-------|-------|------|------|
| – | – | V4_13 | V4_12 | V4_11 | V4_10 | V4_9 | V4_8 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-50. CHANNEL n VOLTAGE Register Field Descriptions

| Bit | Field | Type | Reset | Description | | | | | | |
|---------|------------------|-------------------|-------|---|------|------------------|-------------------|---------|------|----------|
| 13-0 | Vn_13- Vn_0 | R | 0 | <p>Bit Descriptions: Data conversion result. The I²C data transmission is a 2-byte transfer. The equation defining the voltage measured is:</p> $V = N \times V_{STEP}$ <p>Where V_{STEP} is defined below as well as the full scale value:</p> <table border="1" style="margin-left: 20px; border-collapse: collapse; text-align: center;"> <thead> <tr> <th style="width: 25%;">Mode</th> <th style="width: 25%;">Full Scale Value</th> <th style="width: 25%;">V_{STEP}</th> </tr> </thead> <tbody> <tr> <td>Powered</td> <td>60 V</td> <td>3.662 mV</td> </tr> </tbody> </table> <p>Note that a powered voltage measurement is made between VPWR and DRAINn. Note: if a channel is OFF, the result through I²C interface is automatically 0000.</p> | Mode | Full Scale Value | V _{STEP} | Powered | 60 V | 3.662 mV |
| Mode | Full Scale Value | V _{STEP} | | | | | | | | |
| Powered | 60 V | 3.662 mV | | | | | | | | |

9.6.2.47 2x FOLDBACK SELECTION Register

COMMAND = 40h with 1 Data Byte Read/Write

Figure 9-54. 2x FOLDBACK SELECTION Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|-------|---|---|---|---|
| 2xFB4 | 2xFB3 | 2xFB2 | 2xFB1 | - | - | - | - |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | - | - | - | - |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-51. 2x FOLDBACK SELECTION Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 7-4 | 2xFB4- 2xFB1 | R/W | 0 | <p>When set, this activates the 2x Foldback mode for a channel which increases its I_{LIM} and I_{SHORT} levels normal settings, as shown in Figure 9-3. Note that the fault timer starts when the I_{LIM} threshold is exceeded.</p> <p>Notes:</p> <ol style="list-style-type: none"> 1) At turn on, the inrush current profile is unaffected by these bits, as shown in Figure 9-2. 2) When a 2xFBn bit is deasserted, the t_{LIM} setting used for the associated channel is always the nominal value (approximately 60 ms). If 2xFBn bit is asserted, then t_{LIM} for associated channel is programmable as defined in the Timing Configuration register (0x16). 3) If the assigned class for a channel is class 4 or above, the 2xFB bit will be automatically set during turn on. <p>For a single signature 4-pair powered PD both bits will be set For a dual signature 4-pair powered PD each Channel will be set according to the individually assigned PD classification</p> |

Note

For 4-pair wired Ports the 2xFBn bits **individually** control each Channels operation.

Refer to register 0x55h description for more information on additional Foldback and Inrush configuration options

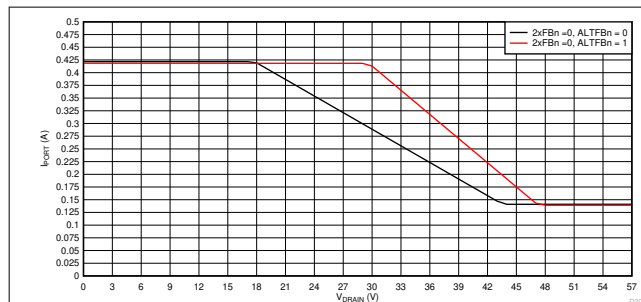


Figure 9-55. 1x Mode (2xFBn = 0) Foldback Curves, I_{PORT} vs V_{DRAIN}

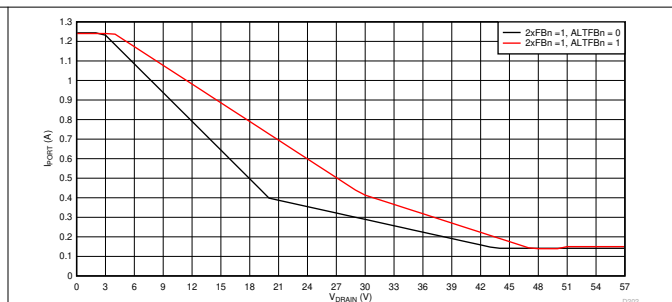


Figure 9-56. 2x Mode (2xFBn = 1) Foldback Curves, I_{PORT} vs V_{DRAIN}

9.6.2.48 FIRMWARE REVISION Register

COMMAND = 41h with 1 Data Byte, Read Only

Figure 9-57. FIRMWARE REVISION Register Format

| | | | | | | | |
|-----|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FRV | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-52. FIRMWARE REVISION Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|--------------------------|
| 7–0 | FRV | R | | Firmware Revision number |

After a RESET or POR fault this value will default to 0000, 0000b, but upon a “valid” SRAM load, this value will reflect the corresponding SRAM version of firmware (0x01h – 0xFEh).

Note

If the value of this register = 0xFFh, the device is running in “safe mode”, and the SRAM needs to be reprogrammed to resume normal operation.

9.6.2.49 I2C WATCHDOG Register

COMMAND = 42h with 1 Data Byte, Read/Write

The I²C watchdog timer monitors the I²C clock line in order to prevent hung software situations that could leave ports in a hazardous state. The timer can be reset by either edge on SCL input. If the watchdog timer expires, all channels will be turned off and WDS bit will be set. The nominal watchdog time-out period is 2 seconds.

Figure 9-58. I2C WATCHDOG Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|-------|-------|-------|-------|-------|
| – | – | – | IWDD3 | IWDD2 | IWDD1 | IWDD0 | WDS |
| – | – | – | R/W-1 | R/W-0 | R/W-1 | R/W-1 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-53. I2C WATCHDOG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|--|
| 4–1 | IWDD3–IWDD0 | R/W | 1011b | I ² C Watchdog disable. When equal to 1011b, the watchdog is masked. Otherwise, it is unmasked and the watchdog is operational. |
| 0 | WDS | R/W | 0 | I ² C Watchdog timer status, valid even if the watchdog is masked. When set, it means that the watchdog timer has expired without any activity on I ² C clock line. Writing 0 at WDS location clears it. Note that when the watchdog timer expires and if the watchdog is unmasked, all channels are also turned off. |

When the channels are turned OFF due to I²C watchdog, the corresponding bits are also cleared:

Table 9-54. I2C WATCHDOG Reset

| Register | Bits to be Reset |
|-----------|--|
| 0x04 | CLSCn and DETCn |
| 0x06 | DISFn and PCUTn |
| 0x08 | STRTn and ILIMn |
| 0x0A/B | PCUTnn |
| 0x0C–0F | Requested Class and Detection |
| 0x10 | PGn and PEn |
| 0x14 | CLEn and DETEn |
| 0x1C | ACn and CCnn |
| 0x1E–21 | 2P Policing set to 0xFFh |
| 0x24 | PFn |
| 0x2A–2B | 4P Policing set to 0xFFh |
| 0x2D | NLMnn, NCTnn, 4PPCTnn, and DCDTnn |
| 0x30–3F | Channel Voltage and Current Measurements |
| 0x40 | 2xFBn |
| 0x44 - 47 | Detection Resistance Measurements |
| 0x4C–4F | Assigned Class and Previous Class |
| 0x51–54 | Autoclass Measurement |

The corresponding PGCn and PECn bits of Power Event register will also be set if there is a change. The corresponding PEn and PGn bits of Power Status Register are also updated accordingly.

Note

If the I²C watchdog timer has expired, the Temperature and Input voltage registers will stop being updated until the WDS bit is cleared. The WDS bit must then be cleared to allow these registers to work normally.

9.6.2.50 DEVICE ID Register

COMMAND = 43h with 1 Data Byte, Read Only

Figure 9-59. DEVICE ID Register Format

| | | | | | | | |
|-----|---|---|---|----|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DID | | | | SR | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-55. DEVICE ID Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------------------|
| 7–5 | DID | R | 0010b | Device ID number |
| 4–0 | SR | R | 0001b | Silicon Revision number |

9.6.2.51 CHANNEL 1 DETECT RESISTANCE Register

COMMAND = 44h with 1 Data Byte, Read Only

Figure 9-60. CHANNEL 1 DETECT RESISTANCE Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|------|------|------|------|
| R1_7 | R1_6 | R1_5 | R1_4 | R1_3 | R1_2 | R1_1 | R1_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.6.2.52 CHANNEL 2 DETECT RESISTANCE Register

COMMAND = 45h with 1 Data Byte, Read Only

Figure 9-61. CHANNEL 2 DETECT RESISTANCE Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|------|------|------|------|
| R2_7 | R2_6 | R2_5 | R2_4 | R2_3 | R2_2 | R2_1 | R2_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.6.2.53 CHANNEL 3 DETECT RESISTANCE Register

COMMAND = 46h with 1 Data Byte, Read Only

Figure 9-62. CHANNEL 3 DETECT RESISTANCE Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|------|------|------|------|
| R3_7 | R3_6 | R3_5 | R3_4 | R3_3 | R3_2 | R3_1 | R3_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.6.2.54 CHANNEL 4 DETECT RESISTANCE Register

COMMAND = 47h with 1 Data Byte, Read Only

Figure 9-63. CHANNEL 4 DETECT RESISTANCE Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|------|------|------|------|
| R4_7 | R4_6 | R4_5 | R4_4 | R4_3 | R4_2 | R4_1 | R4_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-56. DETECT RESISTANCE Register Fields Descriptions

| Bit | Field | Type | Reset | Description | | | | |
|--------------------------|-------------------|------|-------|---|--------------------------|-------------------|---------------|------------|
| 7-0 | Rn_7- Rn_0 | R | 0 | <p>8-bit data conversion result of detection resistance for channel n. Most recent 2-point Detection Resistance measurement result. The I²C data transmission is a 1-byte transfer. Note that the register content is not cleared at turn off. The equation defining the resistance measured is:</p> $R = N \times R_{STEP}$ <p>Where R_{STEP} is defined below as well as the full scale value:</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Useable Resistance Range</th> <th>R_{STEP}</th> </tr> </thead> <tbody> <tr> <td>2 kΩ to 50 kΩ</td> <td>195.3125 Ω</td> </tr> </tbody> </table> | Useable Resistance Range | R _{STEP} | 2 kΩ to 50 kΩ | 195.3125 Ω |
| Useable Resistance Range | R _{STEP} | | | | | | | |
| 2 kΩ to 50 kΩ | 195.3125 Ω | | | | | | | |

9.6.2.55 CHANNEL 1 ASSIGNED CLASS Register

COMMAND = 4Ch with 1 Data Byte, Read Only

Figure 9-64. CHANNEL 1 ASSIGNED CLASS Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|-----|-----|-----|------------|-----|-----|-----|
| AClass Ch1 | | | | PClass Ch1 | | | |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.6.2.56 CHANNEL 2 ASSIGNED CLASS Register

COMMAND = 4Dh with 1 Data Byte, Read Only

Figure 9-65. CHANNEL 2 ASSIGNED CLASS Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|-----|-----|-----|------------|-----|-----|-----|
| AClass Ch2 | | | | PClass Ch2 | | | |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.6.2.57 CHANNEL 3 ASSIGNED CLASS Register

COMMAND = 4Eh with 1 Data Byte, Read Only

Figure 9-66. CHANNEL 3 ASSIGNED CLASS Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|-----|-----|-----|------------|-----|-----|-----|
| AClass Ch3 | | | | PClass Ch3 | | | |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.6.2.58 CHANNEL 4 ASSIGNED CLASS Register

COMMAND = 4Fh with 1 Data Byte, Read Only

Figure 9-67. CHANNEL 4 ASSIGNED CLASS Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|-----|-----|-----|------------|-----|-----|-----|
| AClass Ch4 | | | | PClass Ch4 | | | |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Bit Descriptions: These bits represent the "assigned" and previous classification results for channel n. These bits are cleared when channel n is turned off.

Table 9-57. CHANNEL n ASSIGNED CLASS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|---|
| 7-4 | ACLASS Ch-n | R | 0 | Assigned classification on channel n. See Table 9-58 below |
| 3-0 | PCLASS Ch-n | R | 0 | Previous Class result on channel n. See Table 9-59 below |

Table 9-58. Assigned Class Designations

| ACLASS-Chn | | | | Assigned Class |
|------------|-------|-------|-------|-----------------------------------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | |
| 0 | 0 | 0 | 0 | Unknown |
| 0 | 0 | 0 | 1 | Class 1 |
| 0 | 0 | 1 | 0 | Class 2 |
| 0 | 0 | 1 | 1 | Class 3 |
| 0 | 1 | 0 | 0 | Class 4 |
| 0 | 1 | 0 | 1 | Reserved |
| 0 | 1 | 1 | 0 | Reserved |
| 0 | 1 | 1 | 1 | Reserved |
| 1 | 0 | 0 | 0 | Class 5 - 4-Pair Single Signature |
| 1 | 0 | 0 | 1 | Class 6 - 4-Pair Single Signature |
| 1 | 0 | 1 | 0 | Class 7 - 4-Pair Single Signature |
| 1 | 0 | 1 | 1 | Class 8 - 4-Pair Single Signature |
| 1 | 1 | 0 | 0 | Reserved |
| 1 | 1 | 0 | 1 | Class 5 - 4-Pair Dual Signature |
| 1 | 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | 1 | Reserved |

Table 9-59. Previous Class Designations

| PCLASS-Chn | | | | Previous Class |
|------------|-------|-------|-------|-----------------------------------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | |
| 0 | 0 | 0 | 0 | Unknown |
| 0 | 0 | 0 | 1 | Class 1 |
| 0 | 0 | 1 | 0 | Class 2 |
| 0 | 0 | 1 | 1 | Class 3 |
| 0 | 1 | 0 | 0 | Class 4 |
| 0 | 1 | 0 | 1 | Reserved |
| 0 | 1 | 1 | 0 | Class 0 |
| 0 | 1 | 1 | 1 | Reserved |
| 1 | 0 | 0 | 0 | Class 5 - 4-Pair Single Signature |
| 1 | 0 | 0 | 1 | Class 6 - 4-Pair Single Signature |
| 1 | 0 | 1 | 0 | Class 7 - 4-Pair Single Signature |
| 1 | 0 | 1 | 1 | Class 8 - 4-Pair Single Signature |
| 1 | 1 | 0 | 0 | Reserved |
| 1 | 1 | 0 | 1 | Class 5 - 4-Pair Dual Signature |
| 1 | 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | 1 | Reserved |

“Requested” vs. “Assigned” Classification:

The “requested” class is the classification the PSE measures during Mutual Identification prior to turn on, whereas the “assigned” class is the classification level the Channel was powered on with based on the Power Allocation setting in register 0x29h. The “requested” classification values are available in registers 0x0C-0F

For a 4-pair single signature device, both channels will report the same assigned PD classification within 5ms after classification is completed. However, only the channel that classification was measured on will have the CLSCn bit set in register 0x04h

For a 4-pair dual signature device each Channel will reports its own individually assigned PD classification within 5ms of turn on.

Note

Upon being powered, devices that present a class 0 signature during discovery will be given an assigned class of "Class 3"

Note

There is no Assigned Class assigned for ports/channels powered out of Manual/Diagnostic mode. Any settings such as the port power policing and 1x/2x foldback selection that are typically configured based on the assigned class result need to be manually configured by the user.

Previous Classification

In certain circumstances the requested class result in 0x0C-0F can not properly reflect the actual classification of the PD connected to the port/channel. This will happen when a port has a power allocation limit of 15.4W and the PSE can only provide 1 classification finger during turn on. When this occurs and if the device is configured to run in Semi Auto mode with det and cls enabled, the 3-finger classification measurement that preceded the turn on detection and classification cycle will be stored here. This information can be useful in scenarios where a port had to be demoted to stay under the system power limit at turn on but additional power budget comes available later on.

Note

The Previous Classification results are only valid for channels being used in semi auto mode with ongoing discovery (DETE and CLE = 1).

9.6.2.59 AUTO CLASS CONTROL Register

COMMAND = 50h with 1 Data Byte, Read/Write

Figure 9-68. AUTO CLASS CONTROL Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| MAC4 | MAC3 | MAC2 | MAC1 | AAC4 | AAC3 | AAC2 | AAC1 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-60. AUTO CLASS CONTROL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-------|-------|------|-------|---|
| 7 - 4 | MACn | R/W | 0 | Manual Auto Class Measurement bits 1 = Manual Auto Class Measurement enabled 0 = Manual Auto Class measurement complete The auto class measurement will begin within 10ms of this bit being set. This bit will be cleared by the internal firmware within 1ms of the updated Autoclass measurement result(s) in 0x51-54h. |
| 3 - 0 | AACn | R/W | 0 | Auto Class Auto Adjustment Enable bits 1 = Autoclass auto adjust is enabled and the corresponding PCUT settings will be automatically adjusted based on the measured autoclass power 0 = Autoclass auto adjust is disabled and it is up to the user to adjust the value of PCUT as desired. |

Note

Any MACn bits set prior to turn on will be ignored and cleared during turn on.

Auto Class Pcut Adjustments:

If the ACx bit(s) are set in register 0x50h, the TPS23880 will automatically adjust its PCUT value based on the auto class power measurement (P_{AC} in registers 0x51-54) and Any Automatic Auto Class facilitated (AACn = 1) PCut adjustments will be made within 5 ms of the end of the auto class measurement period.

If the AACn bits are not set, the table and equations below should be used to make any PCUT adjustments based on the auto class power measurement (P_{AC}).

Table 9-61. Typical Auto Class Margins by Measured Power

| Auto Class Measured Power (P_{AC}) | P_{AC_MARGIN} |
|--|------------------|
| $P_{AC} < 18.5\text{ W}$ | 0.5 W |
| $19\text{ W} < P_{AC} < 25.5\text{ W}$ | 1 W |
| $26\text{ W} < P_{AC} < 36.5\text{ W}$ | 2 W |
| $36.5\text{ W} < P_{AC} < 45\text{ W}$ | 3 W |
| $45\text{ W} < P_{AC} < 51.5\text{ W}$ | 4 W |
| $51.5\text{ W} < P_{AC} < 58\text{ W}$ | 5 W |
| $58\text{ W} < P_{AC} < 63\text{ W}$ | 6 W |
| $63\text{ W} < P_{AC} < 68\text{ W}$ | 7W |
| $68\text{ W} < P_{AC} < 73\text{ W}$ | 8W |
| $P_{AC} > 73\text{ W}$ | 9W |

Note

For a PSE supporting Auto Class, the P_{AC_MARGIN} is an IEEE required surplus of power over the measured power during auto class that allows for component degradation over time.

For 2-Pair or Dual Signature 4-Pair PDs, only the 2P-PCut values will be updated based on each pair sets measured PAC according to the equation below.

$$2P\text{-PCut} = P_{AC} + P_{AC_MARGIN}$$

For Single signature 4-Pair PDs, the sum of the autoclass power measurements on each pair set will be used to determine the 4P-PCut setting according to the equation below:

$$4P\text{-PCut} = P_{AC_ALTA} + P_{AC_ALTB} + P_{AC_MARGIN}$$

For Single signature 4-Pair PDs, the auto class measurements will have no impact on the 2P-PCut settings. These values will remain unchanged from the 2P-Pcut settings prior to the start of the auto class measurement.

Note

For 4-pair wired ports with single signature connected devices:

if only one AACn bit is set and an autoclass power measurement is completed (manual or during turn on), the 4-PCut value will still be updated based on the power measurement

If only one MACn bit is set, no autoclass measurement will be completed.

Note

If the result of $P_{AC} + P_{AC_MARGIN}$ is **above** a Channel's assigned classification range, no changes will be made to the either the 2P or 4P Pcut settings.

9.6.2.60 CHANNEL 1 AUTO CLASS POWER Register

COMMAND = 51h with 1 Data Byte, Read Only

Figure 9-69. CHANNEL 1 AUTO CLASS POWER Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|--------|--------|--------|--------|--------|--------|--------|
| - | PAC1_6 | PAC1_5 | PAC1_4 | PAC1_3 | PAC1_2 | PAC1_1 | PAC1_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.6.2.61 CHANNEL 2 AUTO CLASS POWER Register

COMMAND = 52h with 1 Data Byte, Read Only

Figure 9-70. CHANNEL 2 AUTO CLASS POWER Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|--------|--------|--------|--------|--------|--------|--------|
| - | PAC2_6 | PAC2_5 | PAC2_4 | PAC2_3 | PAC2_2 | PAC2_1 | PAC2_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.6.2.62 CHANNEL 3 AUTO CLASS POWER Register

COMMAND = 53h with 1 Data Byte, Read Only

Figure 9-71. CHANNEL 3 AUTO CLASS POWER Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|--------|--------|--------|--------|--------|--------|--------|
| - | PAC3_6 | PAC3_5 | PAC3_4 | PAC3_3 | PAC3_2 | PAC3_1 | PAC3_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.6.2.63 CHANNEL 4 AUTO CLASS POWER Register

COMMAND = 54h with 1 Data Byte, Read Only

Figure 9-72. CHANNEL 4 AUTO CLASS POWER Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|--------|--------|--------|--------|--------|--------|--------|
| - | PAC4_6 | PAC4_5 | PAC4_4 | PAC4_3 | PAC4_2 | PAC4_1 | PAC4_0 |
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-62. AUTO CLASS POWER Register Fields Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|--|
| 6-0 | PACn_6- PACn_0 | R | 0 | 8-bit data conversion result of the auto class power measurement for channel n. Peak average power calculation result from channel voltage and current data conversion measurements taken during the auto class power measurement window. The equation defining the auto class power measured is: $P_{AC} = N \times P_{AC_STEP}$ Where, when assuming 0.255-Ω Rsense resistor is used: $P_{CSTEP} = 0.5 \text{ W}$ |

Note

The IEEE requires a surplus of power (defined as P_{AC_MARGIN}) to be available over the measured auto class power to allow for component degradation over time. See [Table 9-61](#) for the relationship between P_{AC} and P_{AC_MARGIN}

9.6.2.64 ALTERNATIVE FOLDBACK Register

COMMAND = 55h with 1 Data Byte, Read/Write

Figure 9-73. ALTERNATIVE FOLDBACK Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| ALTFB4 | ALTFB3 | ALTFB2 | ALTFB1 | ALTIR4 | ALTIR3 | ALTIR2 | ALTIR1 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-63. ALTERNATIVE FOLDBACK Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|--|
| 7-4 | ALTFBn | R | 0 | Alternative Foldback Enable bits: Used to enable the operational alternative foldback curves while powered. 1 = Alternative Foldback is enabled 0 = Alternative Foldback is disabled The ALTFBn bits should be set prior to issuing a PWONn command to ensure the desired foldback curve is being used. |
| 3-0 | ALTIRn | R | 0 | Alternative Inrush Enable bits: Used to enable the alternative foldback curves during inrush on channel n 1 = Alternative Inrush is enabled 0 = Alternative Inrush is disabled Note: The ALTIRn bits need to be set prior to sending a PWONn command to ensure the desired inrush behavior is followed |

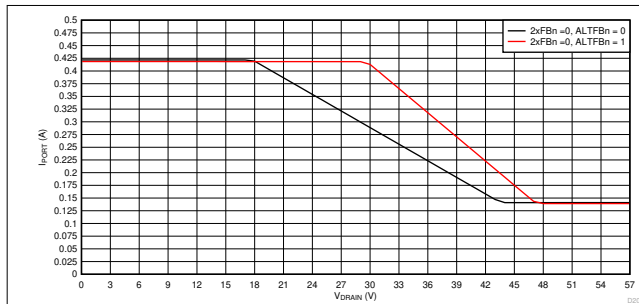


Figure 9-74. 1x Mode (2xFBn = 0) Foldback Curves, I_{PORT} vs V_{DRAIN}

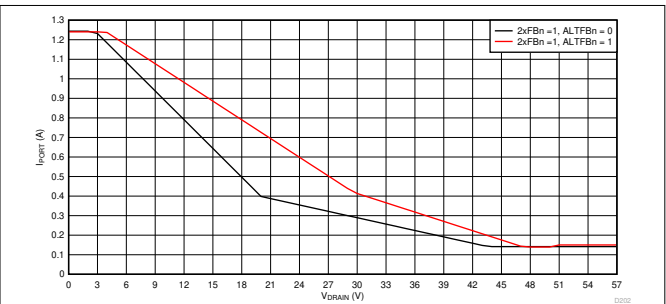


Figure 9-75. 2x Mode (2xFBn = 1) Foldback Curves, I_{PORT} vs V_{DRAIN}

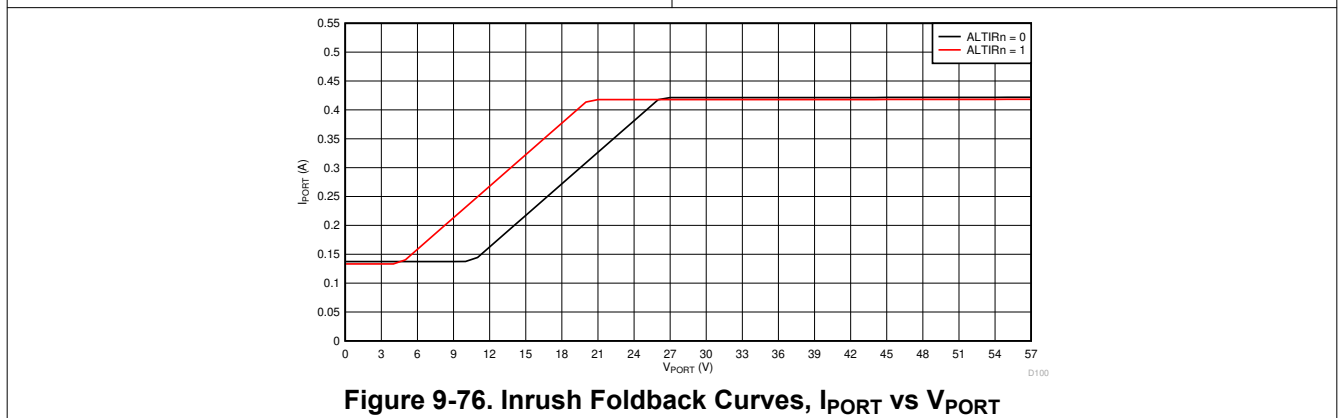


Figure 9-76. Inrush Foldback Curves, I_{PORT} vs V_{PORT}

9.6.2.65 SRAM CONTROL Register

COMMAND = 60h with 1 Data Byte, Read/Write

Figure 9-77. SRAM CONTROL Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---------|-------|--------|--------|---------|-------|---------|
| PROG_SEL | CPU_RST | - | PAR_EN | RAM_EN | PAR_SEL | R/WZ | CLR_PTR |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-64. SRAM CONTROL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|---|
| 7 | PROG_SEL | R/W | 0 | I2C Programming select bit. 1 = SRAM I2C read/write is enabled 0 = SRAM I2C read/write is disabled. |
| 6 | CPU_RST | R/W | 0 | CPU Reset bit 1 = Internal CPU is held in RESET 0 = Internal CPU is active This is strictly a CPU reset. Toggling this bit reset the cpu only and will not change any contents of the I ² C registers |
| 5 | Reserved | R/W | 0 | Reserved |
| 4 | PAR_EN | R/W | 0 | SRAM Parity Enable bit: 1 = SRAM Parity Check will be enabled 0 = SRAM Parity Check will be disabled It is recommended that the Parity function be enable whenever SRAM is being used |
| 3 | RAM_EN | R/W | 0 | SRAM Enable bit 1 = SRAM will be enabled and the internal CPU will run from both SRAM and internal ROM 0 = Internal CPU will run from internal ROM only This bit needs to be set to a 1 after SRAM programing to enable the utilization of the SRAM code |
| 2 | PAR_SEL | R/W | 0 | SRAM Parity Select bit: Setting this bit to a 1 in conjunction with the RZ/W bit enables access to the SRAM Parity bits. 1 = Parity bits read/write is enabled 0 = Parity bits read/write is disabled |
| 1 | R/WZ | R/W | 0 | SRAM Read/Write select bit: 0 = SRAM Write – SRAM data is written with a write to 0x61h 1 = SRAM Read – SRAM data is read with a read from 0x61h SRAM data can be continuously read/written over I2C until a STOP bit is sent. |
| 0 | CLR_PTR | R/W | 0 | Clear Address Pointer bit: 1 = Resets the memory address pointer 0 = Releases pointer for use In order to ensure proper programming, this bit should be toggled (0-1-0) to writing or reading the SRAM or Parity memory. |

9.6.2.65.1 SRAM START ADDRESS (LSB) Register

COMMAND = 62h with 1 Byte, Read/Write

Figure 9-78. SRAM START ADDRESS (LSB) Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| SA_7 | SA_6 | SA_5 | SA_4 | SA_3 | SA_2 | SA_1 | SA_0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.6.2.65.2 SRAM START ADDRESS (MSB) Register

COMMAND = 63h with 1 Byte, Read/Write

Figure 9-79. SRAM START ADDRESS (MSB) Register Format

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| SA_15 | SA_14 | SA_13 | SA_12 | SA_11 | SA_10 | SA_9 | SA_8 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

9.6.2.65.3

Table 9-65. SRAM START ADDRESS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|------|-------------|------|-------|--|
| 15-0 | SA_15- SA_0 | R/W | 0 | SRAM and Parity Programming Start Address bits: the value entered into these registers sets the start address location for the SRAM or Parity programming |

SRAM Programming:

Upon power up, the TPS23880 device requires the SRAM to be programmed via I²C to ensure proper operation and IEEE complaint performance. All I²C traffic other than those commands required to program the SRAM should be deferred until after the SRAM programming sequences are completed.

Note

The latest version of firmware and SRAM release notes may be accessed from the [TI mySecure Software](#) webpage.

The SRAM Release Notes and ROM Advisory document includes more detailed information regarding any know issues and changes that were associated with each firmware release.

Note

The SRAM programming control must be completed at the lower I2C address (Channels 1-4, A0 = 0). Configuring this registers for the upper I2C device address (Channels 5-8) will not program the SRAM

For systems that include multiple TPS23880 devices, the 0x7F "global" broadcast I2C address may be used to programmed all of the devices at the same time.

Note

The SRAM programming needs to be delayed at least 50ms from the initial power on (VPWR and VDD above UVLO) of the device to allow for the device to complete its internal hardware initialization process

Note

For more detailed instructions on the SRAM programing procedures please refer the [How to Load TPS2388x SRAM Code](#) document on TI.com.

0x60h setup for SRAM Programming: Prior to programming/writing the SRAM, the following bits sequence needs to be completed in register 0x60h:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---------|---|--------|--------|---------|-------|-----------|
| PROG_SEL | CPU_RST | - | PAR_EN | RAM_EN | PAR_SEL | R/WZ | CLR_PTR |
| 0 → 1 | 0 → 1 | 0 | 0 | 0 | 0 | 1 → 0 | 0 → 1 → 0 |

The same sequence is required to read the SRAM with the exception that the R/WZ bit needs to be set to "1".

If the device is in "Safe Mode", the same sequence as above may be used to reprogram the SRAM.

An I²C write to 0x61h following this sequence actively programs the SRAM program memory starting from the address set in registers 0x62h and 63h.

0x60h setup for SRAM Parity Programming: Following the programming of the SRAM program memory, the following bits sequence needs to be completed in register 0x60h in order to configure the device to program the Parity memory:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---------|---|--------|--------|---------|-------|-----------|
| PROG_SEL | CPU_RST | - | PAR_EN | RAM_EN | PAR_SEL | R/WZ | CLR_PTR |
| 0 → 1 | 0 → 1 | 0 | 0 | 0 | 0 → 1 | 1 → 0 | 0 → 1 → 0 |

The same sequence is required to read the Parity with the exception that the R/WZ bit needs to be set to “1”.

An I²C write to 0x61h following this sequence actively programs the Parity memory starting from the address set in registers 0x62h and 63h.

0x60h setup to run from SRAM Program Memory: Upon completion of programming, the following bits sequence needs to be completed in register 0x60h in order to enable the device to run properly out of SRAM:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---------|---|--------|--------|---------|------|---------|
| PROG_SEL | CPU_RST | - | PAR_EN | RAM_EN | PAR_SEL | R/WZ | CLR_PTR |
| 1 → 0 | 1 → 0 | 0 | 0 → 1 | 0 → 1 | 1 → 0 | 0 | 0 |

Within 1ms of the completion of the above sequence, the device will complete a compatibility check on the SRAM

If the SRAM load is determined to be “Valid”: Register 0x41h will have a value between 0x01h and 0xFEh, and the device will return to normal operation.

If the SRAM load is determined to be “Invalid”:

- 0x41h will be set to 0xFFh
- The RAM_EN bit will be internally cleared
- The device will operating in “safe mode” until another programming attempt is completed

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS23880 is an 8-channel, IEEE 802.3bt ready PoE PSE controller and can be used in high port count semiauto or fully micro-controller managed applications (The MSP430FR5969 micro-controller is recommended for most applications). Subsequent sections describe detailed design procedures for applications with different requirements including host control.

The schematic of [Figure 10-1](#) depicts semiauto mode operation of the TPS23880, providing functionality to power PoE loads. The TPS23880 can do the following:

1. Performs load detection.
2. Performs classification for type-1 (one finger) through type-4 (five finger) loads.
3. Enables power on with protective foldback current limiting, and Port power policing (P_{CUT}) value.
4. Shuts down in the event of fault loads and shorts.
5. Performs Maintain Power Signature function to insure removal of power if load is disconnected.
6. Undervoltage lock out occurs if VPWR falls below V_{PUV_F} (typical 26.5 V).

Following a power-off command, disconnect or shutdown due to a Start, P_{CUT} or I_{LIM} fault, the port powers down. Following port power off due to a disconnect, the TPS23880 will immediately restart the detection and classification cycles if the DETE and CLE bits are set in register 0x14. If the shutdown is due to a start, P_{CUT} or I_{LIM} fault, the TPS23880 enters into a cool-down period during which any Detect/Class Enable Command for that port will be delayed. At the end of cool down cycle, one or more detection/class cycles are automatically restarted if the class and/or detect enable bits are set. If a port is disabled using the power off command, the DETE and CLE bits will be cleared and these bits will need to be reset over I²C in order for detection and classification to resume.

10.1.1 Introduction to PoE

Power-over-Ethernet (PoE) is a means of distributing power to Ethernet devices over the Ethernet cable using either data or spare pairs. PoE eliminates the need for power supplies at the Ethernet device. Common applications of PoE are security cameras, IP Phones and wireless access points (WAP). The host or mid-span equipment that supplies power is the power source equipment (PSE). The load at the Ethernet connector is the powered device (PD). PoE protocol between PSE and PD controlling power to the load is specified by IEEE 802.3bt standard. Transformers are used at Ethernet host ports, mid-spans and hubs, to interface data to the cable. A DC voltage can be applied to the center tap of the transformer with no effect on the data signals. As in any power transmission line, a relatively high voltage (approximately 50 V) is used to keep currents low and minimize the effects of IR drops in the line to preserve power delivery to the load. Standard 2-Pair PoE delivers approximately 13 W to a type 1 PD, and 25.5 W to a type 2 PD, whereas standard 4-Pair PoE will be capable of delivering approximately 51 W to a type 3 PD and 71 W to a type 4 PD.

10.1.1.1 2-Pair Versus 4-Pair Power and the New IEEE802.3bt Standard

The IEEE 802.3at-2009 standard previously expanded PoE power delivery from 15.4W (Commonly referred to as .af or Type-1 PoE) to 30 W (.at or Type-2 PoE) of sourced power from the PSE (Power Sourcing Equipment) over 2-pairs of ethernet wires (Commonly known as either the Alt-A or Alt-B pair sets). The IEEE 802.3bt standard further expands power delivery up to 90 W sourced from a PSE by allowing for power delivery over both the ALT-A and ALT-B pairsets in parallel. Two new PoE equipment "Types" have also been created as part of the new standard. Type 3 PSE equipment will be capable of sourcing up to 60 W of power over 4-pair or 30 W over 2-pair while supporting the new MPS requirements. Type 4 PSE equipment will be capable of sourcing up to 90 W of power over 4-pair. The TPS23880 has been designed to be fully configurable to support any of these configurations.

The Maintain Power Signature (or MPS) requirements have also been updated for the new standard. The previous version of the standard only required PSEs to maintain power on a port if the PD (Powered Device) current exceeded 10 mA for at least 60 ms every 300 ms to 400 ms. By decreasing these requirements to 6 ms every 320 ms to 400 ms, the minimum power requirement to maintain PoE power have been reduced by a factor of nearly 10.

10.2 Typical Application

This typical application shows an eight (2-Pair) port, semiauto mode application using a MSP430 or similar micro-controller. Operation in any mode requires I²C host support. The TPS23880 provides useful telemetry in multi-port applications to aid in implementing port power management.

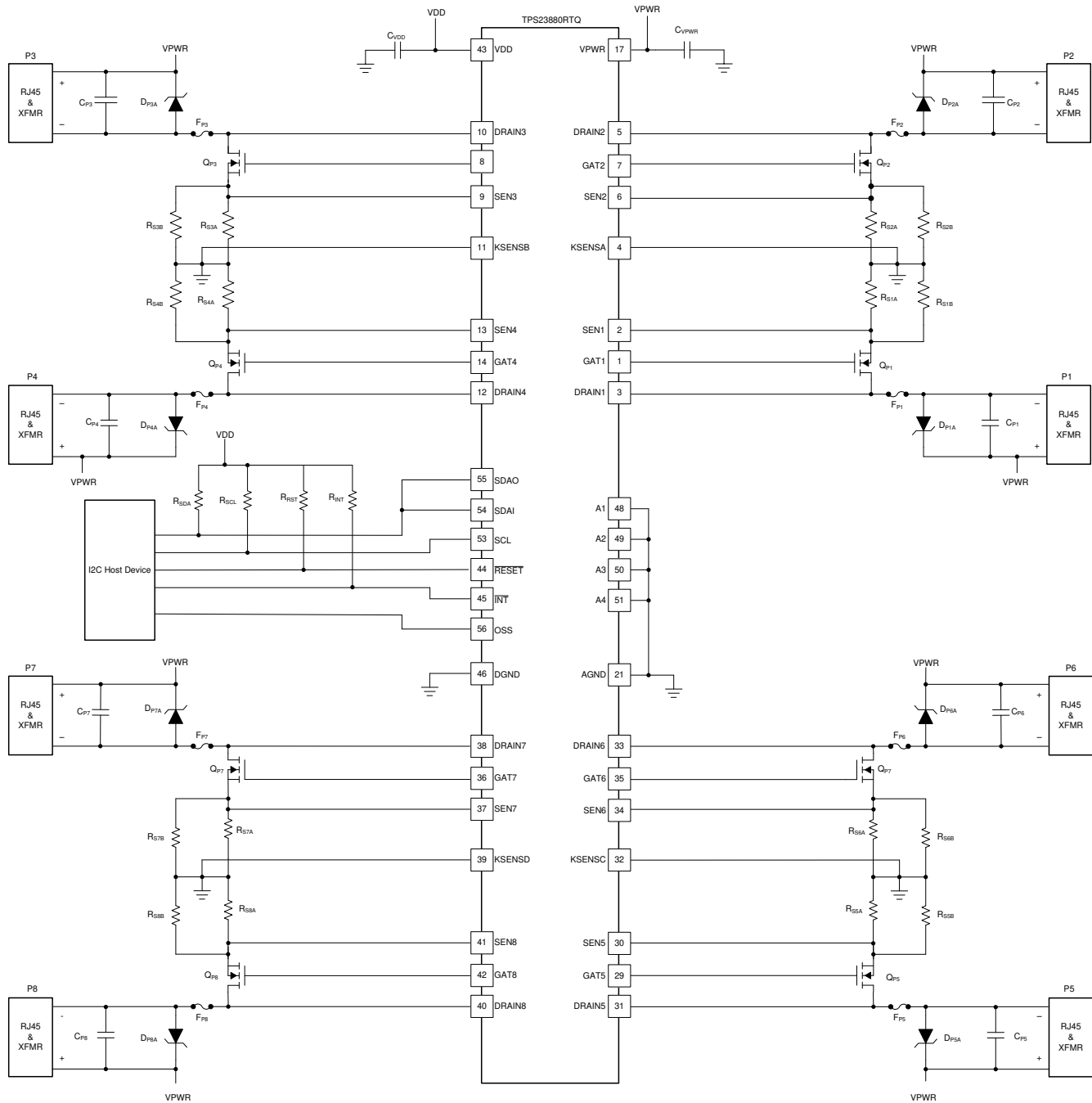


Figure 10-1. Eight 2-Pair Port Application

This typical application shows a four (4-Pair) port, semiauto mode application using a MSP430 or similar microcontroller.

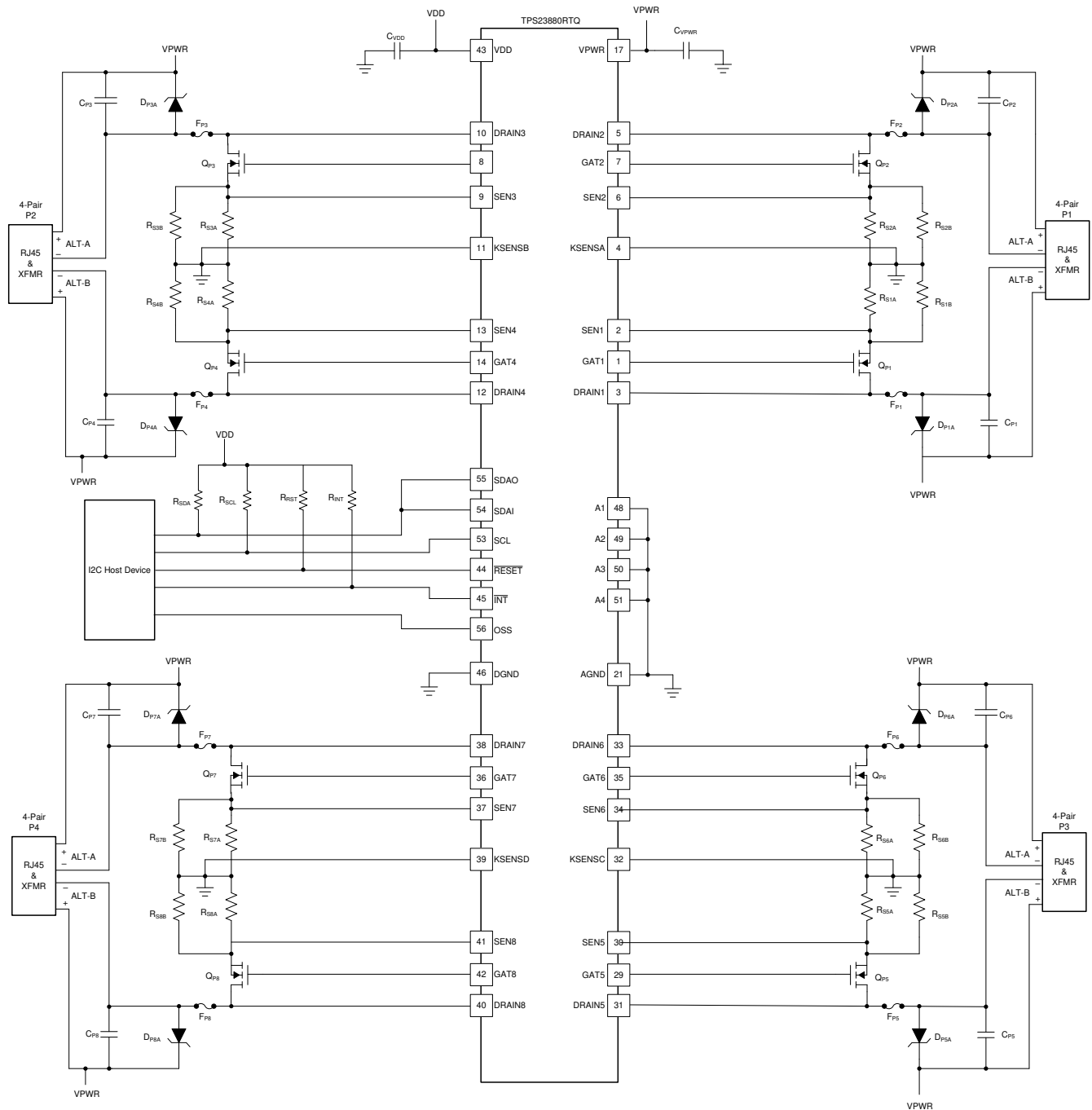


Figure 10-2. Four 4-Pair Port Application

10.2.1 Design Requirements

TPS23880 devices are used in the eight port configuration and are managed by the I²C host device. The I²C address for TPS23880 is programmed using the A4..A1 pins. When using multiple TPS23880 devices in a system, each device requires by a unique I²C address. See [Section 9.6.2.13](#) for more information on how to program the TPS23880 I²C address.

[Figure 10-1](#) and [Figure 10-2](#) show typical application for either all 2-pair or 4-pair ports, but the TPS23880 may also be configured to support any combination of either 2-pair or 4-pair PSE ports. 4-pair port requires the use of both Alternative A and Alternative B wire pair sets at the RJ45 terminal, whereas a 2-pair port only requires the Alternative A pair set to be used.

A MCU is not required to operate the TPS23880 device, but some type of I²C master/host controller device is required to program the internal SRAM and initialize the basic I²C register configuration of the TPS23880.

It is recommended that the $\overline{\text{RESET}}$ pin be connected to a micro-controller or other external circuitry.

Note

The $\overline{\text{RESET}}$ pin must be held low until both VPWR and VDD are above their UVLO thresholds.

Refer to the [TPS23880EVM User's Guide](#) for more detailed information.

10.2.2 Detailed Design Procedure

Refer to the [TPS23880EVM User's Guide](#) for more detailed information on component selection and layout recommendations.

10.2.2.1 Connections on Unused Channels

On unused channels, it is recommended to ground the SENx pin and leave the GATx pin open. DRAINx pins can be grounded or left open (leaving open may slightly reduce power consumption). [Figure 10-3](#) shows an example of an unused PORT2.

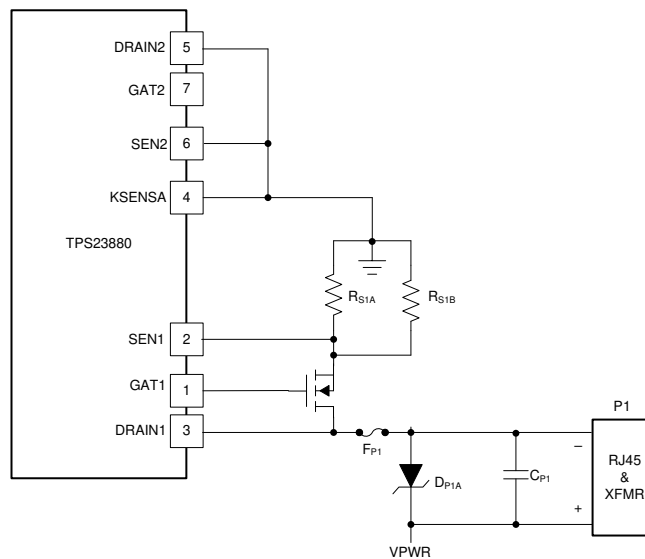


Figure 10-3. Unused PORT2 Connections

10.2.2.2 Power Pin Bypass Capacitors

- **C_{VPWR}**: 0.1 μ F, 100 V, X7R ceramic at pin 17 (VPWR)
- **C_{VDD}**: 0.1 μ F, 5 V, X7R ceramic at pin 43 (VDD)

10.2.2.3 Per Port Components

- **C_{Pn}**: 0.1- μ F, 100-V, X7R ceramic between VPWR and Pn-
- **R_{SnA} / R_{SnB}**: Each channel's current sense resistors are a combination of two 0.51- Ω , 1% resistors in parallel (0.255 Ω). Dual 0.51- Ω , 1%, 0.25-W resistors in an 0805 SMT package are recommended. If a 90W Policing (**P_{CUT}**) threshold is selected, the maximum power dissipation for the resistor pair becomes approximately 212 mW (approximately 106 mW each).
- **Q_{Pn}**: The port MOSFET can be a small, inexpensive device with average performance characteristics. **BV_{DSS}** should be 100 V minimum. Target a MOSFET **R_{DS(on)}** at **V_{GS} = 10 V** of between 50 m Ω and 150 m Ω . The MOSFET GATE charge (**Q_G**) and input capacitance (**C_{ISS}**) should be less than 50 nC and 2000 pF respectively. The maximum power dissipation for **Q_{Pn}** with **R_{DS(on)} = 100 m Ω** at 640 mA nominal policing (**I_{CUT}**) threshold is approximately 45 mW.

Note

In addition to the MOSFET **R_{DS(on)}** and **BV_{DSS}** characteristics, the power MOSFET SOA ratings also need to be taken into consideration when selecting these components for your system design. It is recommended that a MOSFET be chosen with an SOA rating that exceeds the inrush and operational foldback characteristic curves as shown in [Figure 9-2](#) and [Figure 9-3](#). When using the standard current foldback (**ALTIRn** or **ALTFBn = 0**) options, the CSD19538Q3A 100V N-Channel MOSFET is recommended.

- **F_{Pn}**: The port fuse should be a slow blow type rated for at least 60 VDC and above approximately 2 x **P_{CUT}** (max). The cold resistance should be below 200 m Ω to reduce the DC losses. The power dissipation for **F_{Pn}** with a cold resistance of 180 m Ω at maximum **P_{CUT}** is approximately 150 mW.
- **D_{PnA}**: The port TVS should be rated for the expected port surge environment. **D_{PnA}** should have a minimum reverse standoff voltage of 58 V and a maximum clamping voltage of less than 95 V at the expected peak surge current

10.2.2.4 System Level Components (not shown in the schematic diagrams)

The system TVS and bulk VPWR capacitance work together to protect the PSE system from surge events which could cause VPWR to surge above 70 V. The TVS and bulk capacitors should be placed on the PCB such that all TPS23880 ports are adequately protected.

- **TVS:** The system TVS should be rated for the expected peak surge power of the system and have a minimum reverse standoff voltage of 58 V. Together with the VPWR bulk capacitance, the TVS must prevent the VPWR rail from exceeding 70 V.
- **Bulk Capacitor:** The system bulk capacitor(s) should be rated for 100 V and can be of aluminum electrolytic type. Two 47- μ F capacitors can be used for each TPS23880 on board.
- **Distributed Capacitance:** In higher port count systems, it may be necessary to distribute 1- μ F, 100-V, X7R ceramic capacitors across the 54-V power bus. One capacitor per each TPS23880 pair is recommended.
- **Digital I/O Pullup Resistors:** $\overline{\text{RESET}}$ and A1-A4 are internally pulled up to VDD, while OSS is internally pulled down, each with a 50-k Ω (typical) resistor. A stronger pull-up/down resistor can be added externally such as a 10 k Ω , 1%, 0.063 W type in a SMT package. SCL, SDAI, SDAO, and INT require external pull-up resistors within a range of 1 k Ω to 10 k Ω depending on the total number of devices on the bus .
- **Ethernet Data Transformer (per port):** The Ethernet data transformer must be rated to operate within the IEEE802.3bt standard in the presence of the DC port current conditions. The transformer is also chosen to be compatible with the Ethernet PHY. The transformer may also be integrated into the RJ45 connector and cable terminations.
- **RJ45 Connector (per port):** The majority of the RJ45 connector requirements are mechanical in nature and include tab orientation, housing type (shielded or unshielded), or highly integrated. An integrated RJ45 consists of the Ethernet data transformer and cable terminations at a minimum. The integrated type may also contain the port TVS and common mode EMI filtering.
- **Cable Terminations (per port):** The cable terminations typically consist of series resistor (usually 75 Ω) and capacitor (usually 10 nF) circuits from each data transformer center tap to a common node which is then bypassed to a chassis ground (or system earth ground) with a high-voltage capacitor (usually 1000 pF to 4700 pF at 2 kV).

10.2.3 Application Curves

Unless otherwise noted, measurements taken on the TPS23880 EVM and Sifos PSA-3000 PowerSync Analyzer with PSA3202 test cards. Test conditions are $T_J = 25\text{ }^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$, $V_{PWR} = 54\text{ V}$, $V_{DGND} = V_{AGND}$, DGND, KSENSA, KSENSB, KSENSC and KSENSD connected to AGND, and all outputs are unloaded, $2x\text{FBn} = 0$. Positive currents are into pins. $R_S = 0.255\text{ }\Omega$, to KSENSA (SEN1 or SEN2), to KSENSB (SEN3 or SEN4), to KSENSC (SEN5 or SEN6) or to KSENSD (SEN7 or SEN8). All voltages are with respect to AGND unless otherwise noted. Operating registers loaded with default values unless otherwise noted.

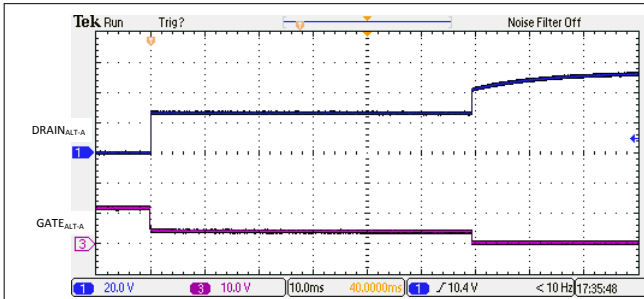


Figure 10-4. 2-Pair I_{LIM} Foldback and Turn Off

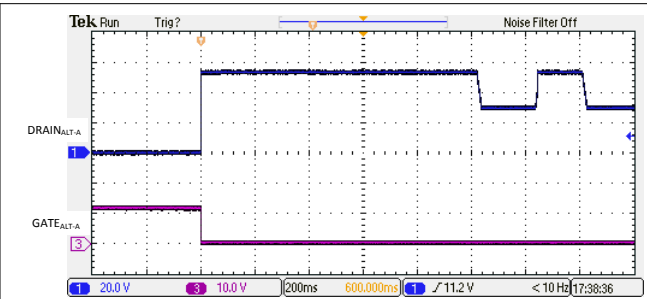


Figure 10-5. 2-Pair Backoff due to PCut Fault

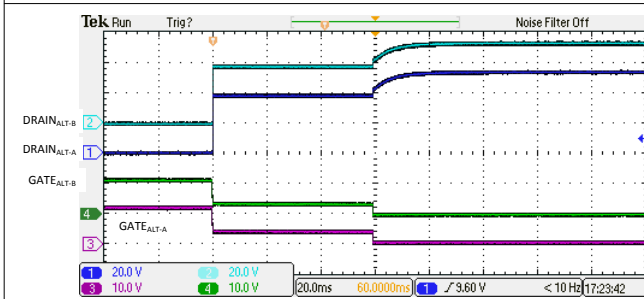


Figure 10-6. 4-Pair I_{LIM} Foldback and Turn Off

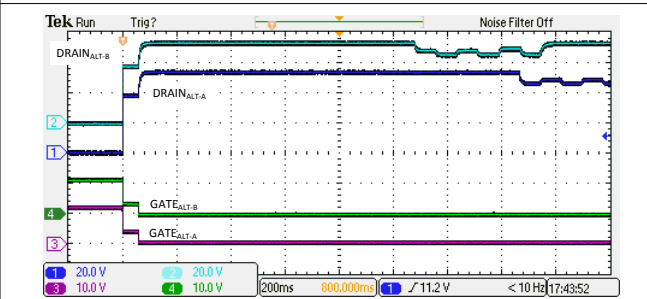


Figure 10-7. 4-Pair Backoff Due to I_{LIM} Fault

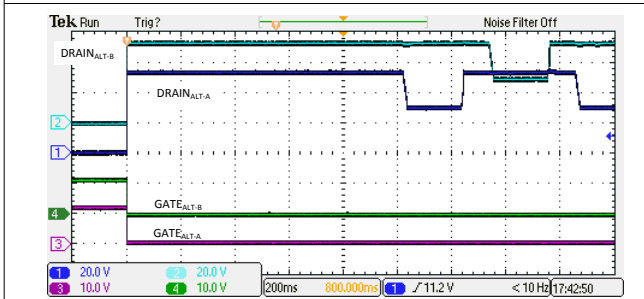


Figure 10-8. 4-Pair Backoff Due to 4PPCut Fault

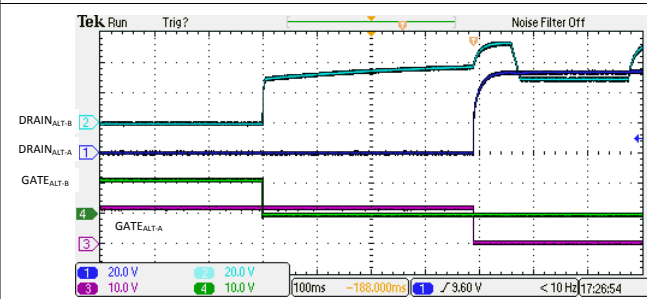


Figure 10-9. 4-Pair Single Signature Class 0-4 Disconnect

10.2.3 Application Curves (continued)

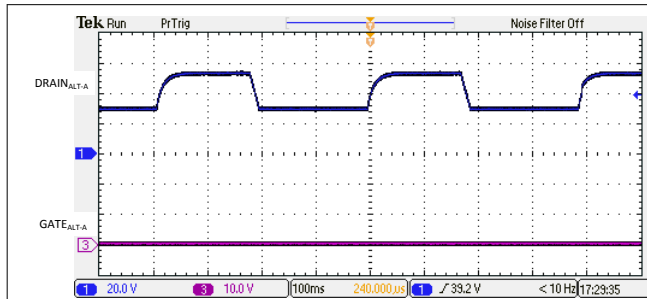


Figure 10-10. 2-Pair Open Circuit Detection Signature

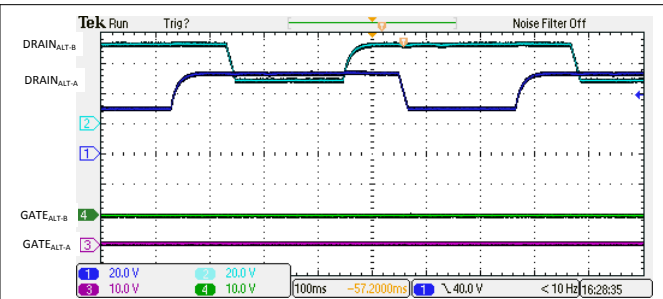


Figure 10-11. 4-Pair Open Circuit Detection Signature

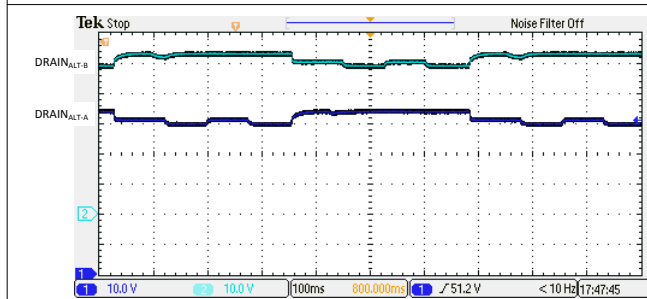


Figure 10-12. 4-Pair Low Resistance (11kΩ) Detection Signature

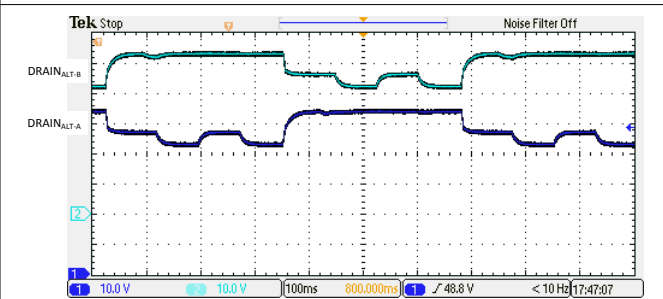


Figure 10-13. 4-Pair High Resistance (36kΩ) Detection Signature

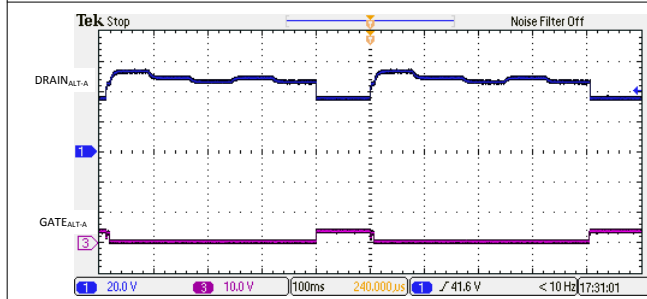


Figure 10-14. 2-Pair Semi-Auto Mode Discovery with a Valid Class 0-3 Load

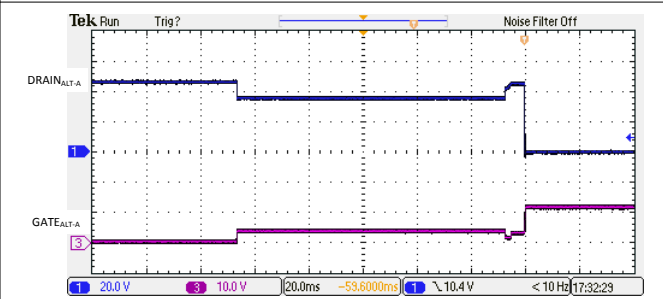


Figure 10-15. 2-Pair 1-Finger Classification and Turn On

10.2.3 Application Curves

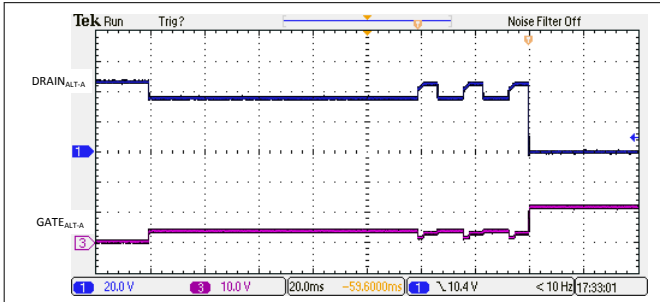


Figure 10-16. 2-Pair 3-Finger Classification and Turn On

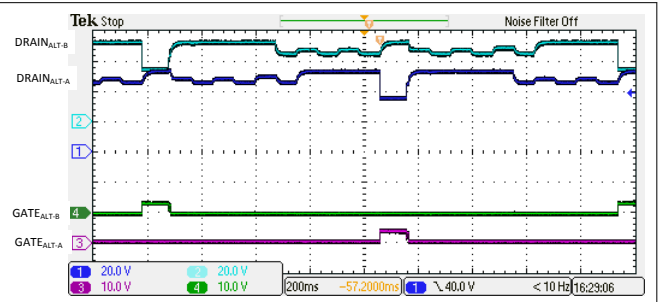


Figure 10-17. 4-Pair Semi-Auto Mode Discovery with a Valid Single Signature Class 0-3 Load

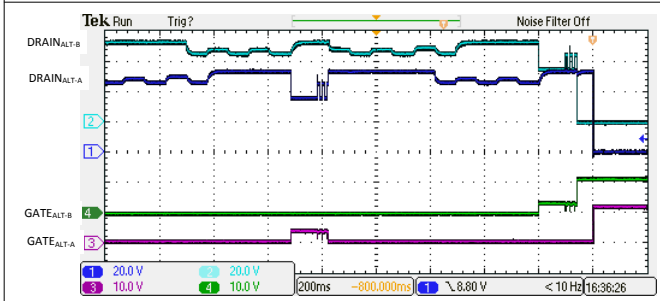


Figure 10-18. 4-Pair Single Signature Discovery and Turn On from Semi-Auto Mode

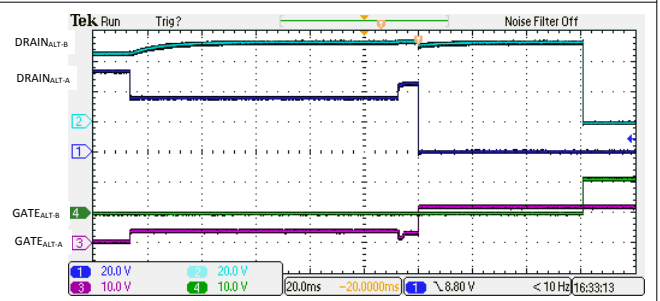


Figure 10-19. 4-Pair Single Signature 1-Finger Classification and Turn On

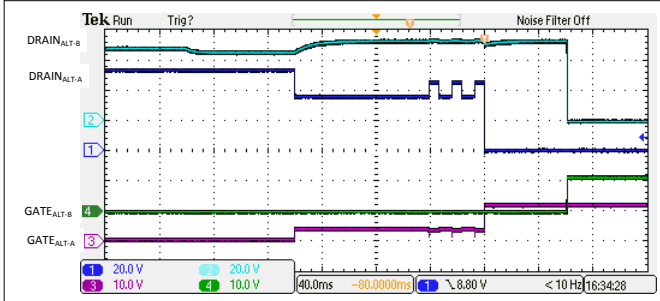


Figure 10-20. 4-Pair Single Signature 3-Finger Classification and Turn On

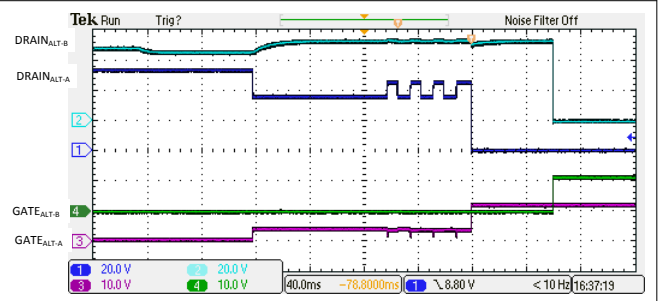


Figure 10-21. 4-Pair Single Signature 4-Finger Classification and Turn On

10.2.3 Application Curves

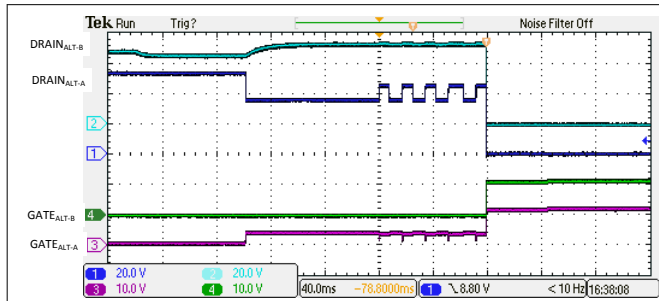


Figure 10-22. 4-Pair Single Signature 5-Finger Classification and Turn On

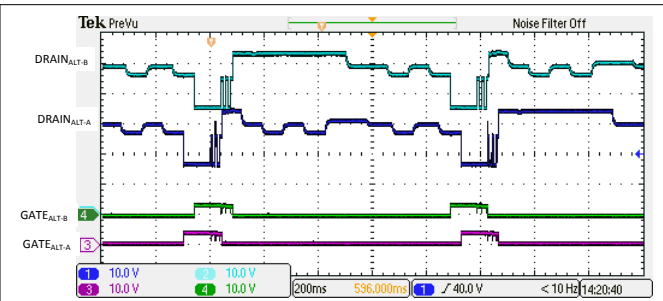


Figure 10-23. 4-Pair Semi-Auto Mode Discovery with a Valid Dual Signature Class 4D Load

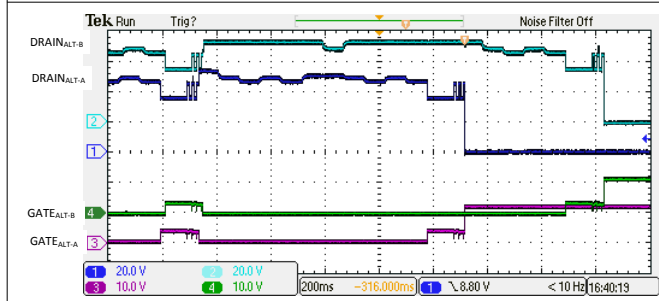


Figure 10-24. 4-Pair Dual Signature Discovery and Turn On from Semi-Auto Mode

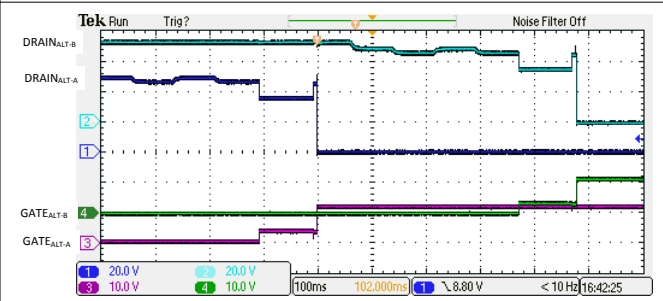


Figure 10-25. 4-Pair Dual Signature 1-Finger Classification and Turn On

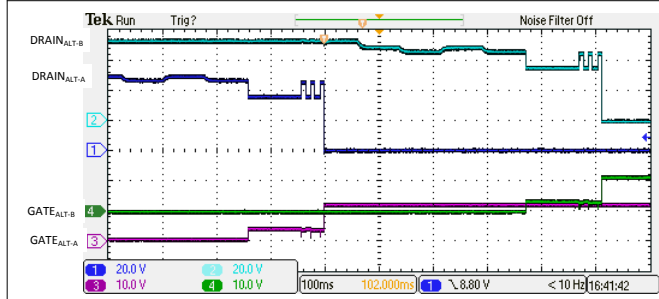


Figure 10-26. 4-Pair Dual Signature 3-Finger Classification and Turn On

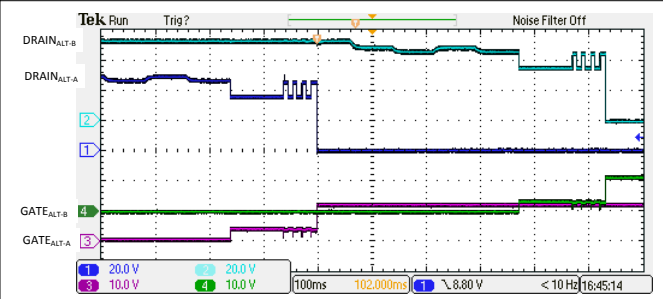


Figure 10-27. 4-Pair Dual Signature 4-Finger Classification and Turn On

11 Power Supply Recommendations

11.1 VDD

The recommended VDD supply voltage requirement is 3.3 V, ± 0.3 V. The TPS23880 requires approximately 6 mA typical and 12 mA maximum from the VDD supply. The VDD supply can be generated from VPWR with a buck-type regulator (A LM5017 based device is recommended) for a higher port count PSE using multiple TPS23880 devices operating in semiauto mode. The power supply design must ensure the VDD rail rises monotonically through the VDD UVLO thresholds without any droop under the UVLO_fall threshold as the loads are turned on. This is accomplished with proper bulk capacitance across the VDD rail for the expected load current steps over worst case design corners. Furthermore, the combination of decoupling capacitance and bulk storage capacitance must hold the VDD rail above the UVLO_fall threshold during any expected transient outages once power is applied.

11.2 VPWR

Although the supported VPWR supply voltage range is 44 V to 57 V, a power supply with a 50 V minimum output is required to provide PoE power levels from 30 W up to 60 W over 2-pair and 4-pair, and a 52 V minimum power supply is required to comply with Type-4 (up to 90W) IEEE requirements. The TPS23880 requires approximately 10-mA typical and 12-mA maximum from the VPWR supply, but the total output current required from the VPWR supply depends on the number and type of ports required in the system. The TPS23880 can be configured to support either 15.5 W, 30 W, 45 W, 60 W, 75W, or 90 W per port and the power limit is set proportionally at turn on. The port power limit, P_{CUT} , is also programmable to provide even greater system design flexibility. However, it is generally recommend to size the VPWR supply accordingly to the PoE Type to be supported. As an example, a 130 W or greater power supply would be recommended for eight type 1 (15.5 W each) ports, or a 500 W or greater power supply is recommended for eight 4-pair type 3 (60 W) ports, assuming maximum port and standby currents.

Note

In IEEE complaint applications, only 4-Pair configured ports are capable of supporting power levels greater than 30 W.

12 Layout

12.1 Layout Guidelines

12.1.1 Kelvin Current Sensing Resistors

Load current in each PSE channel is sensed as the voltage across a low-end current-sense resistor with a value of 255 mΩ. For more accurate current sensing, kelvin sensing of the low end of the current-sense resistor is provided through pins KSENSA for channels 1 and 2, KSENSB for channels 3 and 4, KSENSC for channels 5 and 6 and KSENSD for channels 7 and 8.

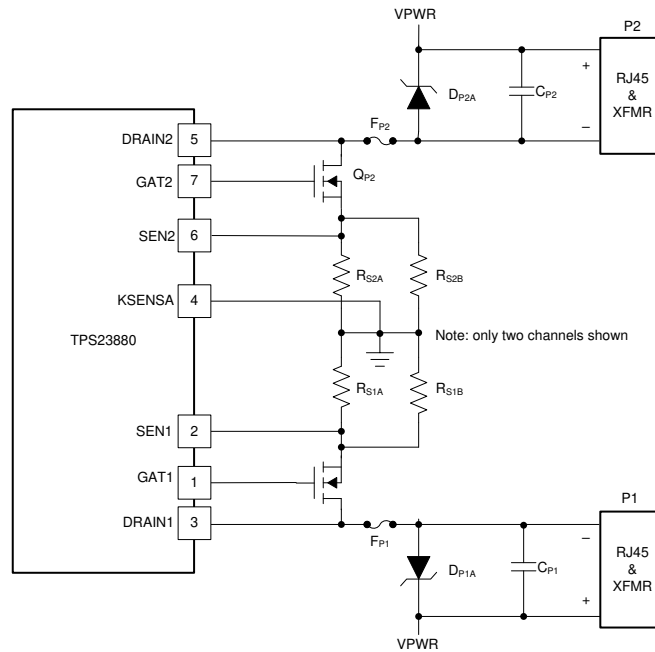


Figure 12-1. Kelvin Current-Sense Connection

KSENSA is shared between SEN1 and SEN2, KSENSB is shared between SEN3 and SEN4, KSENSC is shared between SEN5 and SEN6, and KSENSD is shared between SEN7 and SEN8. To optimize the accuracy of the measurement, the PCB layout must be done carefully to minimize impact of PCB trace resistance. Refer to Figure 12-2 as an example.

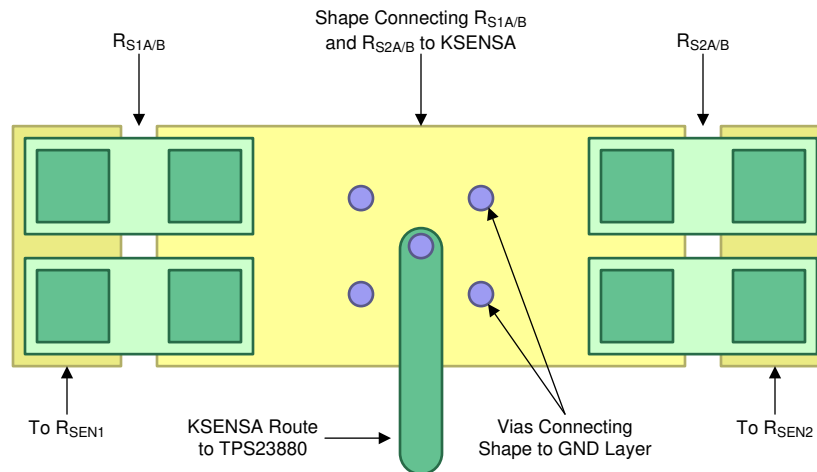


Figure 12-2. Kelvin Sense Layout Example

12.2 Layout Example

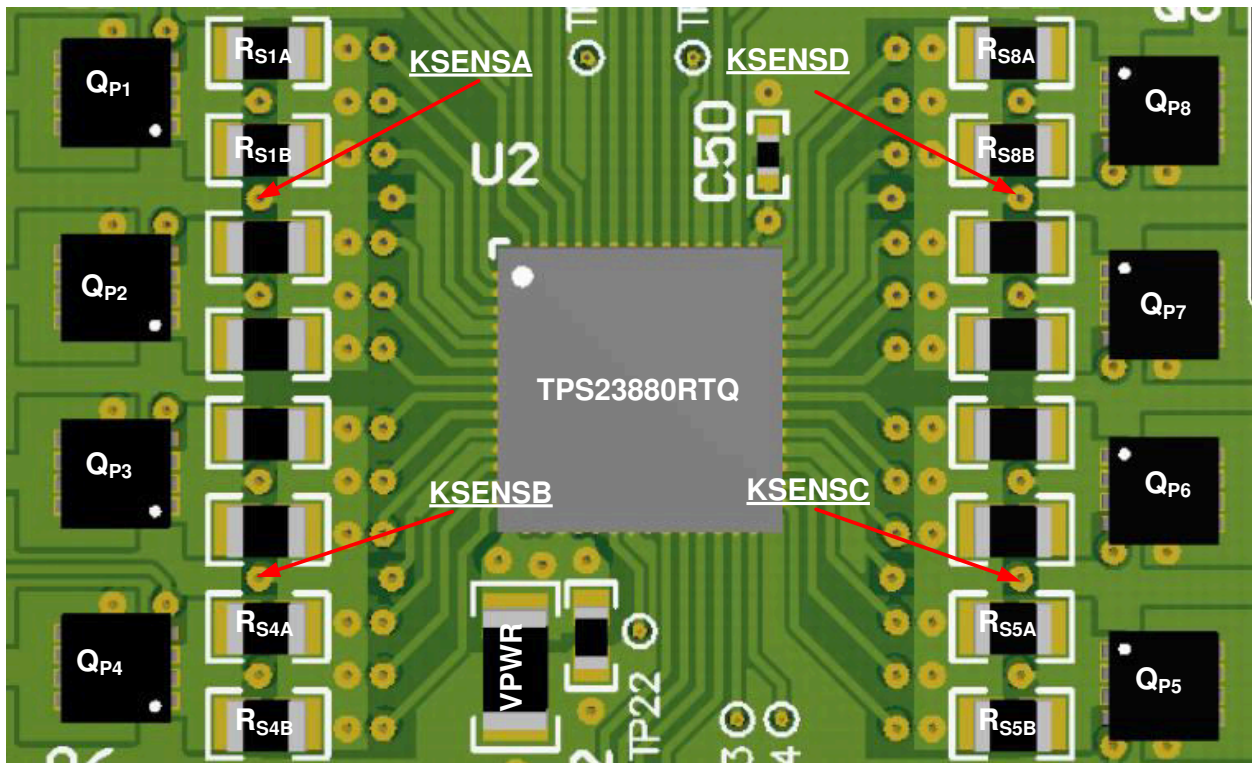


Figure 12-3. Eight Port Layout Example (Top Side)

12.2.1 Component Placement and Routing Guidelines

12.2.1.1 Power Pin Bypass Capacitors

- C_{VPWR} : Place close to pin 17 (VPWR) and connect with low inductance traces and vias according to [Figure 12-3](#).
- C_{VDD} : Place close to pin 43 (VDD) and connect with low inductance traces and vias according to [Figure 12-3](#).

12.2.1.2 Per-Port Components

- R_{SnA} / R_{SnB} : Place according to in a manner that facilitates a clean Kelvin connection with KSENSEA/B/C/D.
- Q_{Pn} : Place Q_{Pn} around the TPS23880 as illustrated in [Figure 12-3](#). Provide sufficient copper from Q_{Pn} drain to F_{Pn} .
- F_{Pn} , C_{Pn} , D_{PnA} , D_{PnB} : Place this circuit group near the RJ45 port connector (or port power interface if a daughter board type of interface is used as illustrated in [Figure 12-3](#)). Connect this circuit group to Q_{Pn} drain or GND (TPS23880- AGND) using low inductance traces.

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [TPS23880EVM: PoE, PSE, TPS23880 Evaluation Module User's Guide](#)
- Texas Instruments, [How to Load TPS2388x SRAM and Parity Code Over I2C Application Report](#)
- [TI mySecure Software](#)

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.4 Trademarks

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13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS23880RTQR | ACTIVE | QFN | RTQ | 56 | 2000 | RoHS & Green | NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | TP23880RTQ | Samples |
| TPS23880RTQT | ACTIVE | QFN | RTQ | 56 | 250 | RoHS & Green | NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | TP23880RTQ | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

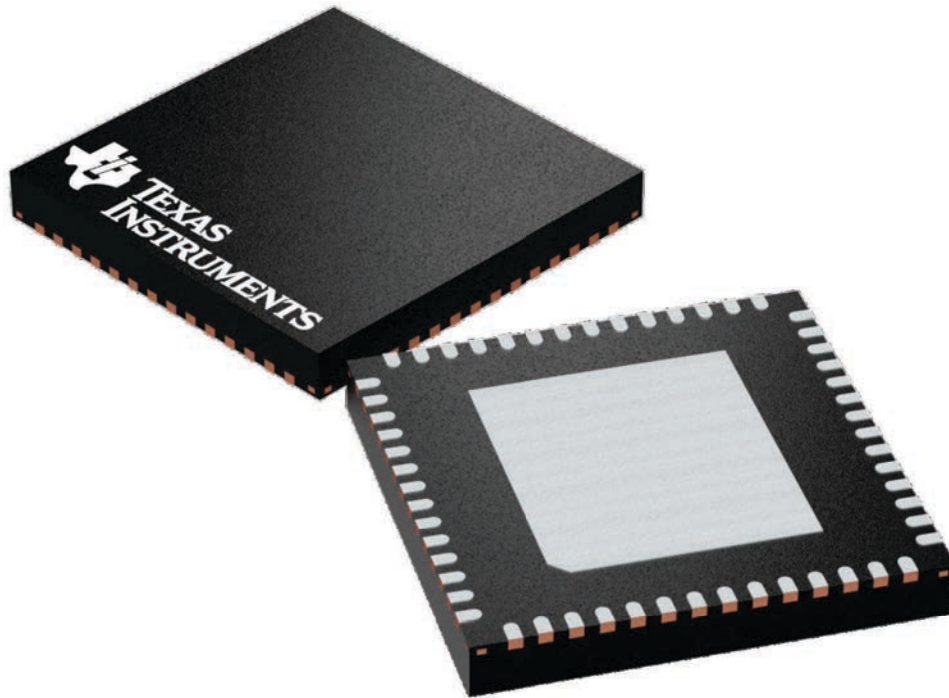
GENERIC PACKAGE VIEW

RTQ 56

VQFN - 1 mm max height

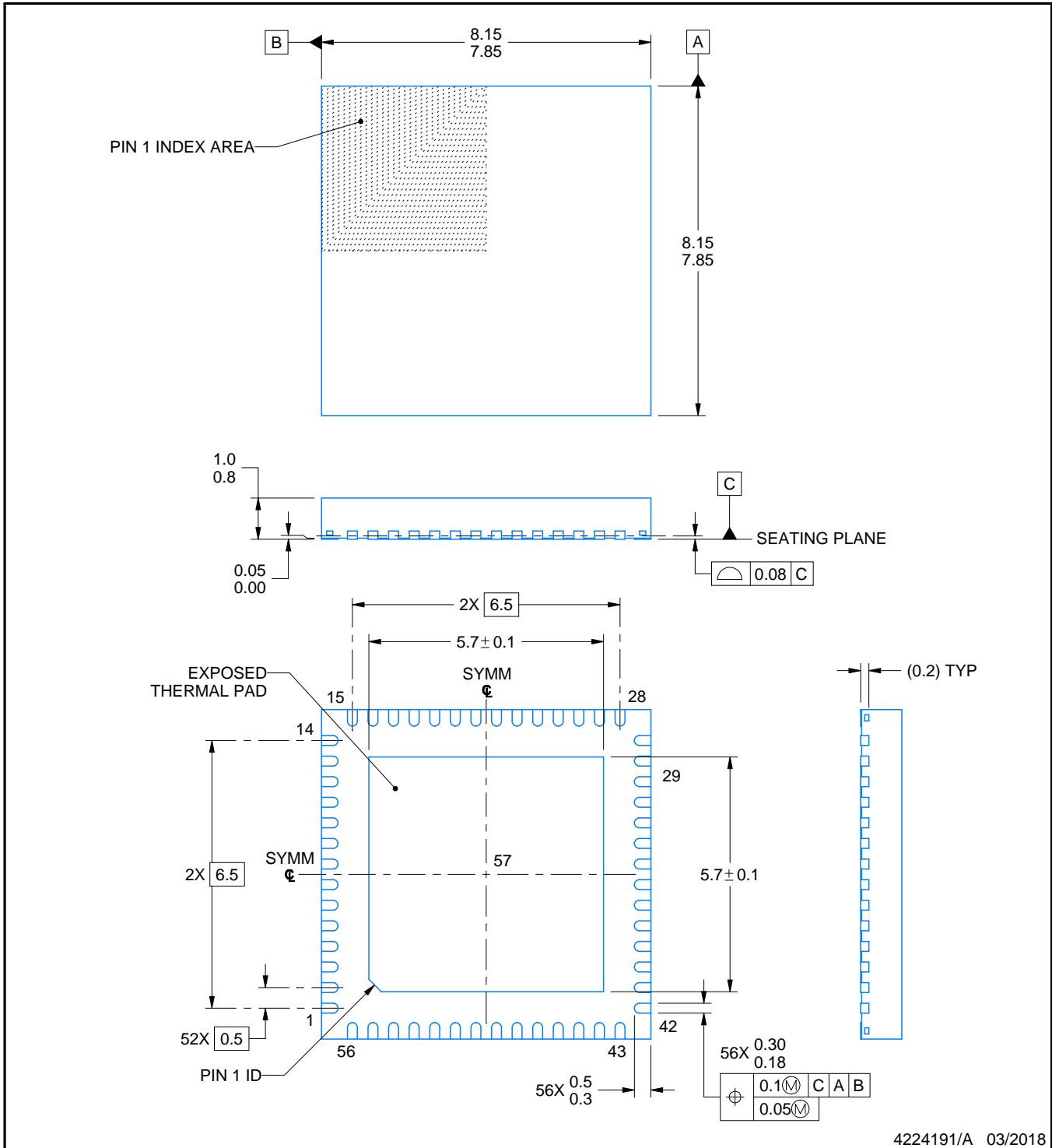
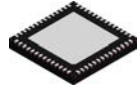
8 x 8, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224653/A



4224191/A 03/2018

NOTES:

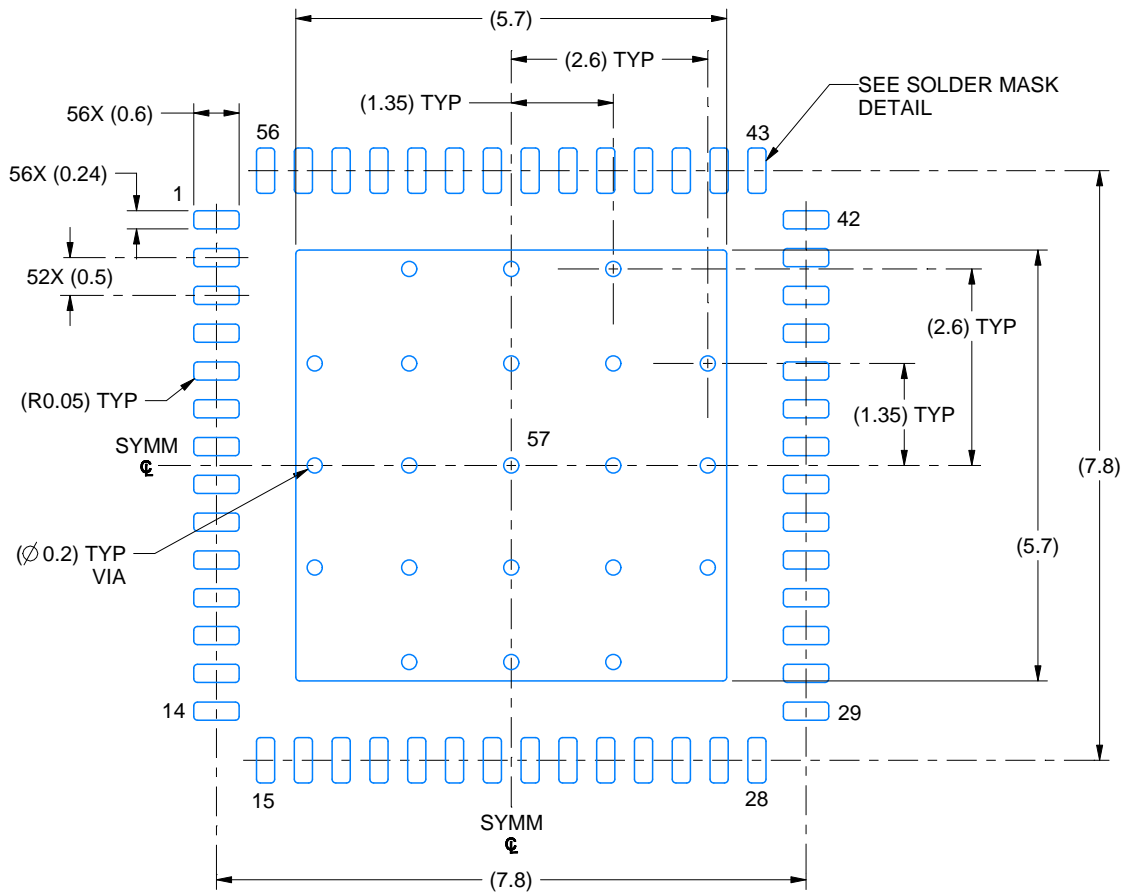
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

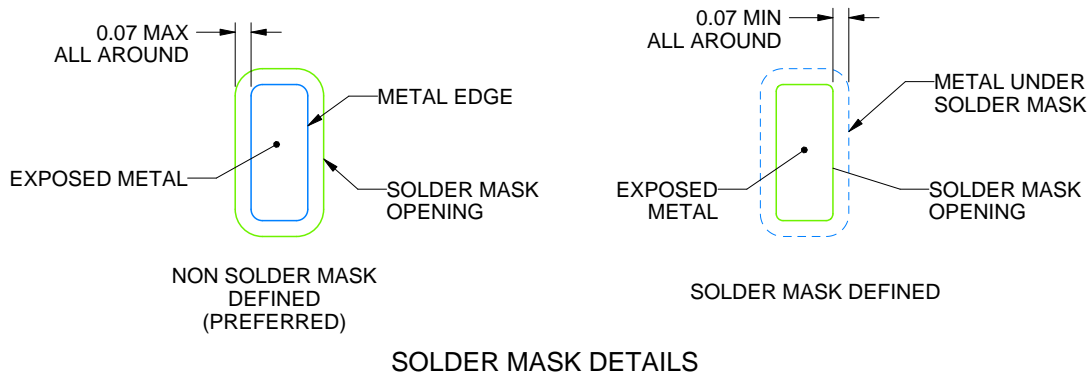
RTQ0056E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4224191/A 03/2018

NOTES: (continued)

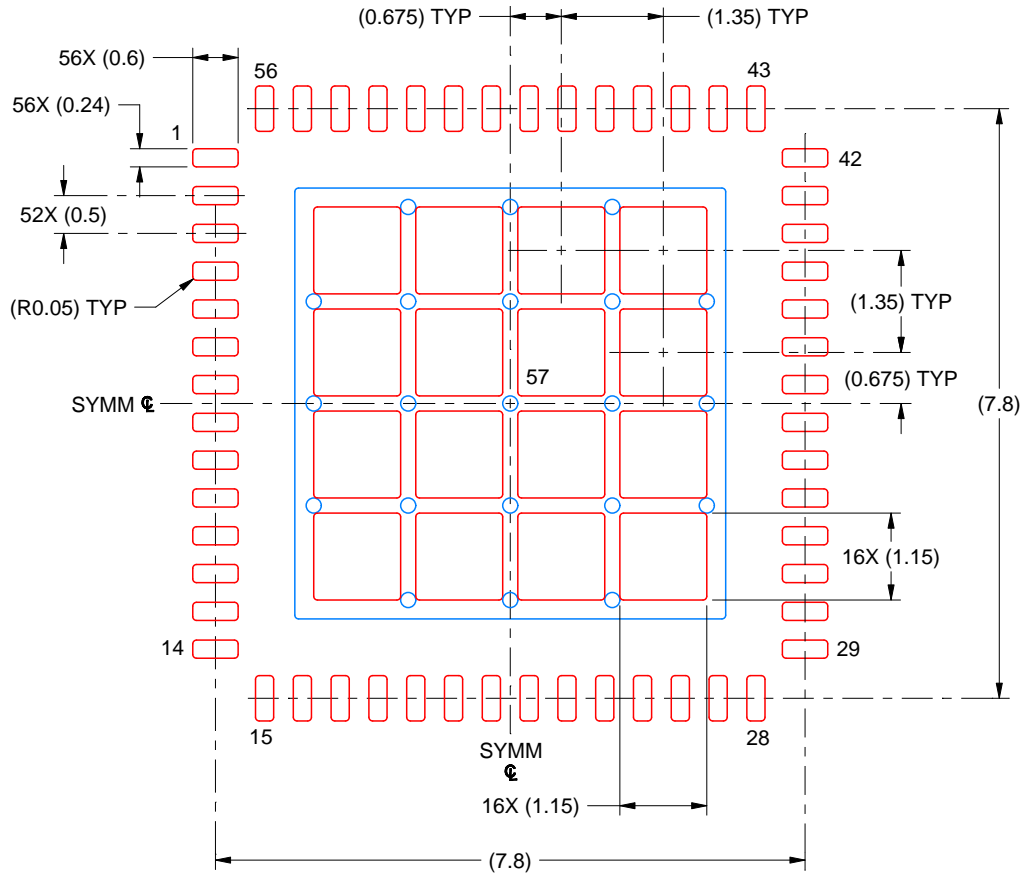
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTQ0056E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 57
65% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224191/A 03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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