ISD ChipCorder®
ISD3800 Series
DataSheet

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1 GENERAL DESCRIPTION

The ISD3800 is a digital ChipCorder® featuring digital compression, comprehensive memory management, and integrated analog/digital audio signal paths. The ISD3800 utilizes serial flash memory to provide non-volatile audio playback for a two-chip solution. The ISD3800 provides an I²S digital audio interface, faster digital programming, higher sampling frequency, and a signal path with SNR 80dB.

The ISD3800 can take digital audio data via I²S or SPI interface. When I²S input is selected, it will replace the analog audio inputs and will support sample rates of 32, 44.1 or 48 kHz depending upon clock configuration. When SPI interface is chosen, the sample rate of the audio data sent must be one of the ISD3800 supported sample rates.

The ISD3800 has inbuilt analog audio inputs, analog audio line driver, and speaker driver output.

The analog audio input, Aux-in, has a fixed gain configured by SPI command. Aux-in can directly feed-through to the analog outputs; it can also mix with the DAC output and then feed-through to the analog outputs.

The ISD3800 can deliver three kinds output: 1) Aux-out, an analog single-ended voltage output; 2) Class-AB BTL (bridge-tied-load) analog differential voltage output; 3) Class-D PWM. Both Class-AB BTL and Class-D PWM output can directly drive a speaker.

2 FEATURES

- External Memory:
  - The ISD3800 supports the following flash:

Manufacturer	Winbond		Numonyx			MXIC
Family	25X	25Q	25P	25PX	25PE	25L / 25V
JEDEC ID	EF 30 1X	EF 40 1X	20 20 1X	20 71 1X	20 80 1X	C2 20 1X

  - The addressing ability of ISD3800 is up to 128Mbit, which is 64-minute playback time based on 8kHz/4bit ADPCM
  - Inbuilt 3V voltage regulator to provide power source to the external flash memory
- Fast Digital Programming
  - Programming rate can go up to 1Mbits/second mainly limited by the flash memory write rate
- Memory Management
  - Store pre-recorded audio (Voice Prompts) using high quality digital compression
  - Use a simple index-based command for playback
  - Execute pre-programmed macro scripts (Voice Macros) designed to control the configuration of the device and play back Voice Prompts sequences
- Sample Rate
  - Seven sampling frequencies are available for a given master sample rate
    For example, the sampling frequencies of 4, 5.3, 6.4, 8, 12.8, 16 and 32kHz are available when the device is clocked at a 32kHz master sample rate
  - For I²S operation, 32, 44.1 and 48kHz master sample rates are available with playback sampling frequencies scaling accordingly
- Compression Algorithm
  - For Pre-Recorded Voice Prompt
    - µ-Law: 6, 7 or 8 bits per sample
    - Differential µ-Law: 6, 7 or 8 bits per sample
    - PCM: 8, 10 or 12 bits per sample
    - Enhanced ADPCM: 2, 3, 4 or 5 bits per sample
    - Variable-bit-rate optimized compression allows best possible compression given a metric of SNR and background noise levels
- Oscillator
  - Internal oscillator with internal reference: 2.048 MHz with ±1% deviation

  - Internal oscillator with external resistor: 2.048 MHz with ±2% deviation (With ±1% precision 80kohm external resistor)
  - External crystal or clock input
    - Crystals support standard audio sampling rates of 2.048, 4.096, 8.192, 12.288 and 11.2896MHz
  - I^2S bit clock input
- Input
  - Aux-in: Analog input with 2-bit gain control configured by SPI command
- Output
  - Aux-out: an analog single-ended voltage output
  - Class-D PWM speaker driver, capable of delivering typical power:
    - 4Ω load: 1W @5.5V; 335mW @3.3V
    - 8Ω load: 930mW @5.5V; 320mW @ 3.3V
  - Class-AB BTL analog differential output, capable of delivering typical power:
    - 4Ω load: 950mW @5.5V; 330mW @3.3V
    - 8Ω load: 930mW @5.5V; 320mW @ 3.3V
- I/O
  - SPI interface: MISO, MOSI, SCLK, SSB for commands and digital audio data
  - I^2S interface: I^2S_CLK, I^2S_WS, I^2S_SDI, I^2S_SDO for digital audio data
  - 8 GPIO pins:
    - 4 GPIO pins share with I^2S
    - 4 GPIO pins share with SPI Interface
    - GPIO pins can trigger Voice Macro for a pushbutton application
- 8-bit Volume Control set by SPI command for flexible mixing
- Talarm temperature threshold: 125°C typical
- Operating Voltage: 2.7 ~ 5.5V
- Standby Current: 1uA typical
- Package:
  - QFN-32 / LQFP-48
  - Package is Halogen-free, RoHS-compliant and TSCA-compliant
- Temperature Options:
  - -40ºC ~ 85ºC

3 BLOCK DIAGRAM

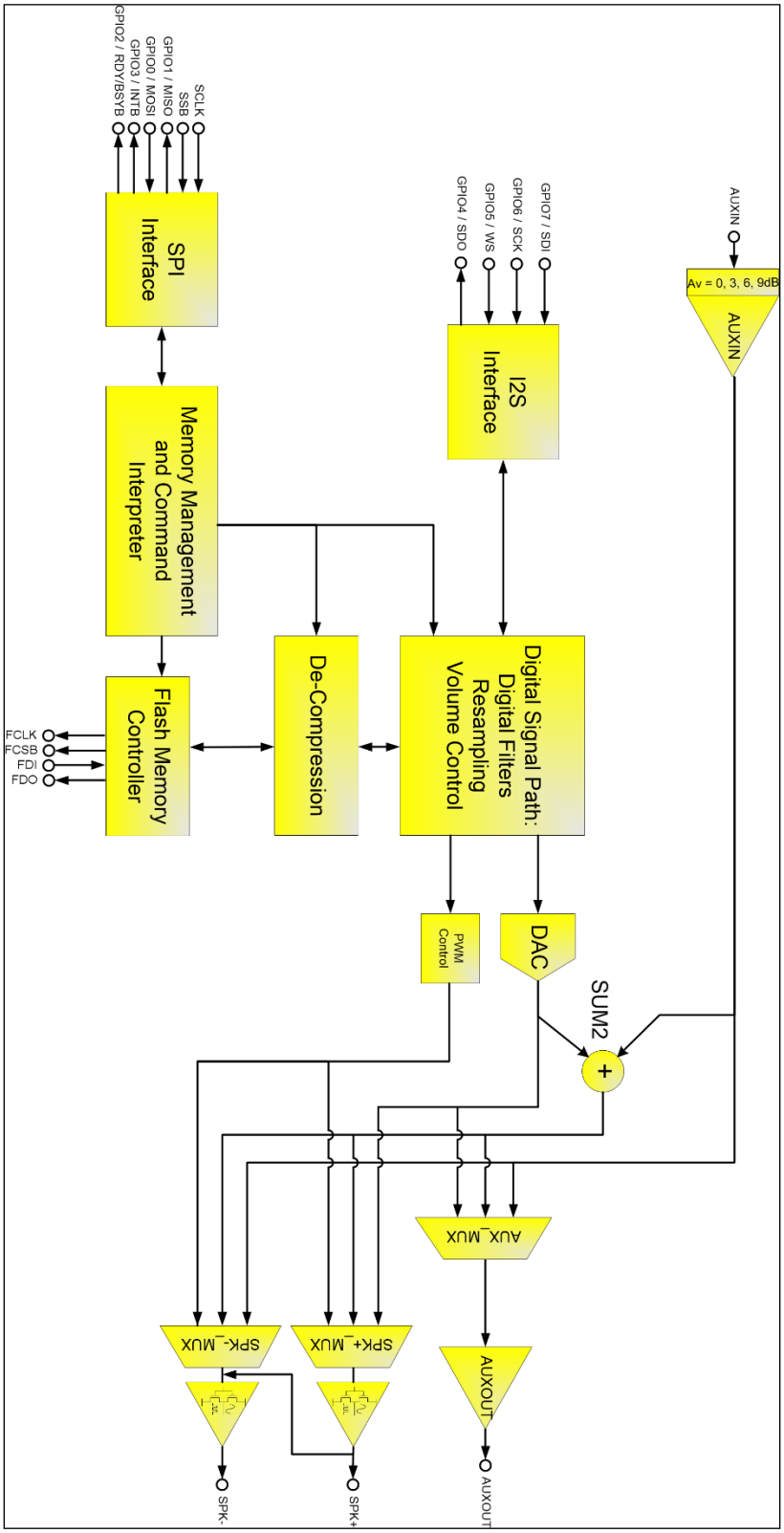


Figure 3-1 ISD3800 Block Diagram

4 PINOUT CONFIGURATION

4.1 48L-LQFP

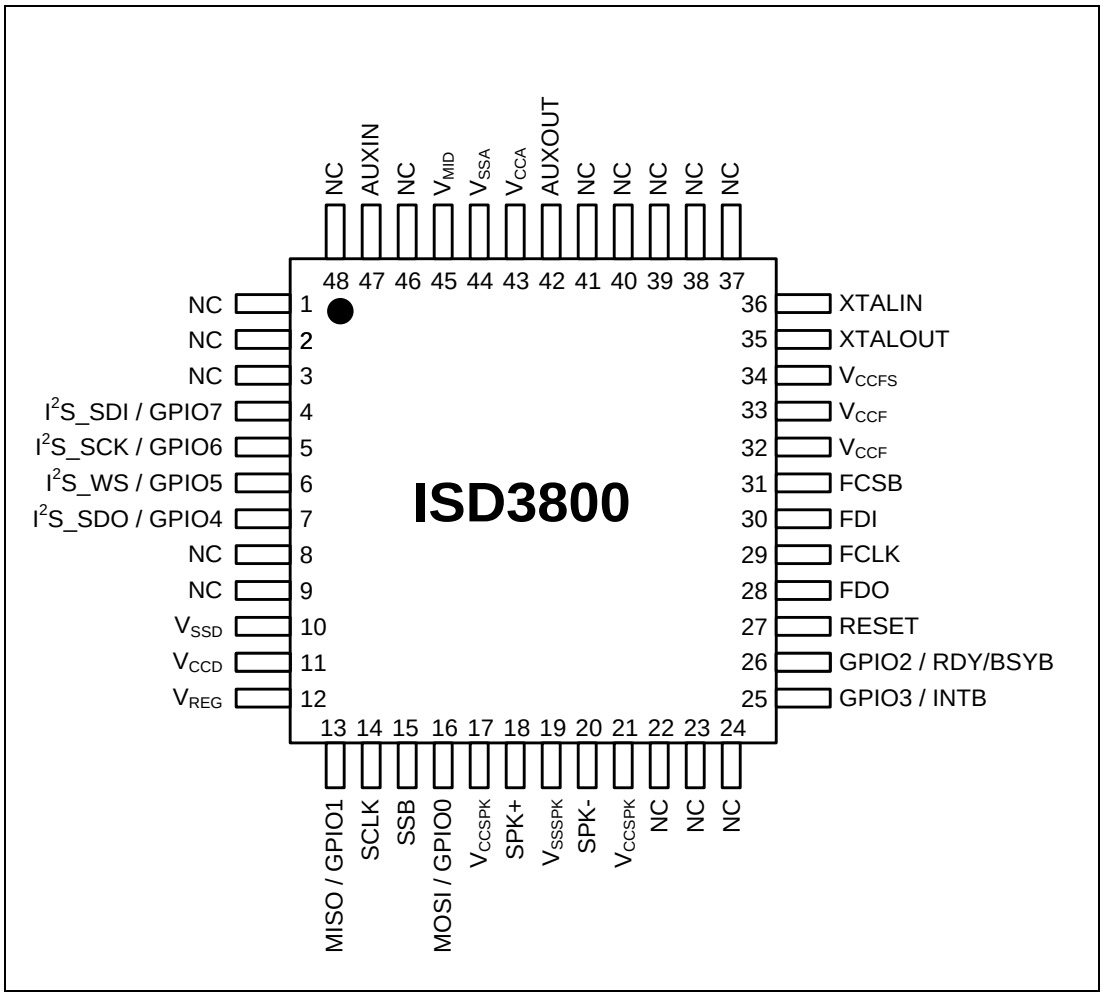


Figure 4-1 ISD3800 48-Lead LQFP Pin Configuration

4.2 32L-QFN

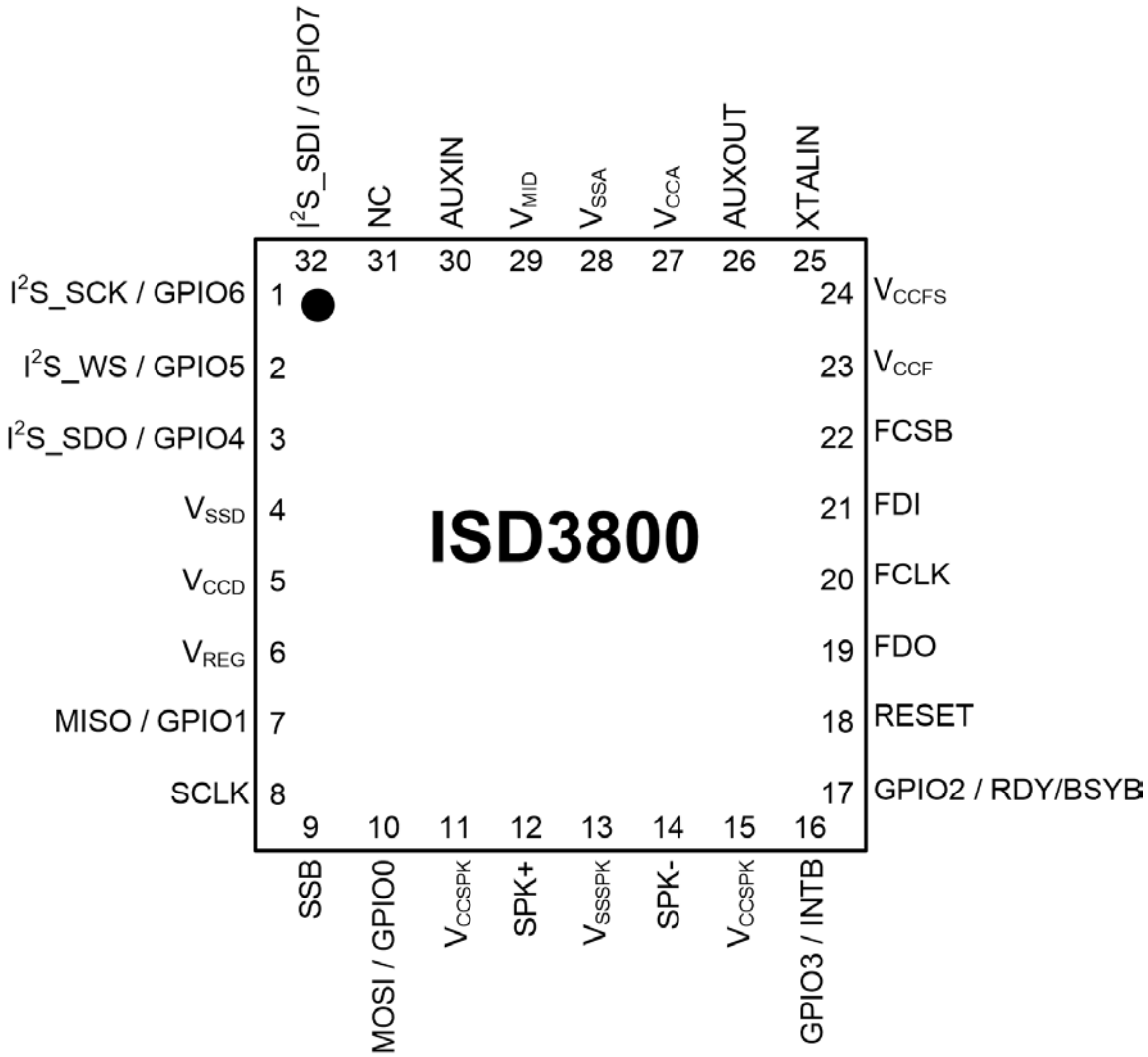


Figure 4-2 ISD3800 32-Lead QFN Pin Configuration

5 PIN DESCRIPTION

Pin #		Pin Name	I/O	Function
LQFP-48	QFN-32			
1		NC		This pin should be left unconnected.
2		NC		This pin should be left unconnected.
3		NC		This pin should be left unconnected.
4	32	GPIO7 / I^2S_SDI	I/O	A GPIO pin. By default this pin is a pull-high input. Can be configured as Serial Data Input of the I^2S interface.
5	1	GPIO6 / I^2S_SCK	I/O	A GPIO pin. By default this pin is a pull-high input. Can be configured as Clock input in slave mode or clock output in master mode. This pin can be configured as an external clock buffer if I^2S is not used.
6	2	GPIO5 / I^2S_WS	I/O	A GPIO pin. By default this pin is a pull-high input. Can be configured as Word Select (WS) input in slave mode or WS output in master mode.
7	3	GPIO4 / I^2S_SDO	I/O	A GPIO pin. By default this pin is a pull-high input. Can be configured as Serial Data Output of the I^2S Interface.
8		NC		This pin should be left unconnected.
9		NC		This pin should be left unconnected.
10	4	V_{SSD}	I	Digital Ground.
11	5	V_{CCD}	I	Digital power supply.
12	6	V_{REG}	O	A 1.8V regulator to supply the internal logic. A minimum 1uF capacitor with low ESR<0.5OHM should be connected to this pin for supply decoupling and stability.
13	7	MISO / GPIO1	O	Master-In-Slave-Out. Serial output from the ISD3800 to the host. This pin is in tri-state when SSB=1. Can be configured as GPIO1.
14	8	SCLK	I	Serial Clock input to the ISD3800 from the host.
15	9	SSB	I	Slave Select input to the ISD3800 from the host. When SSB is low device is selected and responds to commands on the SPI interface.
16	10	MOSI / GPIO0	I	Master-Out-Slave-In. Serial input to the ISD3800 from the host. Can be configured as GPIO0.
17	11	V_{CCSPK}	I	Power supply for speaker driver.
18	12	SPK+	O	PWM driver positive output. This SPK+ output, together with SPK- pin, provide a differential output to drive a speaker. During power down this pin is in tri-state. Or, can be configured as Class-AB BTL which, together with SPK- pin, provides a differential voltage output. Or, can be configured as a Class-AB single-ended output.
19	13	V_{SSSPK}	I	In PWM mode: Digital Ground for the PWM Driver. Or,

Pin #		Pin Name	I/O	Function
LQFP-48	QFN-32			
				In Class-AB mode: Analog Ground for the Class-AB output.
20	14	SPK-	O	PWM driver negative output. This SPK- output, together with SPK+ pin, provides a differential output to drive a speaker. During power down this pin is tri-state. Or, can be configured as Class-AB BTL which, together with SPK+ pin, provides a differential voltage output. Or, can be configured as a Class-AB single-ended output.
21	15	V_{CCSPK}	I	Power supply for speaker driver.
22		NC		This pin should be left unconnected.
23		NC		This pin should be left unconnected.
24		NC		This pin should be left unconnected.
25	16	INTB / GPIO3	O	Active low interrupt request pin. This pin is an open-drain output. Can be configured as GPIO3.
26	17	RDY/ BSYB / GPIO2	O	An output pin to report the status of data transfer on the SPI interface. “High” indicates that ISD3800 is ready to accept new SPI commands or data. Can be configured as GPIO2.
27	18	RESET	I	Applying power to this pin will reset the chip. (A high pulse of 50ms or more will reset the chip.)
28	29	FDO	O	Serial data output of the external serial flash interface. Connects to data input (DI) of external serial flash.
29	20	FCLK	O	Serial data CLK of the external serial flash interface.
30	21	FDI	I	Serial data input to external serial flash interface. Connects to data output (DO) of external flash memory.
31	22	FCSB	O	Chip Select Bar of the external serial flash interface.
32	23	V_{CCF}	O	Digital power supply for the external flash memory. A minimum 1uF capacitor with low ESR<0.5OHM should be connected to this pin for supply decoupling and stability. Refer to the application diagram.
33		V_{CCF}	O	Digital power supply for the external flash memory. A minimum 1uF capacitor with low ESR<0.5OHM should be connected to this pin for supply decoupling and stability. Refer to the application diagram.
34	24	V_{CCFS}	I	Digital power supply for the inbuilt voltage regulator for the external flash memory. A 0.1uF capacitor should be connected to this pin for supply decoupling and stability. Refer to the application diagram.
35		XTALOUT	O	Crystal interface output pin.
36	25	XTALIN	I	The CLK_CFG register determines one of the following three configurations: (1) A crystal or resonator connected between the XTALOUT and XTALIN pins. (2) A resistor connected to GND as a reference current to the internal oscillator and left the XTALOUT unconnected. (3) An external clock input to the device and left the XTALOUT unconnected.

Pin #		Pin Name	I/O	Function
LQFP-48	QFN-32			
37		NC		This pin should be left unconnected.
38		NC		This pin should be left unconnected.
39		NC		This pin should be left unconnected.
40		NC		This pin should be left unconnected.
41		NC		This pin should be left unconnected.
42	26	Aux-out	O	Aux Out. This pin is an analog voltage output. If AUXOUT is not used, this pin should be left unconnected.
43	27	V_{CCA}	I	Analog power supply pin.
44	28	V_{SSA}	I	Analog ground pin.
45	29	V_{MID}	O	Middle voltage reference for the swing of analog/digital audio outputs. A 4.7uF capacitor should be connected to this pin for supply decoupling and stability.
46		NC		This pin should be left unconnected.
47	30	Aux-in	I	Auxiliary input with the gain set by SPI command If Aux-in is not used, this pin should be left unconnected.
48	31	NC		This pin should be left unconnected.

6 ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS

DESCRIPTION	SYMBOL	CONDITION	MIN	MAX	UNITS
DC Power Supply	V_{CCD}	$V_{CCD} – V_{SSD}$	-0.3	+6.0	V
	V_{CCA}	$V_{CCA} – V_{SSA}$	-0.3	+6.0	V
	V_{CCSPK}	$V_{CCSPK} – V_{SSSPK}$	-0.3	+6.0	V
Digital Input Voltage	DV_{IN}	DV_{IN} - V_{SSD}	$V_{SSD} – 0.3$	$V_{CCD} + 0.3$	V
Analog Input Voltage	AV_{IN}	AV_{IN} - V_{SSA}	$V_{SSA} – 0.3$	$V_{CCA} + 0.3$	V
Junction Temperature	T_J	-	-40	+125	°C
Storage Temperature	T_{st}	-	-65	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended period of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty. These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

6.2 OPERATING CONDITIONS

CONDITIONS	VALUES
Operating temperature range (Case temperature)	-40°C to +85°C
Digital Supply voltage (V_{CCD}) [1]	+2.7V to +5.5V
Digital Ground voltage (V_{SSD}) [2]	0V
Analog Supply voltage (V_{CCA}) [3]	+2.7V to +5.5V
Analog Ground voltage (V_{SSA}) [2]	0V
Speaker Supply voltage (V_{CCSPK}) [3]	+2.7V to +5.5V
Speaker Ground voltage (V_{SSSPK}) [2]	0V
Flash Source Supply voltage (V_{CCFS}) [4] – to regulate V_{CCF}	+2.7V to +5.5V
Flash Source Supply voltage (V_{CCFS}) [4] – tied to V_{CCF}	+2.25V to +3.6V
Flash Supply voltage - (V_{CCF}) [4] – regulated from V_{CCFS}	+2.4V to +3.0V
Flash Supply voltage - (V_{CCF}) [4] – tied to V_{CCFS}	+2.25V to +3.6V

NOTES:

[1] V_{CCD} 2.7 ~ 5.5V; No restrictions with respect to V_{CCA} and V_{CCSPK}.

[2] $V_{SSD} = V_{SSA} = V_{SSSPK}$

[3] In Class-AB mode: V_{CCSPK} must equal V_{CCA}. Otherwise: $V_{CCSPK} \geq V_{CCA}$.

[4] If V_{CCFS} is guaranteed to be below 3.6V (or upper flash supply limit), then V_{CCF} should be tied to V_{CCFS}.

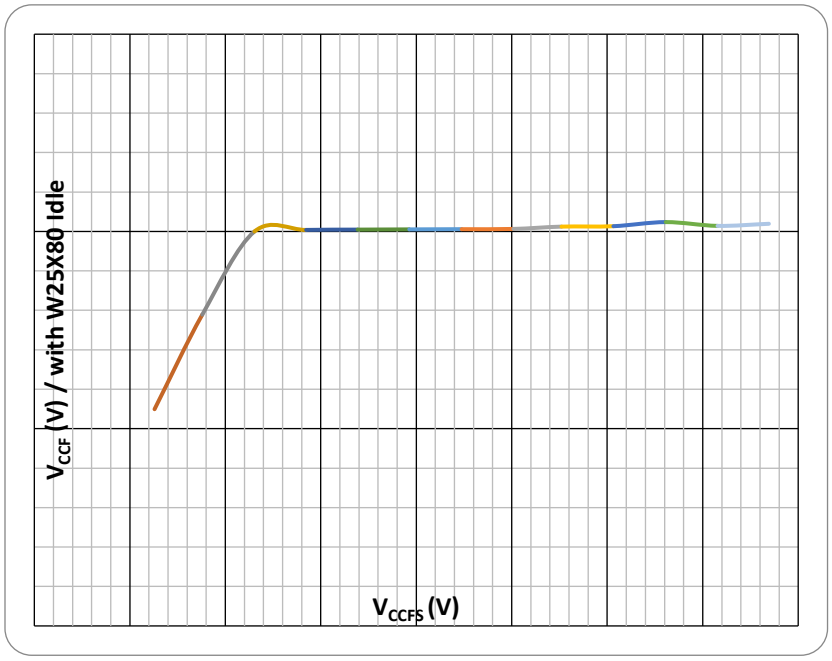


Figure 6-1 V_{CCF} vs. V_{CCFS} – V_{CCF} is regulated internally from V_{CCFS}[4]

6.3 DC PARAMETERS

PARAMETER	SYMBOL	MIN	TYP. [1]	MAX	UNITS	CONDITIONS
Digital Supply Voltage	V_{CCD}	2.7		5.5	V	
Analog Supply Voltage	V_{CCA}	2.7		5.5	V	
Speaker Supply Voltage	V_{CCSPK}	2.7		5.5	V	
Flash Source Supply Voltage	V_{CCFS}	2.7		5.5	V	to regulate V_{CCF}
		2.25		3.6		tied to V_{CCF}
Flash Supply Voltage (refer to Figure 6-1)	V_{CCF}		V_{CCFS}-0.3		V	regulated from V_{CCFS} V_{CCFS} = 2.7 ~ 3.3V
			3.0			regulated from V_{CCFS} V_{CCFS} = 3.3 ~ 5.5V
		2.25		3.6		tied to V_{CCFS}
Input Low Voltage	V_{IL}	V_{SSD}-0.3		0.3xV_{CCD}	V	
Input High Voltage	V_{IH}	0.7xV_{CCD}		V_{CCD}	V	
Output Low Voltage	V_{OL}	V_{SSD}-0.3		0.3xV_{CCD}	V	I_{OL} = 1mA
Output High Voltage	V_{OH}	0.7xV_{CCD}		V_{CCD}	V	I_{OH} = -1mA
INTB Output Low Voltage	V_{OH1}			0.4	V	
Playback Current	$I_{DD\_Playback}$			30	mA	No load
Standby Current	I_{SB}		1	10	µA	V_{CCD} = 3.0v
Input Leakage Current	I_{IL}	-1		+1	µA	Force V_{CCD}

Notes: [1] Conditions V_{CCD}=V_{CCA}=V_{CCSPK}=V_{CCFS}=3V, T_A=25°C unless otherwise stated

6.4 AC PARAMETER

6.4.1 Internal Oscillator

Parameter	Symbol	Min	Typ.	Max	Unit	CONDITION
Internal oscillator with internal reference	FINT	-1%	2.048 MHz	+1%	MHz	V_{CCD} = 3.3V. At room temperature.
Internal oscillator with external reference	FEXT	-2%	2.048 MHz	+2%	MHz	With ±1% precision resistor, 80kohm. V_{CCD} = 3.3V. At room temperature.

6.4.2 Input

AUX-IN:

Conditions: VCCD = 3.3V, VCCA = VCCSPK, MCLK = 16.384MHz, TA = +25°C, 1kHz signal

Parameter	Symbol	Min	Typ.	Max	Unit	CONDITION
Auxiliary Analog Inputs (AUXIN)						
Full scale input signal[1]		Gain = 0dB		1.0 0		Vrms dBV
AUX Programmable gain			0		9	dB
AUX programmable gain step size		Guaranteed Monotonic		3		dB
Input resistance	Raux_in	Aux direct-to-out path, only Input gain = +9.0dB Input gain = +6.0dB Input gain = +3.0dB Input gain = 0dB		 21 27 33 40		 kΩ kΩ kΩ kΩ
Aux-in Gain Accuracy	$A_{AUX(GA)}$		-0.5dB		+0.5dB	dB

Note: VCCA = VCCSPK=3.3V or VCCA = VCCSPK=5.0V

6.4.3 Output

AUX-OUT

Conditions: V_{CCD} = 3.3V, V_{CCA} = V_{CCSPK} = 5V, 16KHz Sample rate, PCM12, T_A = +25°C, 1kHz signal

Parameter	Symbol	Comment/Condition	Min	Typ.	Max	Unit
Digital to Analog Converter (DAC) driving AUXOUT with 5kΩ / 100pF load						
Full-scale output [1]		Gain paths all at 0dB gain		V_{CCA} / 3.3		V_{rms}
Signal-to-noise ratio	SNR	A-weighted		85		dB
Total harmonic distortion [2]	THD+N	R_L = 5kΩ; full-scale signal A-weighted		-80		dB

Conditions: V_{CCD} = 3.3V, V_{CCA} = V_{CCSPK} = 3.3V, 16KHz Sample rate, PCM12, T_A = +25°C, 1kHz signal

Parameter	Symbol	Comment/Condition	Min	Typ.	Max	Unit
Digital to Analog Converter (DAC) driving AUXOUT with 5kΩ / 100pF load						
Full-scale output [1]		Gain paths all at 0dB gain		V_{CCA} / 3.3		V_{rms}
Signal-to-noise ratio	SNR	A-weighted		80		dB
Total harmonic distortion [2]	THD+N	R_L = 5kΩ; full-scale signal A-weighted		-77		dB

PWM OUTPUT

Conditions: V_{CCD} = 3.3V, V_{CCA} = V_{CCSPK} = 5V, 16KHz Sample rate, PCM12, T_A = +25°C, 1kHz signal, 8Ω load

Parameter	Symbol	Comment/Condition	Min	Typ.	Max	Unit
Signal-to-noise ratio[3]	SNR	A-weighted + Class D Filter		65		dB
Total harmonic distortion [2]	THD	A-weighted + Class D Filter		-40		dB
Efficiency	E_{PWM}	8Ω bridge-tied-load		85		%

Conditions: V_{CCD} = 3.3V, V_{CCA} = V_{CCSPK} = 3.3V, 16KHz Sample rate, PCM12, T_A = +25°C, 1kHz signal, 8Ω load

Parameter	Symbol	Comment/Condition	Min	Typ.	Max	Unit
Signal-to-noise ratio[3]	SNR	A-weighted + Class D Filter		65		dB
Total harmonic distortion [2]	THD	A-weighted + Class D Filter		-40		dB
Efficiency	E_{PWM}	8Ω bridge-tied-load		80		%

CLASS-AB BTL OUTPUT

Conditions: V_{CCD} = 3.3V, V_{CCA} = V_{CCSPK} = 5V, 16KHz Sample rate, PCM12, T_A = +25°C, 1kHz signal, 8Ω load

Parameter	Symbol	Comment/Condition	Min	Typ.	Max	Unit
Full scale output [1]		Gain paths all at 0dB gain		V_{CCA} / 3.3		V_{rms}
Signal-to-noise ratio	SNR	A-weighted		90		dB
Total harmonic distortion [2]	THD	A-weighted		-60		dB
Efficiency	E_{AB}	8Ω bridge-tied-load		50		%

Conditions: V_{CCD} = 3.3V, V_{CCA} = V_{CCSPK} = 3.3V, 16KHz Sample rate, PCM12, T_A = +25°C, 1kHz signal, 8Ω load

Parameter	Symbol	Comment/Condition	Min	Typ.	Max	Unit
Full scale output [1]		Gain paths all at 0dB gain		V_{CCA} / 3.3		V_{rms}
Signal-to-noise ratio	SNR	A-weighted		84		dB
Total harmonic distortion [2]	THD	A-weighted		-60		dB
Efficiency	E_{AB}	8Ω bridge-tied-load		50		%

Notes

1. Full Scale is relative to the magnitude of VCCA and can be calculated as FS = VCCA/3.3.
2. Distortion is measured in the standard way as the combined quantity of distortion products plus noise. The signal level for distortion measurements is at 3dB below full scale, unless otherwise noted.
3. SNR measured with a -100dbFS signal at input.

SPEAKER OUTPUT POWER

Conditions: V_{CCD} = 3.3V, 16KHz sample rate, 12bit PCM, T_A = +25°C, 1kHz signal

Parameter	Symbol	mode	Min	Typ	Max	Unit	Comment/Condition[1]
Output Power	P_{OUT_SPK}	Class-D PWM		260		mW	@ 3.3V, Load 8Ω, 1% THD
				640		mW	@ 5.0V, Load 8Ω, 1% THD
				770		mW	@ 5.5V, Load 8Ω, 1% THD
				335		mW	@ 3.3V, Load 4Ω, 10% THD
				840		mW	@ 5.0V, Load 4Ω, 10% THD
				1.00		W	@ 5.5V, Load 4Ω, 10% THD
		Class-AB BTL		255		mW	@ 3.3V, Load 8Ω, 0.3% THD
				610		mW	@ 5.0V, Load 8Ω, 0.3% THD
				750		mW	@ 5.5V, Load 8Ω, 0.3% THD
				330		mW	@ 3.3V, Load 4Ω, 10% THD
				800		mW	@ 5.0V, Load 4Ω, 10% THD
				950		mW	@ 5.5V, Load 4Ω, 10% THD

Note:

1. VCCA=VCCSPK.

6.4.4 SPI Timing

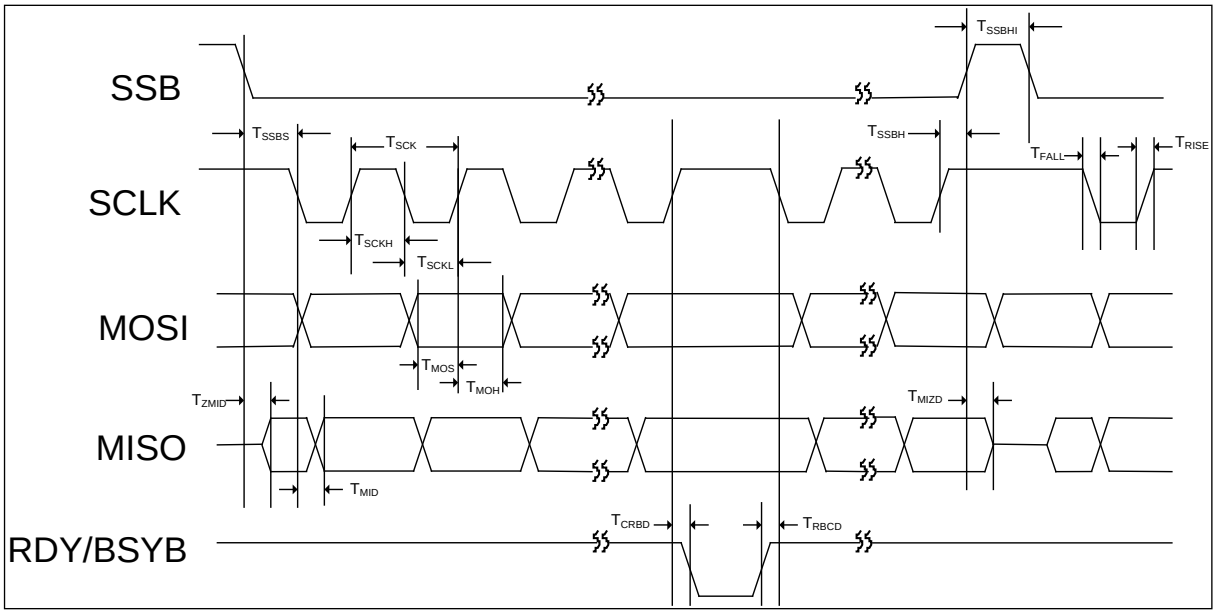


Figure 6-2 SPI Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{SCK}	SCLK Cycle Time	60	---	---	ns
T_{SCKH}	SCLK High Pulse Width	25	---	---	ns
T_{SCKL}	SCLK Low Pulse Width	25	---	---	ns
T_{RISE}	Rise Time for All Digital Signals	---	---	10	ns
T_{FALL}	Fall Time for All Digital Signals	---	---	10	ns
T_{SSBS}	SSB Falling Edge to 1st SCLK Falling Edge Setup Time	30	---	---	ns
T_{SSBH}	Last SCLK Rising Edge to SSB Rising Edge Hold Time	30ns	---	50us	---
T_{SSBHI}	SSB High Time between SSB Lows	20	---	---	ns
T_{MOS}	MOSI to SCLK Rising Edge Setup Time	15	---	---	ns
T_{MOH}	SCLK Rising Edge to MOSI Hold Time	15	---	---	ns
T_{ZMID}	Delay Time from SSB Falling Edge to MISO Active	--	--	12	ns
T_{MIZD}	Delay Time from SSB Rising Edge to MISO Tri-state	--	--	12	ns
T_{MID}	Delay Time from SCLK Falling Edge to MISO	---	---	12	ns
T_{CRBD}	Delay Time from SCLK Rising Edge to RDY/BSYB Falling Edge	--	--	12	ns
T_{RBCD}	Delay Time from RDY/BSYB Rising Edge to SCLK Falling Edge	0	--	--	ns

6.4.5 I²S Timing

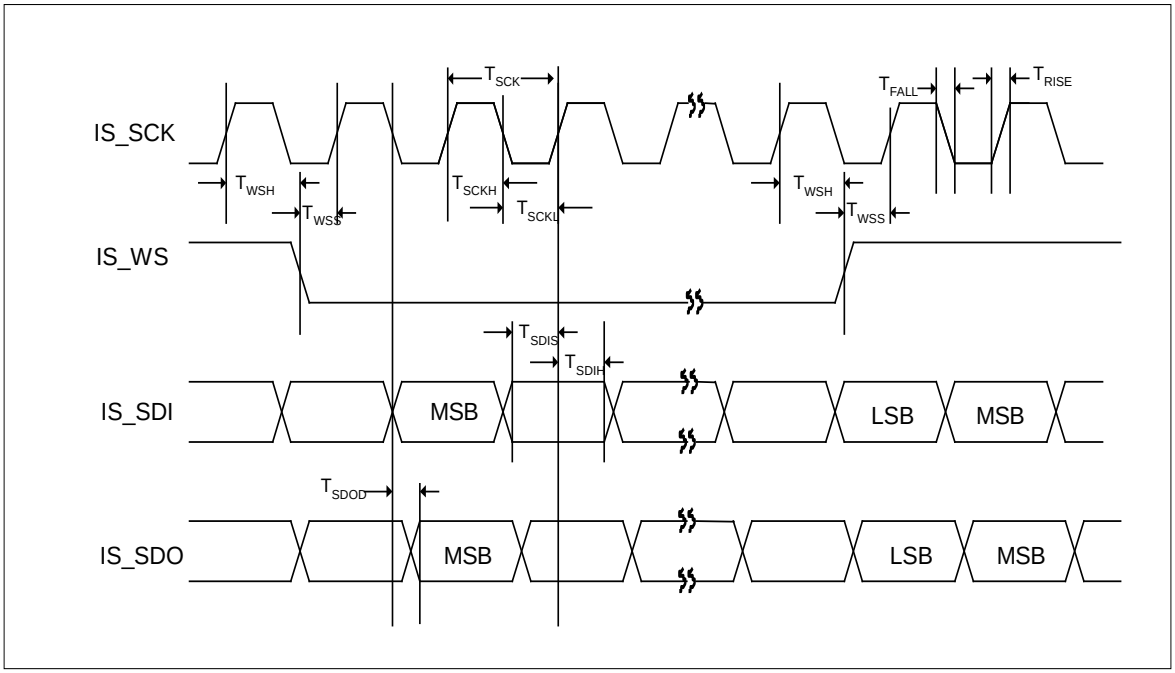


Figure 6-3 I²S Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{SCK}	IS_SCK Cycle Time	60	---	---	ns
T_{SCKH}	IS_SCK High Pulse Width	25	---	---	ns
T_{SCKL}	IS_SCK Low Pulse Width	25	---	---	ns
T_{RISE}	Rise Time for All Digital Signals	---	---	10	ns
T_{FALL}	Fall Time for All Digital Signals	---	---	10	ns
T_{WSS}	WS to IS_SCK Rising Edge Setup Time	20	---	---	ns
T_{WSH}	IS_SCK Rising Edge to IS_WS Hold Time	20	---	---	ns
T_{SDIS}	IS_SDI to IS_SCK Rising Edge Setup Time	15	---	---	ns
T_{SDIH}	IS_SCK Rising Edge to IS_SDI Hold Time	15	---	---	ns
T_{SDOD}	Delay Time from IS_SCLK Falling Edge to IS_SDO	---	---	12	ns

7 APPLICATION DIAGRAM

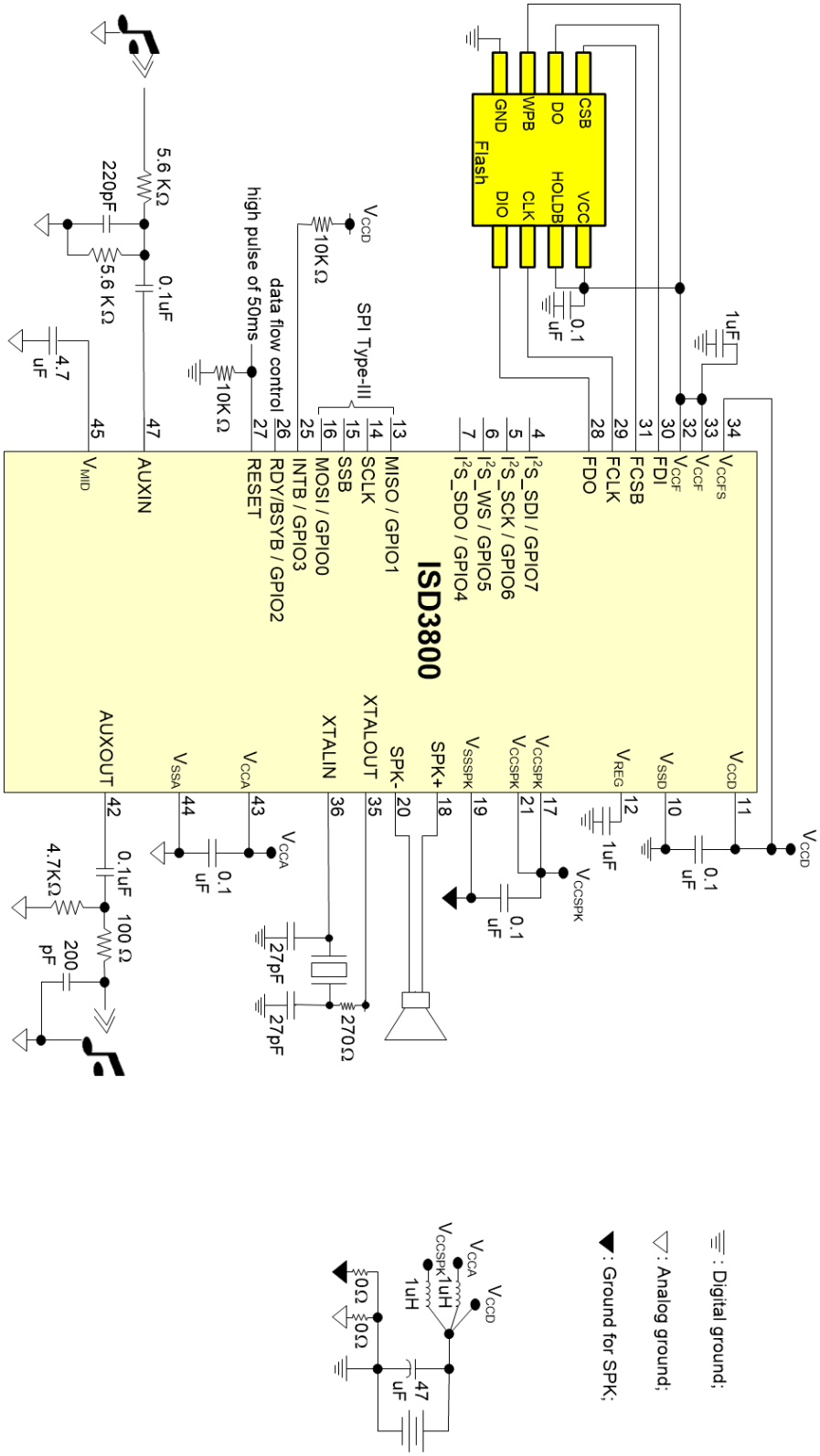


Figure 7-1 ISD3800 Application Diagram – V_{CCF} is regulated internally from V_{CCFS}

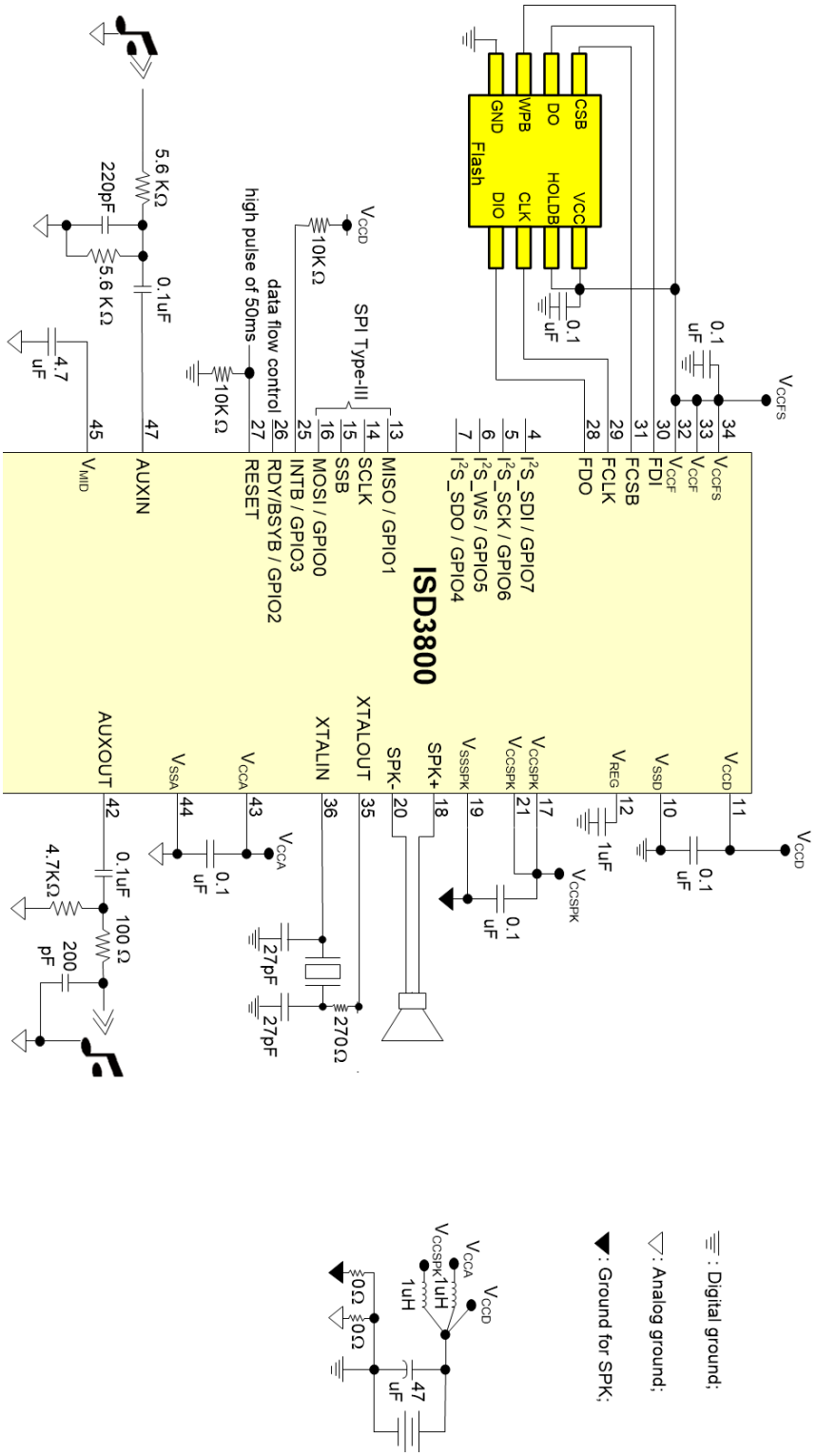
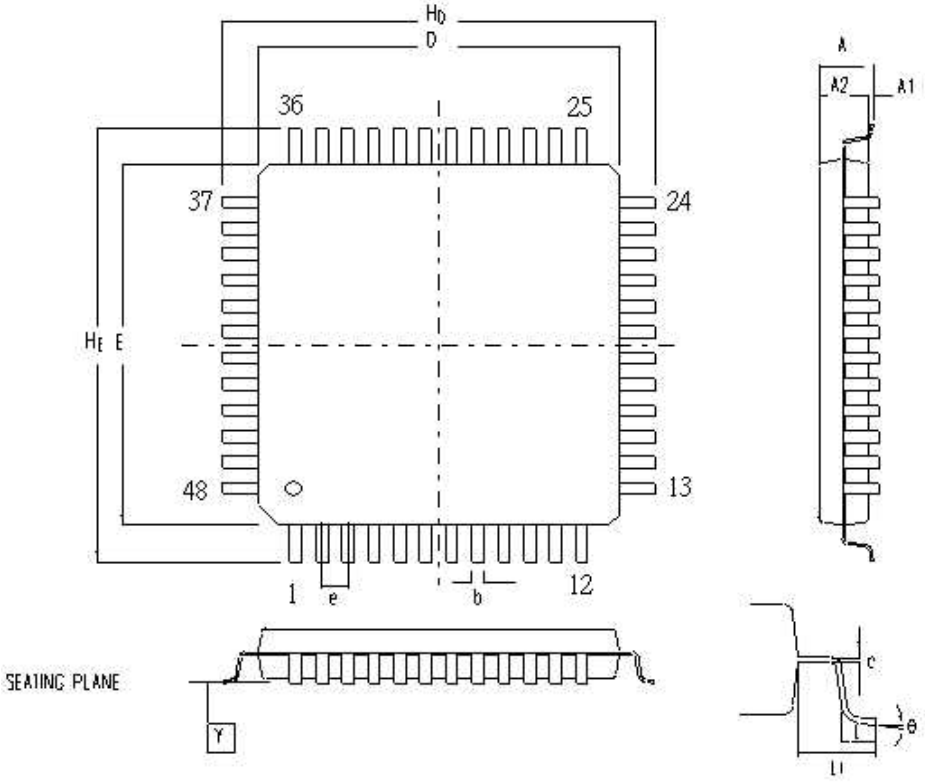


Figure 7-2 ISD3800 Application Diagram – V_{CCF} is tied to V_{CCFS}

8 SPACKAGE SPECIFICATION

8.1 48 LEAD LQFP(7X7X1.4MM FOOTPRINT 2.0MM)

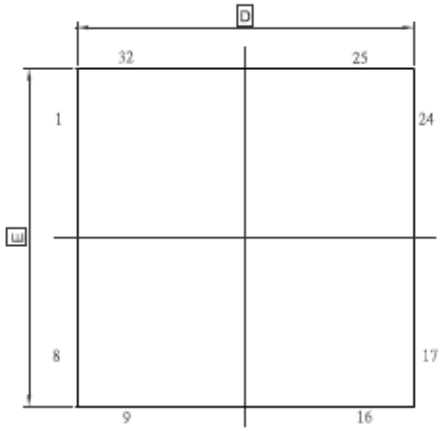


Controlling dimension : Millimeters

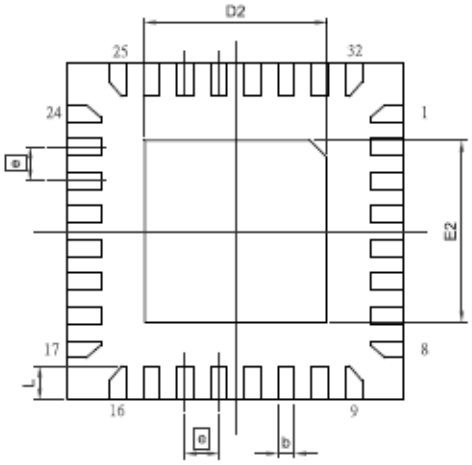
Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

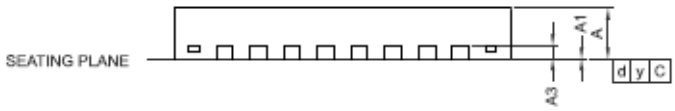
8.2 32 LEAD QFN (5X5 MM^2, THICKNESS 0.8MM ,PITCH 0.5 MM)

TOP VIEW



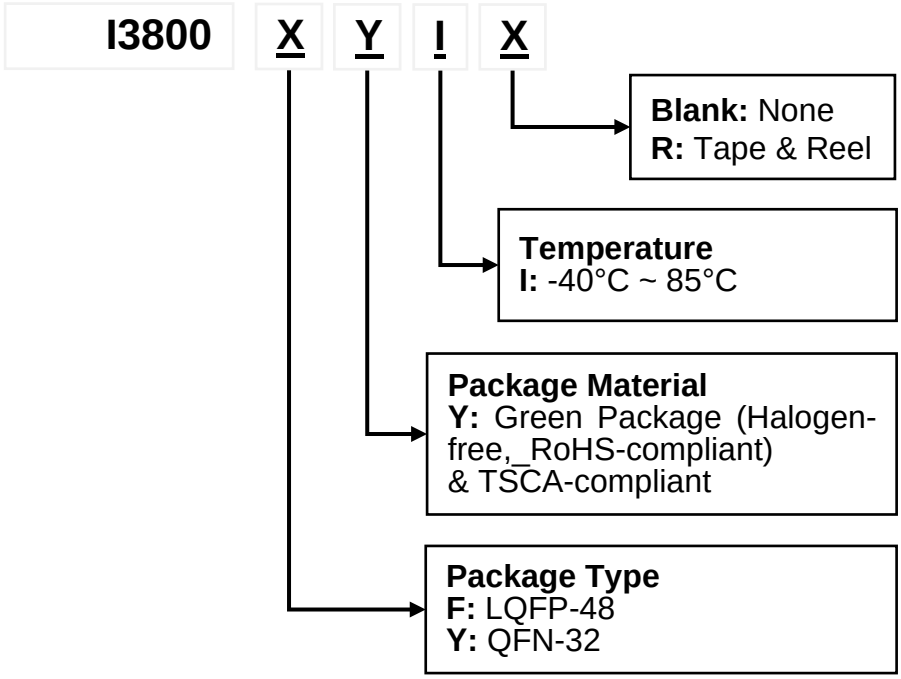
BOTTOM VIEW





SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0275	0.0295	0.0315
A1	0	0.02	0.05	0	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	5.00 BSC			0.197 BSC		
D2	2.60	2.70	2.80	0.1024	0.1063	0.1102
E	5.00 BSC			0.197 BSC		
E2	2.60	2.70	2.80	0.1024	0.1063	0.1102
e	0.50 BSC			0.0197 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
y	0.10			0.0039		

9 ORDERING INFORMATION



Package Number	Part Number	Ordering Number	Duration	Package	Temperature	Notes
ISD3800FYI	ISD3800FYI	I3800FYI	0 ~ 64min	LQFP-48	-40°C ~ 85°C	
ISD3800FYIR	ISD3800FYIR	I3800FYIR	0 ~ 64min	LQFP-48 Tape & Reel	-40°C ~ 85°C	
ISD3800YYI	ISD3800YYI	I3800YYI	0 ~ 64min	QFN-32	-40°C ~ 85°C	
ISD3800YYIR	ISD3800YYIR	I3800YYIR	0 ~ 64min	QFN-32 Tape & Reel	-40°C ~ 85°C	

10 REVISION HISTORY

REVISION	DATE	DESCRIPTION
1.0	Aug 23, 2013	Initial Release
1.1	July 13, 2016	Add storage temperature
1.2	Aug 1,2016	Add absolute maximum ratings Add Talarm temperature threshold typical value
1.3	Mar 29, 2020	Document Format Update
1.4	May 11, 2020	Add QFN32 Package
1.5	Jun 15, 2021	Update Ordering Information Update output power Remove buzzer description
1.6	Feb 1, 2023	Update Halogen-free, RoHS-compliant and TSCA-compliant description

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Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.