

Single P-channel MOSFET

KFJ4B0622ZL

Datasheet

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1. GENERAL DESCRIPTION

Single P-channel MOSFET for automotive.

2. FEATURES

- Drain-source On-state Resistance: $R_{DS(on)}$ typ = 56 m Ω ($V_{GS} = -10$ V)
- CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)
- AEC-Q101 Qualified

3. MARKING SYMBOL: 25

4. PACKAGING

Embossed type (Thermo-compression sealing): 10,000 pcs / reel (standard)

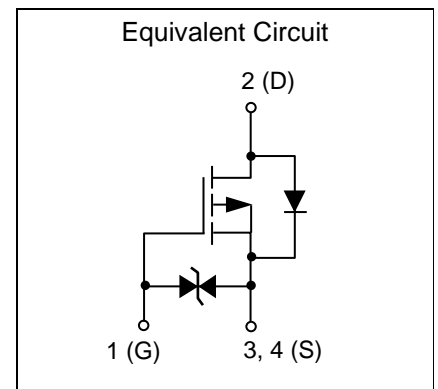
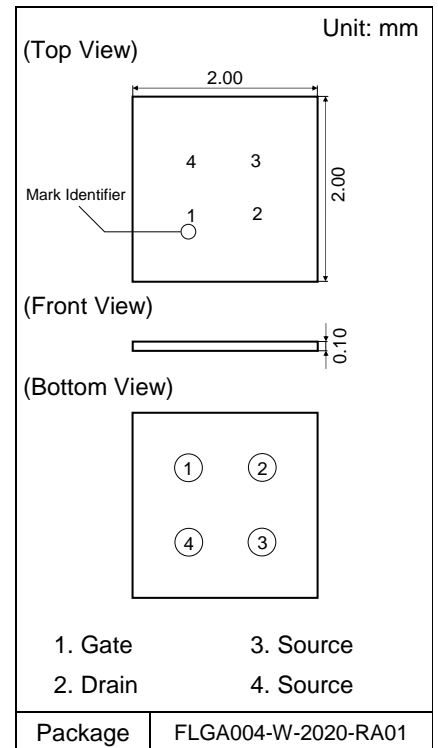
5. ABSOLUTE MAXIMUM RATINGS $T_a = 25$ °C

Parameter		Symbol	Rating	Unit
Drain-source Voltage		VDS	- 60	V
Gate-source Voltage		VGS	- 20 / + 10	V
Drain Current	DC ^{*1}	ID1	- 2.4	A
	DC ^{*2}	ID2	- 3.8	
	DC ^{*3}	ID3	- 4.9	
	Pulsed ^{*4}	IDp	- 30.4	
Total Power Dissipation	DC ^{*1}	PD1	0.45	W
	DC ^{*2}	PD2	1.09	
	DC ^{*3}	PD3	1.79	
Operating Junction and Storage Temperature Range		Tj, Tstg	- 55 to + 150	°C

6. THERMAL CHARACTERISTICS $T_a = 25$ °C

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth1 ^{*1}	280	°C / W
	Rth2 ^{*2}	115	
	Rth3 ^{*3}	70	

- Note
- *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad (65.2 mm² area, 36 μ m thickness).
 - *2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board fully covered with copper pad (616 mm² area, 36 μ m thickness).
 - *3 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).
 - *4 t = 10 μ s, Duty Cycle \leq 1 %.



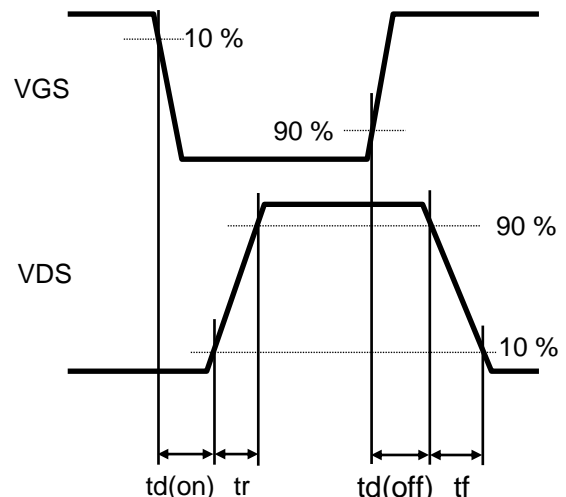
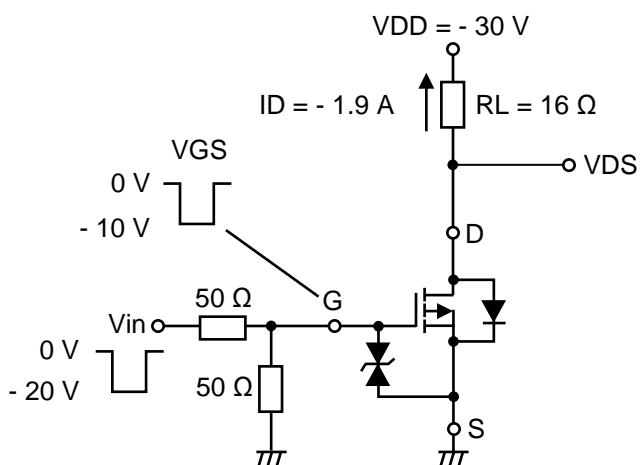
7. ELECTRICAL CHARACTERISTICS $T_a = 25\text{ }^\circ\text{C} \pm 3\text{ }^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = - 1 mA, VGS = 0 V	- 60			V
Zero Gate Voltage Drain Current	IDSS	VDS = - 60 V, VGS = 0 V			- 1	μA
Gate-source Leakage Current	IGSS	VGS = - 16 V, VDS = 0 V			- 10	μA
		VGS = + 8 V, VDS = 0 V			10	
Gate-source Threshold Voltage	Vth	ID = - 11.2 mA, VDS = - 10 V	- 1	- 2	- 3	V
Drain-source On-state Resistance	RDS(on)1	ID = - 1.9 A, VGS = - 10 V	39	56	73	m Ω
	RDS(on)2	ID = - 1.9 A, VGS = - 4.5 V	42	60	100	
Body Diode Forward Voltage	VF(s-d)	IF = - 1.9 A, VGS = 0 V		- 0.77	- 1.2	V
Input Capacitance *1	Ciss	VDS = - 30 V, VGS = 0 V f = 1 MHz		3000		pF
Output Capacitance *1	Coss			110		
Reverse Transfer Capacitance *1	Crss			100		
Turn-on Delay Time *1, *2	td(on)	VDD = - 30 V, VGS = 0 to - 10 V		20		ns
Rise Time *1, *2	tr	ID = - 1.9 A		30		
Turn-off Delay Time *1, *2	td(off)	VDD = - 30 V, VGS = - 10 to 0 V		220		
Fall Time *1, *2	tf	ID = - 1.9 A		90		
Total Gate Charge *1	Qg1	VDD = - 30 V, VGS = - 4.5 V ID = - 3.8 A		21		nC
	Qg2	VDD = - 30 V, VGS = - 10 V ID = - 3.8 A		43		
Gate-source Charge *1	Qgs			5.5		
Gate-drain Charge *1	Qgd			10		

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

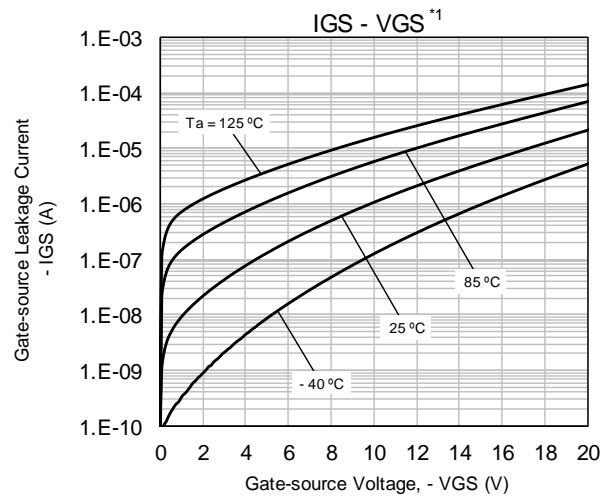
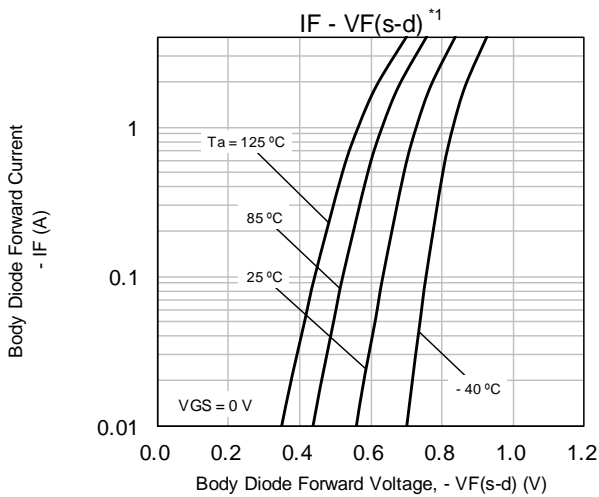
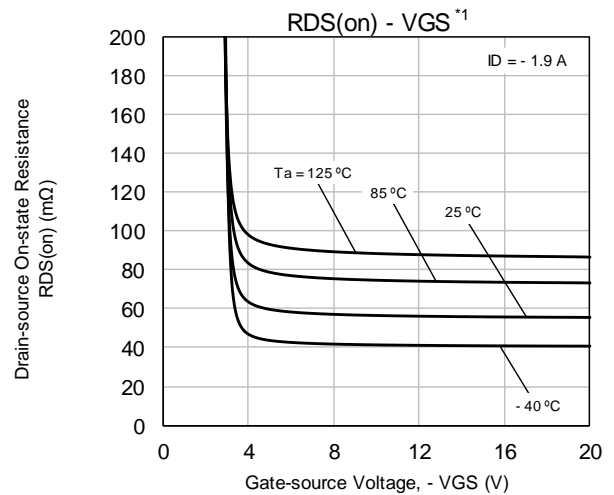
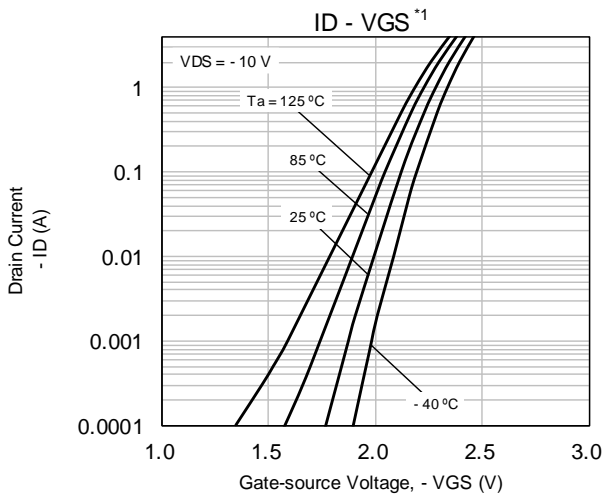
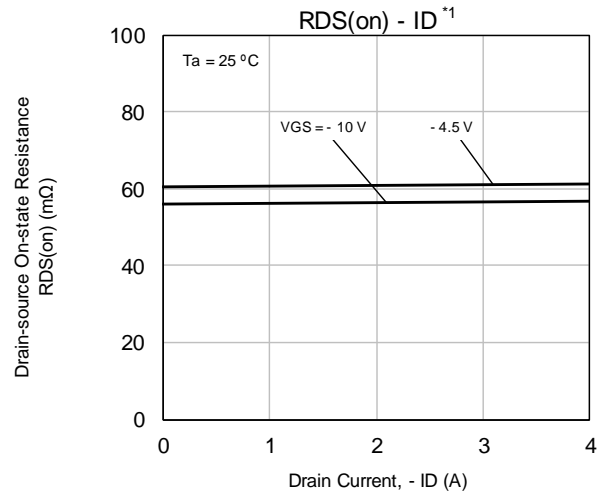
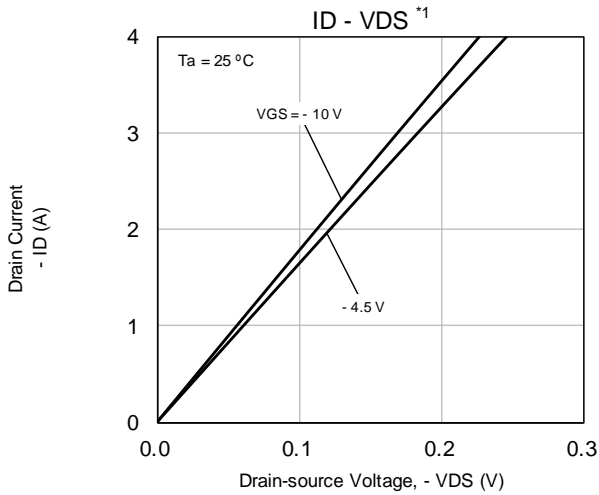
*1 Guaranteed by design, not subject to production testing.

*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.

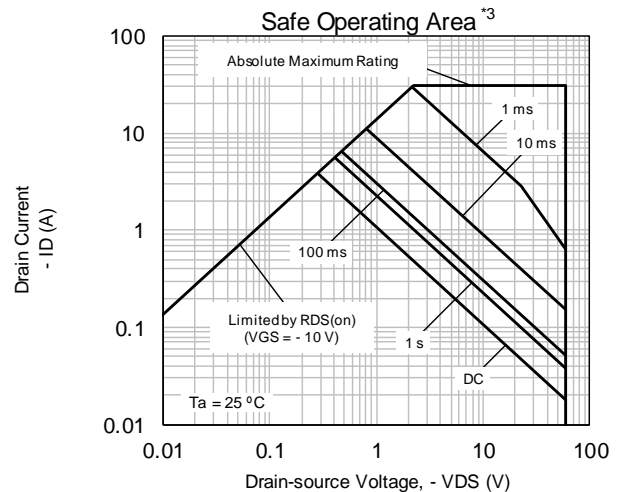
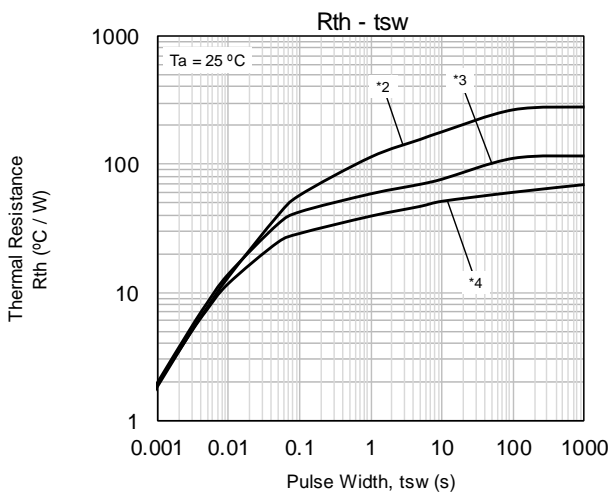
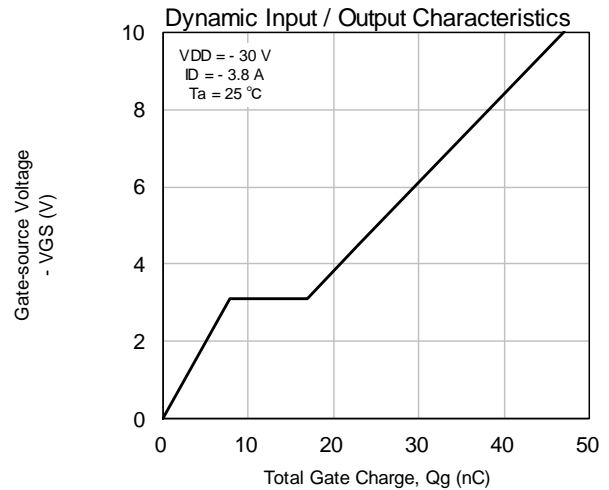
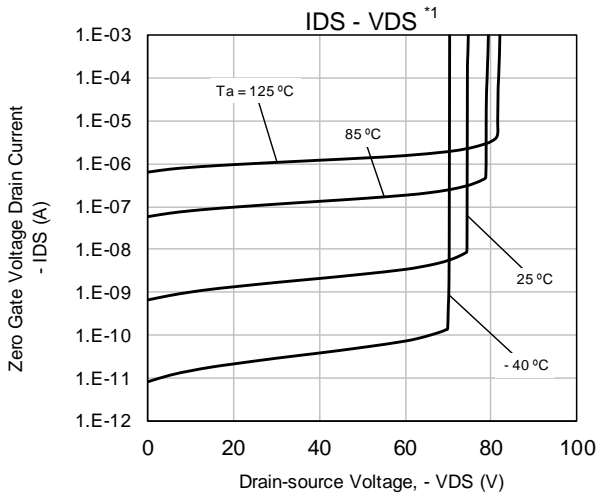


8. TECHNICAL DATA (Reference)

Technical Data (Reference)



TECHNICAL DATA (Reference)



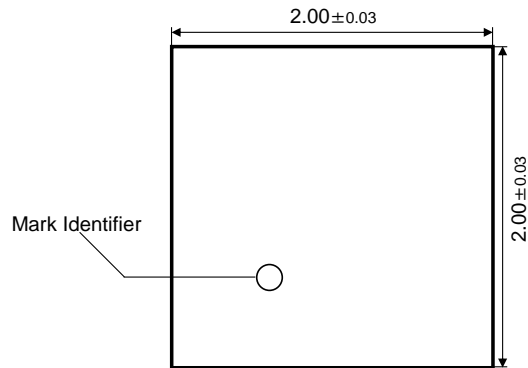
Note

- *1 Pulse measurement.
- *2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad (65.2 mm² area, 36 μm thickness).
- *3 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
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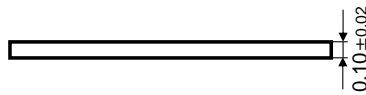
9. OUTLINE

(Top View)

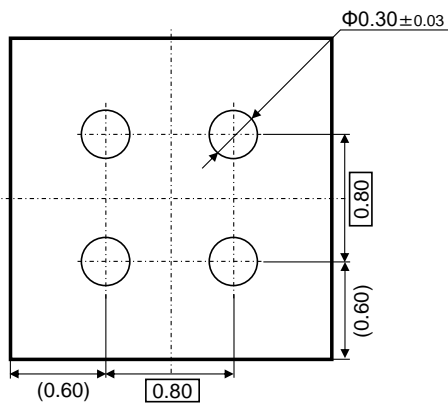
Unit: mm



(Front View)

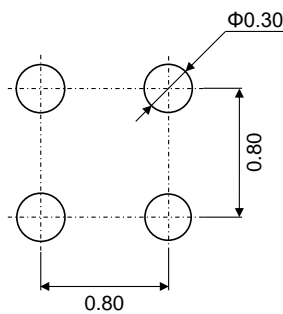


(Bottom View)



10. LAND & STENCIL PATTERN (Reference)

Unit: mm



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.

Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

11. REVISION HISTORY

Date	Revision	Description
2021.11.17	1.00	1. Initially issued.
2021.12.21	2.00	1. Added Technical data.

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