NuMicro® Family
Arm® Cortex-A35-based Microprocessor

MA35D1 Series
Datasheet

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1 GENERAL DESCRIPTION

The NuMicro MA35D1 series is a heterogeneous multi-core microprocessor targeted to high-end edge IIoT gateway. It is based on dual 64-bit Arm Cortex-A35 cores with speed up to 1 GHz, and one 180 MHz Arm Cortex-M4 core. Based on the high-performance cores, the MA35D1 series facilitates the tiny AI/ML for edge computing.

The MA35D1 series has a built-in 128 KB IBR (Internal Boot ROM) and supports secure booting from USB, SD/eMMC, NAND, and SPI Flash (SPI NOR/SPI NAND) modes. The MA35D1 series supports 16-bit DDR2 and DDR3/DDR3L SDRAM. For an easy system design and manufacture, the MA35D1 series also offers LQFP and BGA packages stacked with the DDR2/DDR3L SDRAM and density up to 512 MB to significantly reduce PCB layer, size and electromagnetic interference (EMI).

The MA35D1 series is a trusted system for IoT products' security requirements. It includes several advanced security mechanisms such as Nuvoton Trusted Secure Island (TSI), an isolated secure hardware unit, TrustZone®, secure boot, tamper-detection, built-in cryptographic accelerators with AES, SHA, ECC, RSA, SM2/3/4, and a TRNG, as well as Key Store and OTP memory. All the security operations are performed in the TSI to protect sensitive and high-value data. The features also satisfy customers in IEC 62443 certification requirements.

For high-end edge IIoT gateway requirements, the MA35D1 series integrates PDMA to increase the system performance. The PDMA can access system memory directly without the intervention of the CPU. Also, the MA35D1 series provides multiple advanced and high-speed connection interfaces, such as Gigabit Ethernet, SDIO3.0, USB 2.0 HS, and CAN FD, for edge gateway and new energy applications.

For HMI applications, the MA35D1 series provides a LCD display controller with the resolution up to 1920x1080 at 60 FPS, a 2D graphic engine, a JPEG and a H.264 decoder integrated for better graphical HMI effects and video playback.

The MA35D1 series has highly integrated functions and it is grouped into five sub-systems, Core sub-system, Memory sub-system, Security sub-system, Display, Video sub-system, Connectivity, and I/O sub-system.

1.1 Core Sub-system

The MA35D1 series equipped with dual 64/32-bit Arm Cortex-A35 cores for Armv8-A architecture running up to 1 GHz for high-performance processing data in edge, 32/32 KB I/D L1 cache for each core, and a 512 KB shared L2 cache with Snoop Control Unit (SCU)-L2 cache protection, with Arm TrustZone, Arm Cryptographic Extension Arm NEON™ SIMD Engine and FPU (Floating Point Unit) supported.

The real-time processor Arm Cortex-M4 core runs up to 180 MHz for industrial control in real-time. It includes 16/16 KB I/D cache, FPU (Floating Point Unit), MPU (Memory Protect Unit), and a dedicated 128 KB SRAM for program code execution and data access. Besides, it can extend access to the system SDRAM up to 3.875MB.

In addition to giving data processing and real-time control in edge, the computing power also facilities the basic AI/ML applications.

The MA35D1 series also provides the WWDT (Window Watchdog Timer), RTC (Real Time Clock), hardware semaphore and Wormhole for Cortex-A35 and Cortex-M4 communication, and most peripherals can be allocated to either the Cortex-A35 or Cortex-M4 cores to meet a wide application requirements.

1.2 Memory Sub-system

The MA35D1 series has a built-in 128 KB mask ROM and supports secure booting from USB, SD/eMMC, NAND, and SPI Flash (SPI NOR/SPI NAND).

There are 384 (128 + 256) KB on-chip SRAM and 16-bit DDR2/DDR3/DDR3L SDRAM interface running up to 533 MHz, and up to 2 GB of SDRAM.

The MA35D1 series also supports stacking a DDR2/DDR3L SDRAM device into LQFP and BGA package to ease PCB design with lowered EMI and reduced BOM cost.

1.3 Security Sub-system

The MA35D1 series is a trusted system for IoT products. There are advanced security features to prevent sensitive and high-value data from being eavesdropped on and tampered. MA35D1 series can easily establish encrypted communications, secure data storage, and a secure environment for applications.

Execution Security

The Cortex-A35 is an ARMv8-A architecture with the TrustZone technology, preventing non-secure programs from accessing secure hardware functions to provide a secure environment for applications.

The MA35D1 series also supports secure boot to ensure system image's authenticity and integrity, and avoid executing the malware or unauthorized software implanted on the system.

The MA35D1 series is equipped with a TSI (Trusted Secure Island), which is an isolated secure hardware unit and its operation is not affected the MA35D1 system. All the cryptographic accelerators, Key Store, and OTP memory are built in the TSI, which perform all the security operations, including secure boot and tamper pins detection. The TSI interacts with the MA35D1 through a secure channel that effectively reduces the interfaces of malware attacks and preventing confidential data from being eavesdropped on and tampered with. The TSI also offers RTIC (Run-Time Integrity Checker) mechanism. It periodically checks the integrity of code or data sections in the background without interfering with the MA35D1's normal operation, preventing a Trojan system from being inserted or tampered with.

Communication Security

The MA35D1 series is equipped with several hardware cryptographic accelerators such as AES, SHA, ECC, RSA, SM2/3/4, and TRNG (True Random Number Generator), which facilitates exchanging secret keys, data encryption, and decryption between communications, and reduces the processor load.

Chip-level Storage Security

The MA35D1 series provides Key Store for key management and write-protected OTP (One-Time Programmable) memory for secret key or sensitive data storage to prevent tamper. Key Store and OTP memory can be accessed by the cryptographic engines, retrieving secret keys without the need of CPU access to reduce further risk of leakage of the sensitive cryptographic keys.

Physical Security

There is one pair of dynamic loop tamper pins or two individual tamper pins for tamper detection. Binding the tamper pins with PCB, the data and keys are destroyed if the system is threatened.

1.4 Display and Video Sub-system

For HMI applications, the MA35D1 series supports TFT-LCD display in a parallel RGB interface, the resolution up to 1920x1080 at 60 fps, and the display controller also supports the hardware cursor and OSD (On Screen Display). It also integrates a 2D graphic engine for graphics acceleration, such as BitBlt, rotation, multi-source alpha blending, and color format converting. A hardware JPEG decoder can decode compressed image size from 48x48 to 16368x16368. Another hardware H.264 decoder can decode compressed video stream, which supports resolution up to 1920x1080 at 45 FPS.

There are two sets of camera inputs supporting the video and image input for the image and video capture with machine learning applications.

1.5 Connectivity and I/O Sub-system

For high-end industrial control and edge gateway requirements, the MA35D1 series integrates four sets of PDMA to increase the system performance for peripherals to direct access the system memory without the intervention of the CPU. Also, it provides multiple advanced and high-speed connection interfaces, such as Gigabit Ethernet, SDIO3.0, USB 2.0 HS, and CAN FD.

The MA35D1 series is suitable for a wide range of applications such as:

- Edge Gateway
  - Smart Factory
  - Smart City
  - Smart Building
  - Smart Retail
  - Smart Agriculture
- Tiny AI (Artificial Intelligent) / ML (Machine Learning)
  - Audio Sensing
  - Image Classification
  - Intelligent Data Security
- HMI (Human Machine Interface) & Industrial Control
  - Factory Automation
  - Industrial HMI
  - Smart Home
  - Smart Appliance
- New Energy Applications
  - Smart Grid
  - Smart Power
  - Energy System

2 FEATURES

2.1 MA35D1 Series Features

Core Sub-system	
Arm Cortex-A35	• Dual 64/32-bit Arm Cortex-A35 core running up to 1 GHz • Built-in 32 Kbytes instruction and 32 Kbytes data L1 cache for each core with Memory Management Unit (MMU) • Built-in 512 Kbytes shared L2 cache with Snoop Control Unit (SCU)-L2 cache protection • Arm TrustZone • Arm NEON SIMD Engine and FPU • Arm Cryptographic Extension • Armv8 debug logic • Supports Generic Interrupt Controller (GIC) CPU interface • Supports 64-bit count input for Generic Timer
Arm Cortex-M4	• 32-bit Arm Cortex-M4 processor core running up to 180 MHz • Built-in 16 Kbytes instruction and 16 Kbytes data cache • Built-in Memory Protection Unit (MPU) • Built-in Nested Vectored Interrupt Controller (NVIC) • Hardware IEEE 754 compliant Floating-point Unit (FPU) • DSP extension with hardware divider and single-cycle 32-bit hardware multiplier • 24-bit system tick timer • Programmble and maskable interrupt • Low Power Sleep mode by WFI and WFE instructions

Arm CoreLink® GIC-400 Generic Interrupt Controller (GIC)	• Up to 170 interrupts
	  – 16 Software Generated Interrupt (SGIs)
	  – 4 external Private Peripheral Interrupts (PPIs) for each processor
	  – 1 internal PPI for each processor
	  – 138 Shared Peripheral Interrupt (SPIs)
	• Interrupt Enabled or Disabled
	• Interrupt Prioritized
	• Interrupt to dual Arm Cortex-A35 processor core
	• Level-sensitive interrupt
	• Security Extensions
	  – Group 0 interrupt as Secure interrupts
	  – Group 1 interrupt as Non-secure interrupts
	• Virtualization Extensions

Hardware Semaphore	• Eight hardware semaphores for inter-processor synchronization

	• Support interrupt when semaphore released
Wormhole	• Supports two wormhole controllers for inter-processor communication • Supports interrupt for reset event and power state change event • Four general event interrupts • Eight 16-byte unidirectional message channels, four for each processor • Supports message recall mechanism
Watchdog	• Three Watchdogs, one for TrustZone Secure (TZS), one for TrustZone Secure/Non-Secure (TZS/TZNS) and the other for SubM • 20-bit free running up counter for WDT time-out interval • Supports multiple clock sources from LIRC (default selection), PCLK/4096 or LXT with 9 selectable time-out period • Able to wake up system from Power-down or Idle mode • Time-out event to trigger interrupt or reset system • Supports four WDT reset delay periods, including 1026, 130, 18 or 3 WDT_CLK reset delay period • Configured to force WDT enabled on chip power-on or reset
Window Watchdog	• Three Window Watchdogs, one for TrustZone Secure (TZS), one for TrustZone Secure/Non-Secure (TZS/TZNS) and the other for SubM • Clock sourced from LIRC (default selection) or PCLK/4096; the window set by 6-bit counter with 11-bit prescale • Suspended in Idle/Power-down mode
Real-Time Clock (RTC)	• Real-Time Clock with a separate power domain (V_{BAT}) • RTC clock source including Low-speed external crystal oscillator (LXT) • RTC block including 64 bytes backup registers • Able to wake up CPU • Supports ±5ppm within 5 seconds software clock accuracy compensation • Supports Alarm registers (second, minute, hour, day, month, year) • Supports RTC Time Tick and Alarm Match interrupt • Automatic leap year recognition • Supports 1 Hz clock to be Timer capture source for calibration • Supports 1 pairs dynamic loop tamper pin or 2 individual tamper pin
External Clock Source	• 24 MHz High-speed external crystal oscillator (HXT) for precise timing operation • 32.7688 kHz Low-speed external crystal oscillator (LXT) for RTC function and low-power operation • Supports clock failure detection for external crystal oscillators and exception generatation (NMI)

Internal Clock Source	• 32 kHz Low-speed Internal RC oscillator (LIRC) • 12 MHz High-speed Internal RC oscillator (HIRC) trimmed to 5% accuracy at -40 to 85°C • Six on-chip PLLs up to 1 GHz on-chip PLL, sourced from HXT, allows CPU operation up to the maximim CPU frequency
System Security Memory Configuration Controller (SSMCC)	• Three Arm CoreLink TZC-400 TrustZone Address Space Controllers for seven AXI channels • Configurable security attribution of SDRAM memory • Security violation detection, report and interrupt generation • Programmable SDRAM region for SubM system • Write Protect of security configuration
System Security Peripheral Configuration Controller (SSPCC)	• Configurable security attribution of SRAM by boundary • Configurable security attribution of GPIO by pin • Configurable security attribution of peripherals • Security violation detection, report and interrupt generation • Write Protect of security configuration • Debug interface protection mechanism • Product Lift-cycle Management
Temperature Sensor	• Built-in temperature sensor with ±5°C accuracy
Low Voltage Detect (LVD)	• Two-level LVD with low voltage detect interrupt (2.8V/2.6V)
Low Voltage Reset (LVR)	• LVR with 2.4V threshold voltage level.
Memory Sub-system	
Boot Loader	• Factory pre-loaded 128 Kbytes mask ROM supporting four booting modes – Boot from USB (as device/host) – Boot from SD/eMMC – Boot from NAND Flash – Boot from SPI Flash (SPI-NOR/SPI-NAND)
SRAM	• Up to 384 (128 + 256) KB on-chip SRAM • Supports byte-, half-word- and word-access • Supports PDMA operation
SDRAM	• Supports DDR2 (Double-Data-Rate 2), DDR3 (Double-Data-Rate 3) and DDR3L (DDR3 Low Voltage) type of SDRAM • Clock speed up to 533 MHz • Supports 16-bit data width • SDRAM burst length of 8 • Up to 2 memory ranks • Maximum SDRAM size up to 2 GB (each chip select for 1 GB)

Security Sub-system	
Trusted Secure Island (TSI)	• An isolated secure hardware unit and operation is not affected by MA35D1 system • Built-in cryptographic accelerators, Key Store and OTP memory • Performs all the security operations, including secure boot and tamper-pin detection • Refer to the TSI Application Note document for more detailed information
True Random Number Generator (TRNG)	• Compliant with NIST SP800-90A/B/C and BSI AIS 20/31 • 128-bit random number generation • 128-bit or 256-bit of security strength • Background noise collection to speed reseeding operations • Internal random seeding operation • Start-up, continuous and on-demand health tests
Pseudo Random Number Generator (PRNG)	• Supports 128, 163, 192, 224, 233, 255, 256, 283, 384, 409, 512, 521 and 571 bits random number generation (283~571 bits only generate for Key Store) • Can take the true random number seed from TRNG • Can take the true random number from TRNG (only for Key Store)
Advanced Encryption Standard (AES)	• Hardware AES accelerator • Supports FIPS NIST 197 • Supports SP800-38A and addendum • Supports 128, 192, and 256 bits key • Supports both encryption and decryption • Supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2 and CBC-CS3 modes • Supports CCM mode, GCM mode and GHASH function • Supports SM4 block cipher algorithm • Supports key expander • Supports one technique to improve side-channel attack protection ability
Secure Hash Algorithm (SHA)	• Hardware SHA accelerator • Supports FIPS NIST 180, 180-2, 180-4 • Supports MD5 • Supports SHA-160, SHA-224, SHA-256, SHA-384, SHA-512 and SHA-512/t • Supports SHA3-224, SHA3-256, SHA3-384, SHA3-512, SHAKE128 and SHAKE256 • Supports SM3 Cryptographic Hash Algorithm
Elliptic Curve	• Hardware ECC accelerator

Cryptography (ECC)	• Supports both prime field GF(p) and binary filed GF(2^m) • Supports NIST P-192, P-224, P-256, P-384, and P-521 • Supports NIST B-163, B-233, B-283, B-409, and B-571 • Supports NIST K-163, K-233, K-283, K-409, and K-571 • Supports Curve25519 • Supports Public Key Cryptographic Algorithm SM2 Based on Elliptic Curves • Supports point multiplication, addition and doubling operations in GF(p) and GF(2^m) • Supports modulus division, multiplication, addition and subtraction operations in GF(p) • Supports three techniques to improve side-channel attack protection ability
Rivest、Shamir and Adleman Cryptography (RSA)	• Hardware RSA accelerator • Supports both encryption and decryption with 1024, 2048, 3072 and 4096 bits • Supports CRT decryption with 2048, 3072 and 4096 bits • Supports three techniques to improve side-channel attack protection ability
KeyStore	• Supports programming interface for key management • Supports key size required for Cryptography from 128 bits to 4096 bits • Supports 32 keys for SRAM and 9 keys for OTP at most • Supports crypto engine access or store key in key store directly • Supports ECDH operation with ECC and PRNG engine • Supports to store middle data for RSA CRT and SCAP mode • Supports revoke operation • Supports erase key in SRAM and revoke key in OTP while tamper detected • Supports integrity checking • Supports data scrambling • Supports data remanence prevention at SRAM • Supports silent access for side-channel protection at SRAM
OTP Controller	• Supports 32 bits programming function and reading function • Supports 8kbits Secure OTP memory • Supports data retention more than 10 years • Supports fault tolerant mechanism • Supports read only lock bit • Supports side-band handshaking signals with KeyStore
Display and Video Sub-system	

TFT LCD Display Interface	• Display Interface – Supports parallel pixel output with 24-bit Data, HSync, VSync, Data enable – Supports DPI 24-bit, 18-bit and 16-bit – Supports i80/m68 MPU type interface with optional VSYNC or TE signal • Frame rate up to 1920 x 1080 @ 60 fps • Input Format – ARGB2101010, A/XRGB8888, A/XRGB1555, RGB565, A/XRGB4444 – Index1/2/4/8 – YUV422 packed and semi planar (YUV2, UYVY, NV16) – YUV420 semi-planar (YUY2(P010), NV12 and YUV420 semi-planar 10-bit) • Output Format – DPI_D16CFG1, DPI_D16CFG2, DPI_D16CFG3 – DPI_D18CFG1, DPI_D18CFG2 – DPI_D24 • Color Space Conversion BT.2020 and BT.709 • Supports ARGB888 and Mask cursor formats for hardware cursor • Supports On Screen Display (OSD)
2D Graphic Engine (GFX)	• BitBLT, Stretch Blit and Filter Blit • Line drawing, Rectangle fill and clear • Mono expansion for text rendering • ROP2, ROP3 and ROP4 • Alpha blending, including Java 2 Porter-Duff compositing blending rules • 32K x 32K coordinate system • 90 / 180 / 270 degree rotation • Transparency by monochrome mask, chroma key, or pattern mask • Supports 2x2 in 4x4 tile format • Supports XMajor and YMajor Super Tile 64x64 format • A8 output with rotation in filter blit and bit blit • Supports Source and Destination color key full bypass • Multi source blending – Full support for Multi source blending with variable block size – Up to 8 sources – Programmable block size – Supports 90, 180, 270 degree rotation with different block size • Supports format converting for non-planar YUV to planar YUV • YUV422 output with alpha blending
Video and Image Decoder	**AVC(H.264) / MVC / SVC Decoding**

- Input stream format
  - AVC(H.264) stream including Byte stream and NAL unit stream
  - MVC stream
  - SVC stream
- Output picture format
  - YCbCr 4:2:0 semi-planar raster-scan
  - YCbCr 4:2:0 semi-planar 8x4 tiled
  - YCbCr 4:0:0 (monochrome)
- Frame by frame (field by field) and slice by slice decoding scheme
- Picture size from 48 x 48 to 1920 x 1080 with step size 16 pixels
- Frame rate up to 1920 x 1080 @ 45 fps

JPEG Decoding

- Input picture format
  - JFIF file format 1.02
  - YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
- Output picture format
  - YCbCr4:2:0 semi-planar raster scan
- Picture size from 48 x 48 to 16368 x 16368 with step size 8 pixels
- Supports JPEG compressed thumbnails

Post Processing

- Input data format
  - YCbCr 4:2:0 semi-planar raster-scan
  - YCbCr 4:2:0 semi-planar 8x4 tiled
  - YCbCr 4:2:0 planar
  - YCbCr 4:0:0 (monochrome)
  - YCbYCr 4:2:2, YCrYCb 4:2:2
  - CbYCrY 4:2:2, CrYCbY 4:2:2
- Output data format
  - YCbCr 4:2:0 semi-planar
  - YCbYCr 4:2:2 raster-scan or 4x4 tiled
  - YCrYCb 4:2:2 raster-scan or 4x4 tiled
  - CbYCrY 4:2:2 raster-scan or 4x4 tiled
  - CrYCbY 4:2:2 raster-scan or 4x4 tiled
  - Fully configurable ARGB channel lengths and locations inside 32 bits, such as ARGB 32-bit (8-8-8-8), RGB 16-bit (5-6-5), ARGB 16-bit (4-4-4-4)
- Input image size from 48 x 48 to 16368 x 16368 with step size 8 pixels
- Output image size from 16 x 16 to 1920 x 1080 with horizontal step size 8 and vertical step size 2
- Down Scaling
  - Arbitrary, non-integer scaling ratio separately for both dimensions
  - Unlimited down-scaling ratio

	• Up Scaling – Arbitrary, non-integer scaling ratio separately for both dimensions – Maximum output width is 3x the input width (within the maximum output image size limit) – Maximum output height is 3x the input height – 2 pixels (within the maximum output image size limit) • YCbCr to RGB color conversion – BT.601-5 compliant – BT.709 compliant – User definable conversion coefficient • Dithering • Alpha blending • De-interlacing • Contrast, brightness and color saturation adjustment for RGB image • Supports Image cropping and digital zoom • Picutre in picture, output image masking • Image rotation – Rotation 90, 180 or 270 degrees • Horizontal and vertical flip
CMOS Sensor Interface	• Two sets of CMOS sensor interfaces supporting CCIR601 and CCIR656 type sensor • Resolution up to 3M pixels • Supports YUV422 and RGB565 color format for data output by CMOS image sensor • Supports YUV422, RGB565, RGB555 and Y-only color format with planar and packet data format for data storing to system memory • Supports image cropping and cropping window up to 4096x2048 • Supports vertical and horizontal scaling-down with N/M scaling factor • Supports Negative, Sepia and Posterization color effects
Connectivity and I/O Sub-system	
Peripheral DMA (PDMA)	• Four sets of PDMA with 10 independent and configurable channels for automatic data transfer between memories and peripherals • Basic and Scatter-Gather transfer modes • Each channel supporting circular buffer management using Scatter-Gather Transfer mode • Stride function for rectangle image data movement • Fixed-priority and Round-robin priorities modes • Single and burst transfer types • Byte-, half-word- and word tranfer unit with count up to 65536

	• Incremental or fixed source and destination address

Gigabit Ethernet MAC (GMAC)	• Two sets of Gigabit Ethernet MAC
	• Compliant with IEEE Std 802.3-2008 for Ethernet MAC
	• Compliant with IEEE Std 1588-2008 for precision networked clock synchronization
	• Compliant with IEEE Std 802.3az-2010 for Energy Efficient Ethernet (EEE)
	• Compliant with RGMII specification version 2.6 from HP/Marvell
	• Compliant with RMII specification version 1.2 from RMII consortium
	• Full-duplex operation
	  – IEEE 802.3x flow control automatic transmission of zero-quanta Pause frame on flow control input de-assertion
	  – Forwarding of received Pause frames to the user application
	• Half-duplex operation
	  – CSMA/CD Protocol support
	  – Flow control using backpressure support
	  – Frame bursting and frame extension in 1000 Mbps half-duplex operation
	• Programmable frame length to support Standard or Jumbo Ethernet frames with up to 16 Kbytes of size
	• IEEE 802.1Q VLAN tag detection for reception frames
	• Receive module for checksum off-load for received IPv4 and TCP packets encapsulated by the Ethernet frame (Type 1)
	• Enhanced Receive module for checking IPv4 header checksum and TCP, UDP, or ICMP checksum encapsulated in IPv4 or IPv6 datagrams (Type 2)
	• CRC replacement, Source Address field insertion or replacement, and VLAN insertion, replacement, and deletion in transmitted frames with per-frame control
	• Serial management interface (MDC/MDIO) master mode for PHY device configuration and management
	• Supports Magic Packet recognition to wake system up from Power-down mode

USB 2.0 High Speed with on-chip transceiver	**USB 2.0 High Speed Host/Device** • One set of on-chip USB 2.0 high speed dual role transceiver configurable as host, device or ID-dependent • One set of on-chip USB 2.0 high speed transceiver with host only **USB 2.0 High Speed Host Controller** • Compliant with USB Revision 2.0 Specification • Compatible with EHCI (Enhanced Host Controller Interface) Revision 1.0 • Compatible with OHCI (Open Host Controller Interface) Revision 1.0 • Supports high-speed (480Mbps), full-speed (12Mbps) and low-speed (1.5Mbps) USB devices

	• Integrated with a port routing logic to route full/low speed device to OHCI controller • Supports an integrated Root Hub • Built-in DMA **USB 2.0 High Speed Device Controller** • Compliant with USB Revision 2.0 Specification • Supports up to eight bi-directional endpoints, in addition to control endpoint 0 • Supports Control, Bulk, Interrupt and Isochronous transfers • Supports Descriptor (Scatter-Gather) DMA operation • Supports LPM feature • Supports V_{BUS}/Resume wake-up from system power-down mode
Secure Digital Host Controller (SDHC)	• Two sets of Secure Digital Host Controllers • Supports 1-bit and 4-bit data bus width for SD memory card specification version 3.0. (SDR104 speed limited to maximum allowed I/O speed SPI mode, DDR50 and UHS-II mode not supported) • Supports 1-bit, 4-bit and 8-bit data bus widths for the eMMC interface(HS200 speed limited to maximum allowed I/O speed and HS400 not supported) • Supports SD/SDHC/SDXC/SDIO, eMMC card • Supports SD/eMMC tuning, CMD19(SD) or CMD21(eMMC) • Supports 200 MHz to achieve eMMC HS200 at 1.8V I/O operation
CAN FD	• Four sets of CAN FD controllers • Compliant with CAN protocol version 2.0 part A, B and ISO 11898-1: 2015 • Compliant with CAN FD version 1.0 with up to 64 data bytes supported • Supports CAN Error logging, AUTOSAR and SAE J1938 • Built-in 2K word (32-bit) Message SRAM for each CAN FD controller • Supports power-down
Quad SPI	• Two sets of SPI Quad controllers with Master/Slave mode, up to 100 MHz • Supports Dual and Quad I/O Transfer mode • Supports one data channel half-duplex transfer • Supports receive-only mode • Configurable bit length of a transfer word from 8 to 32-bit • Provides separate 8-level depth transmit and receive FIFO buffers • Supports MSB first or LSB first transfer sequence • Supports the byte reorder function • Supports Byte or Word Suspend mode

	• Supports 3-wired, no slave select signal, bi-direction interface • PDMA operation
SPI/I²S	• Four sets of SPI/I²S controllers with Master/Slave mode • For SPI PDMA function disable, provides separate 8-level of 32-bit or 16-level of 16-bit transmit and receive FIFO buffers • For SPI PDMA function enable, provides separate 8-level of 32-bit, 16-level of 16-bit or 32-level of 8-bit transmit and receive FIFO buffers **SPI** • Up to 100 MHz in Master mode • Configurable bit length of a transfer word from 8 to 32-bit • MSB first or LSB first transfer sequence • Byte reorder function • Supports Byte or Word Suspend mode • Supports one data channel half-duplex transfer • Supports receive-only mode • Supports 3-wired, no slave select signal, bi-direction interface **I²S** • Supports mono and stereo audio data with 8-, 16-, 24- and 32-bit audio data sizes • Supports PCM mode A, PCM mode B, I²S and MSB justified data format • PDMA operation
I²S	• Two sets of I²S interfaces with Master/Slave mode • Supports I²S audio sampling frequencies up to 192 kHz • Supports mono and stereo audio data with 8-, 16-, 24- and 32-bit word sizes • Two 16-level FIFO data buffers, one for transmitting and the other for receiving • Supports I²S protocols: Philips standard, MSB-justified, and LSB-justified data format • Supports PCM protocols: PCM standard, MSB-justified, and LSB-justified data format • PCM protocol supporting TDM multi-channel transmission in one audio sample; the number of data channel can be set as 2, 4, 6 or 8 • PDMA operation
Low-power UART	• 17 sets of UARTs with up to 9.5 MHz baud rate • Auto-Baud Rate measurement and baud rate compensation function • Supports low power UART (LPUART): baud rate clock from LXT(32.768 kHz) with 9600bps in Power-down mode even system clock is stopped • Separated receive and transmit 32/32-byte FIFOs with receive FIFO

	programmable level trigger supported • Auto flow control (nCTS and nRTS) • Supports IrDA (SIR) function • Supports RS-485 9-bit mode and direction control • Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function in idle mode • Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction • Supports wake-up function • 8-bit receiver FIFO time-out detection function • Supports break error, frame error, parity error and receive/transmit FIFO overflow detection function • Supports Single-wire mode • PDMA operation
I²C	• Six sets of I²C devices with Master/Slave mode • Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps) • Supports 10 bits mode • Programmable clocks allowing for versatile rate control • Supports multiple address recognition (four slave address with mask option) • Supports multi-address power-down wake-up function • PDMA operation
Enhanced PWM (EPWM)	• Eighteen 16-bit counters with 12-bit clock prescale for eighteen PWM output channels • Up to 18 independent input capture channels with 16-bit resolution counter • Supports dead zone with maximum divided 12-bit prescale • Up, down or up-down PWM counter type • Supports complementary mode for 3 complementary paired PWM output channels • Synchronous function for phase control • Counter synchronous start function • Brake function with auto recovery mechanism • Mask function and tri-state output for each PWM channel • Able to trigger EADC to start conversion
32-bit Timer	**Timer** • Twelve sets of 32-bit timers with 24-bit up counter and one 8-bit pre-scale counter from independent clock source • One-shot, Periodic, Toggle and Continuous Counting operation modes

	• Event counting function to count the event from external pin • Input capture function to capture or reset counter value • External capture pin event for interval measurement • External capture pin event to reset 24-bit up counter • Chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated • Timer interrupt flag or external capture interrupt flag to trigger EPWM, EADC and PDMA • internal capture triggered from internal clock (HIRC, LIRC) or external clock (HXT, LXT) • Inter-Timer trigger capture mode **PWM** • Twelve16-bit PWM counters with 12-bit clock prescale • Supports 12-bit deadband (dead zone) • Up, down or up-down PWM counter type • Supports brake function • Supports mask function and tri-state output for each PWM channel
Quadrature Encoder Interface (QEI)	• Three sets of QEIs with two QEI phase inputs (QEI_A, QEI_B) and one Index input (QEI_INDEX) each • Supports 2/4 times free-counting mode and 2/4 compare-counting mode • Supports encoder pulse width measurement mode with ECAP
Smart Card Interface	• Two sets of ISO-7816-3 compliant with ISO-7816-3 T=0, T=1 • Supports full duplex UART function • 4-byte FIFOs with programmable level trigger • Programmable guard time selection (11 ETU ~ 266 ETU) • One 24-bit and two 8 bit time-out counters for Answer to Request (ATR) and waiting times processing • Auto inverse convention function • Stop clock level and clock stop (clock keep) function • Transmitter and receiver error retry function • Supports hardware activation, deactivation and warm reset sequence process • Supports hardware auto deactivation sequence after card removal
Enhanced Capture (ECAP)	• Three sets of ECAPs • Input Capture Timer/Counter • Supports three input channels with independent capture counter hold register • 24-bit Input Capture up-counting timer/counter supporting captured events reset and/or reload capture counter • Supports rising edge, falling edge and both edge detector options

	with noise filter in front of input ports • Supports compare-match function
NAND Flash Controller	• Supports SLC and MLC type NAND Flash device • Supports 2 Kbytes, 4 Kbytes and 8 Kbytes page size NAND Flash device • 8-bit data width • Supports EDO mode • Supports ECC8, ECC12 and ECC24 BCH algorithm with ECC code generation, error detection and error correction • Supports dedicated DMA master with Scatter-Gather function to accelerate the data transfer between system memory and NAND Flash
KeyPad Interface (KPI)	• Matrix keypad interface with up to 8x8 array • Programmable de-bounce time • Low-power wake-up mode • Programmable three-key reset • Generate interrupt and update press/release status of all keys once key press or release detected
GPIO	• Supports three I/O modes – Push-Pull output mode – Open-Drain output mode – Input only with high impendence mode • Selectable TTL/Schmitt trigger input • Configured as interrupt source with edge/level trigger setting • Supports independent pull-up/pull-down control
Enhanced Analog-to-Digital Converter (EADC)	• One 12-bit, 4.7 MSPS SAR EADC with up to 8 single-ended input channels or 4 differential input pairs; 10-bit accuracy is guaranteed • One internal channels for Battery power (V_{BAT}) • Supports external V_{REF} pin or internal reference voltage • Analog-to-Digital conversion can be triggered by software enable, external pin, Timer 0~11 overflow pulse trigger, ADINT0 and ADINT1 EOC interrupt pulse trigger, or EPWM trigger • Configurable EADC sampling time • Up to 9 sample modules, supporting double data buffers for sample module 0~3 • Supports PDMA operation
Analog-to-Digital Converter (ADC)	• One 12-bit, 8-ch 500k SPS SAR ADC with up to 8 single-ended input channels; 10-bit accuracy is guaranteed • Supports 4-wire or 5-wire touch screen • Supports external V_{REF} pin
External Bus Interface	• Supports up to three memory banks with individual adjustment of

(EBI)	timing parameter • Each bank supporting dedicated external chip select pin with polarity control and up to 1 Mbytes addressing space • 8-/16-bit data width • Supports byte write enable in 16-bit data width mode • Configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R) • Supports Address/Data multiplexed mode • Supports address bus and data bus separate mode • PDMA operation

3 PARTS INFORMATION

3.1 MA35D1 Series Package Type

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

Part No.	LQFP-EP 216-Pin	BGA 312-Ball	BGA 364-Ball
MA35D1	MA35D16F787C*1 / MA35D16F987C*2	MA35D16A887C*2	MA35D16A087C*3

Note 1: This part number is stacked with the DDR2-type SDRAM. The supply voltage of MV_{DD} power input pin is 1.8V for the internal DDR2-type SDRAM and MV_{REF} = 1/2MV_{DD}.

Note 2: This part number is stacked with the DDR3L-type SDRAM. The supply voltage of MV_{DD} power input pin is 1.35V for the internal DDR3L-type SDRAM and MV_{REF} = 1/2MV_{DD}.

Note 3: The supply voltage of MV_{DD} power input pin depends on the external SDRAM type and MV_{REF_CA} = MV_{REF_DQ} = 1/2MV_{DD}.

Table 3.1-1 MA35D1 Series Package Type

3.2 MA35D1 Series Naming Rule

M	A35	D1	6	A	8	8	7	C
MPU	CPU	Number of CPU	Function	Package	DRAM Size	CPU Speed	Core Code	CAN FD
Nuvoton Microprocessor	Arm A35 Core	D1: Dual A35 Generation 1	6: Display + H.264 decoder	F: LQFP216 A: BGA	0: Non 7: 128 MB 8: 256 MB 9: 512 MB	8: 800 MHz A: 1 GHz	A35 TSI M4 7 Dual 1 1	C: CAN FD N/A

Figure 3-1 MA35D1 Series Part Number Naming Guide

3.3 MA35D1 Series Selection Guide

Part Number		MA35D16F787C / MA35D16F987C	MA35D16A887C	MA35D16A087C
	Cortex-A35	x2	x2	x2
	CPU Frequency	800 MHz	800 MHz	800 MHz
	L1-Cache I/D (KB)	32+32	32+32	32+32
	L2-Cache (KB)	512	512	512
	Real-time Processor with Cortex-M4	x1	x1	x1
	Cortex-M4 I/D Cache (KB)	16+16	16+16	16+16
	SRAM (KB) (Cortex-A35 System + Cortex-M4 RTP)	256+128	256+128	256+128
	Stacked DDR Size (MB)	128 (DDR2*1) / 512 (DDR3L*2)	256 (DDR3L*2)	External*3
	LCD Display (RGB)	24-bit/18-bit	24-bit/18-bit	24-bit/18-bit
	2D Graphic and JPEG Decoder	√	√	√
	H.264 Decoder	√	√	√
	CMOS Sensor Interface	2	2	2
	10 / 100Mb / 1Gb Ethernet MAC	10/100M x1 + 1G x1	1G x2	1G x2
	USB 2.0 HS Host	1	1	1
	USB 2.0 HS Host / Device	1	1	1
	Secure Boot	√	√	√
Booting	USB	√	√	√
	NAND Flash	√	√	√
	SPI-NOR Flash (1/4 bit)	√	√	√
	SPI-NAND (1/4 bit)	√	√	√
	SD/eMMC	√	√	√
Connectivity	UART	17	17	17
	ISO-7816 (Smart Card I/F)	2	2	2
	Quad SPI	2	2	2
	SPI/I^2S	4	4	4
	I^2S	2	2	2
	I^2C	6	6	6
	CAN FD	4	4	4
	SDHC/SDIO/eMMC	2	2	2

Part Number		MA35D16F787C / MA35D16F987C	MA35D16A887C	MA35D16A087C
Crypto	PRNG 512	√	√	√
	AES 256	√	√	√
	RSA 4096	√	√	√
	ECC	√	√	√
	TRNG 128	√	√	√
	SHA 512	√	√	√
	SM 2/3/4	√	√	√
	Key Store	√	√	√
	OTP 8K-bit	√	√	√
	Tamper pin	--	2	2
External Bus Interface		√	√	√
32-bit Timer		10	12	12
Enhanced Capture (ECAP)		3	3	3
Enhanced PWM (EPWM)		18	18	18
Quadrature Encoder Interface (QEI)		3	3	3
12-bit ADC channel		8	8	8
12-bit EADC channel		--	8	8
GPIO		154	208	208
INT		4	4	4
Watchdog		3	3	3
Window Watchdog		3	3	3
RTC (V_{BAT} 3.3V)		√	√	√
Power Control Pin for PMIC		--	√	√
Temperature Sensor		√	√	√
Operating Temperature		-40°C to 85°C	-40°C to 85°C	-40°C to 85°C
Package		LQFP-EP 216-Pin 24x24x1.4mm, 0.4mm pitch	LFBGA 312-Ball 15x15x1.4mm, 0.8mm pitch	LFBGA 364-Ball 14x14x1.4mm, 0.65mm pitch

Note 1: For the internal DDR2-type SDRAM, the supply voltage of MV_{DD} power input pin is 1.8V and MV_{REF} = 1/2MV_{DD}.

Note 2: For the internal DDR3L-type SDRAM, the supply voltage of MV_{DD} power input pin is 1.35V and MV_{REF} = 1/2MV_{DD}.

Note 3: The supply voltage of MV_{DD} power input pin depends on the external SDRAM type and MV_{REF_CA} = MV_{REF_DQ} = 1/2MV_{DD}.

4 PIN CONFIGURATION

4.1 Pin Configuration

4.1.1 MA35D1 Series LQFP-EP 216-Pin Pinout Diagram

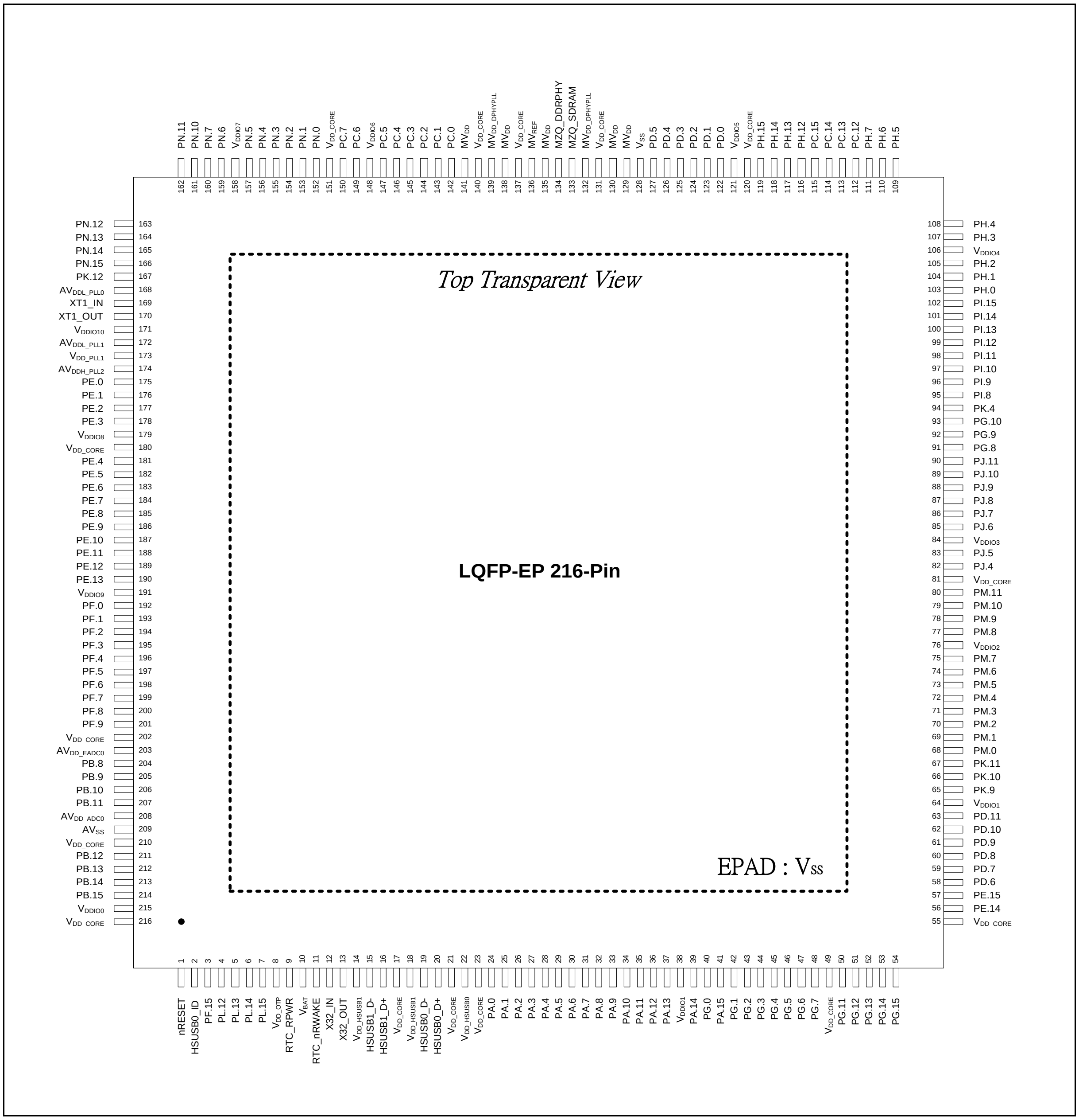


Figure 4-1 NuMicro MA35D1 Series LQFP-EP 216-Pin Pinout Diagram

4.1.2 MA35D1 Series BGA 312-Ball Pinout Diagram

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V
18	V_{SS}	PN.2	PN.3	PC.1	PC.2	PC.0	PC.3	PC.4	PL.5	PL.4	PL.3	PL.0	PL.1	PL.2	PH.14	PH.15	PH.13	V_{SS}
17	PN.5	PN.0	PN.1	V_{SS}	PC.7	PC.6	PC.5	PL.6	PL.7	PL.8	PL.9	PL.10	PL.11	PK.8	PH.12	PC.13	PC.15	PD.1
16	PN.11	PN.7	PN.4	V_{SS}	V_{SS}	PI.6	PK.1	PK.0	PK.3	PK.2	PJ.12	PJ.13	PJ.15	PJ.14	PC.14	PC.12	PD.0	PD.2
15	PN.12	PN.10	PN.6	V_{SS}	V_{SS}	PD.15	PA.15	PI.1	PI.2	PI.0	PI.3	PI.5	PI.4	PI.7	V_{SS}	PD.5	PD.3	PD.4
14	PN.14	PN.13	PK.14	PK.13			PD.13	MV_{REF}	MZQ_DDRPHY	MZQ_SDRAM	PD.14	PD.12			PH.7	PH.6	PH.5	PH.4
13	XT1_IN	XT1_OUT	PK.12	PN.15		V_{DDIO7}	V_{DDIO6}	MV_{DD}	MV_{DD}	MV_{DD}	MV_{DD}	V_{DDIO5}	V_{DDIO4}		PH.3	PH.2	PH.1	PH.0
12	PE.2	PE.1	PE.0	PK.15	AV_{DDL_PLL2}	V_{DD_PLL1}	V_{DDIO10}	V_{DD_CORE}	V_{DD_CORE}	V_{DD_CORE}	V_{DD_CORE}	$MV_{DD\_DPHYPLL}$	V_{DDIO3}	PK.7	PI.14	PI.13	PI.12	PI.11
11	PE.5	PE.6	PE.4	PE.3	V_{DDIO8}	AV_{DDL_PLL1}	AV_{DDL_PLL0}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_CORE}	PK.6	PI.9	PI.8	PI.15	PI.10
10	PE.8	PE.9	PE.7	PE.10	V_{DDIO9}	AV_{DDH_PLL2}	AV_{DDH_PLL1}	AV_{SS_PLL}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_CORE}	PK.5	PK.4	PG.8	PG.9	PG.10
9	PE.11	PE.12	PE.13	PF.0	PH.8	V_{REF_EADC0}	AV_{DD_EADC0}	AV_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_CORE}	PJ.4	PJ.9	PJ.6	PJ.8	PJ.10
8	PF.1	PF.2	PF.3	PF.4	PH.9	AV_{DD}	AV_{DD_ADC0}	V_{DD_CORE}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_CPU}	PJ.5	PJ.3	PJ.2	PJ.11	PJ.7
7	PF.6	PF.7	PF.9	PF.8	RTC_RPWR	V_{BAT}	V_{DD_HSUSB0}	AV_{DDL_ROSC}	V_{DD_CORE}	V_{DD_CORE}	V_{DD_CPU}	V_{DD_CPU}	V_{DD_CPU}	PM.1	PJ.1	PM.8	PM.10	PJ.0
6	PF.5	PF.13	PF.12	PF.10		V_{DD_HSUSB1}	V_{DD_OTP}	V_{DD_CORE}	V_{DD_CORE}	V_{DD_CORE}	V_{DDIO0}	V_{DDIO1}	V_{DDIO2}		PM.9	PM.7	PM.5	PM.6
5	PF.11	EADC0_CH1	EADC0_CH0	PF.14			RTC_nRWAKE	nRESET	HSUSB0_ID	PA.10	PG.6	PA.14			PM.11	PM.3	PM.4	PM.2
4	EADC0_CH2	EADC0_CH5	EADC0_CH4	V_{SS}	PF.15	PA.3	PA.5	PA.7	PA.8	PA.12	PG.4	PG.3	PG.7	PG.11	V_{SS}	PK.11	PM.0	PK.10
3	EADC0_CH6	PB.8	EADC0_CH7	EADC0_CH3	PL.13	PL.15	PA.0	PA.1	PA.6	PA.9	PG.2	PG.5	PM.12	PG.15	PD.7	PD.11	PD.10	PK.9
2	PB.9	PB.11	PB.13	PB.10	PL.14	V_{SS}	X32_OUT	HSUSB1_D-	HSUSB0_D-	PA.4	PA.11	PG.0	PM.14	PG.12	PG.13	PE.15	PD.8	PD.9
1	V_{SS}	PB.12	PB.15	PB.14	PL.12	V_{SS}	X32_IN	HSUSB1_D+	HSUSB0_D+	PA.2	PA.13	PG.1	PM.13	PM.15	PG.14	PE.14	PD.6	V_{SS}

Top Transparent View

Figure 4-2 NuMicro MA35D1 Series BGA 312-Ball Pinout Diagram

4.1.3 MA35D1 Series BGA 364-Ball Pinout Diagram

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y
20	V_{SS}	PC.3	MD14	MD12	MDMask1	MDQS1_N	MD10	MD8	MDQS0_N	MD3	MD0	MCK_P	MD6	MD4	MD5	V_{SS}	PD.3	PD.1	PH.14	V_{SS}
19	PC.1	PC.5	V_{SS}	MD15	MD13	MDQS1_P	MD9	MD11	MDQS0_P	MD2	MD1	MCK_N	MDMask0	MD7	V_{SS}	PD.0	PD.5	PH.12	PH.15	PD.4
18	PN.13	PC.2	PC.0	V_{SS}	MBA2	MA5	MA12	MA1	MCASn	MWEn	MA6	MA4	MA9	MA14	MA8	V_{SS}	PH.13	PD.2	PC.13	PH.4
17	PN.2	PN.0	V_{SS}	V_{SS}	MBA1	MA10	MA3	MA0	MBA0	MRASn	MA2	MA11	MA7	MA15	MA13	V_{SS}	PC.12	PC.15	PH.6	PH.3
16	PN.6	PN.4	V_{SS}	V_{SS}	PC.7	PC.6	V_{SS}	MCS1n	MCKE1	MCKE0	MODT1	MODT0	MRESETn	MCS0n	V_{SS}	PK.7	PH.7	PH.5	PH.1	PI.15
15	XT1_IN	XT1_OUT	PN.5	PC.4	PK.12											PK.5	PH.0	PI.14	PI.13	PI.11
14	PN.11	PN.12	PN.10	PN.3	PN.15		V_{DDIO6}	V_{DD_PLL1}	V_{DDIO10}	$MV_{DD\_DPHYPLL}$	MV_{REF_DQ}	MV_{REF_CA}	MZQ_DDRPHY	V_{DDIO5}		PK.6	PI.10	PI.12	PC.14	PI.9
13	PN.1	PK.15	PK.14	V_{SS}	PK.13		V_{DDIO7}	AV_{DDL_PLL0}	V_{DD_CORE}	MV_{DD}	MV_{DD}	MV_{DD}	MV_{DD}	V_{DDIO4}		PJ.5	PG.9	PK.4	PG.10	PH.2
12	PN.7	PE.1	PE.2	PE.0	PN.14		AV_{DDL_PLL2}	AV_{DDL_PLL1}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_CORE}	V_{DDIO3}		PJ.4	PJ.9	PI.8	PJ.10	PG.8
11	PE.3	PE.8	PE.10	PE.4	EADC0_CH0		AV_{DDH_PLL2}	AV_{DDH_PLL1}	AV_{SS_PLL}	V_{SS}	V_{SS}	V_{SS}	V_{DD_CORE}	V_{DD_CORE}		PL.5	PM.9	PJ.7	PJ.6	PJ.8
10	PE.5	PE.7	PF.2	PE.12	EADC0_CH4		V_{REF_EADC0}	AV_{DD_EADC0}	AV_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_CPU}	V_{DD_CORE}		PL.0	PM.5	PM.6	PJ.11	PJ.2
9	PE.9	PE.13	PF.4	PE.6	PB.8		V_{BAT}	AV_{DD}	AV_{DD_ADC0}	V_{SS}	V_{SS}	V_{SS}	V_{DD_CPU}	V_{DD_CORE}		PM.1	PM.3	PM.4	PJ.1	PJ.0
8	PE.11	PF.7	PF.6	PF.0	PB.10		V_{DD_HSUSB1}	V_{DD_HSUSB0}	V_{DD_CORE}	AV_{DDL_ROSC}	V_{DD_CORE}	V_{DD_CPU}	V_{DD_CPU}	V_{DDIO2}		PL.1	PK.11	PM.2	PM.10	PJ.3
7	PF.1	PF.9	PF.8	PL.15	nRESET		V_{DDIO8}	V_{DDIO9}	V_{DD_OTP}	V_{DD_CORE}	V_{DD_CORE}	V_{DD_CORE}	V_{DDIO0}	V_{DDIO1}		PD.8	PM.11	PM.7	PM.0	PM.8
6	PF.3	PF.12	EADC0_CH1	PF.15	PL.13											PL.7	PE.15	PK.9	PL.4	PK.10
5	PF.5	PF.14	EADC0_CH5	PB.13	PH.9	PH.8	PA.1	PA.3	PA.8	PA.10	PA.14	PA.15	PM.14	PG.15	PK.3	PJ.13	PL.11	PL.3	PL.2	PK.8
4	PF.10	PF.13	PB.11	PB.14	PL.14	RTC_nRWAKE	PA.5	PA.6	PD.13	PA.12	PG.2	PG.6	PG.11	PI.1	PK.1	PJ.15	PL.9	PD.11	PD.6	PD.10
3	PF.11	EADC0_CH2	PB.9	PL.12	RTC_RPWR	HSUSB0_ID	PA.0	PA.9	PA.13	PD.12	PG.4	PM.12	PG.13	PI.3	PI.0	PI.5	PI.7	PD.9	PL.8	PD.7
2	EADC0_CH3	EADC0_CH6	PB.12	V_{SS}	X32_OUT	HSUSB1_D-	HSUSB0_D-	PA.4	PA.7	PD.15	PD.14	PG.7	PM.13	PG.14	PI.4	PJ.14	PJ.12	PK.2	PL.6	PL.10
1	V_{SS}	EADC0_CH7	PB.15	V_{SS}	X32_IN	HSUSB1_D+	HSUSB0_D+	PA.2	PA.11	PG.0	PG.1	PG.3	PG.5	PM.15	PG.12	PI.2	PI.6	PK.0	PE.14	V_{SS}

Top Transparent View

Figure 4-3 NuMicro MA35D1 Series BGA 364-Ball Pinout Diagram

4.2 Pin Description

4.2.1 MA35D1 Series LQFP-EP 216-Pin Pinout Function Table

Pin	Type	MA35D16F787C / MA35D16F987C (LQFP-EP 216-Pin, MCP with 128 / 512 MB DDR) Pin Function
1	I	nRESET / WDT_nRST
2	I	HSUSB0_ID
3	I/O	PF.15 / HSUSB0_VBUSVLD
4	I/O	PL.12 / EPWM0_SYNC_IN / UART7_nCTS / ECAP1_IC0 / UART14_RXD / SPI0_SS0 / I2S1_LRCK / SC1_CLK / EBI_AD0 / HSUSBH_PWREN / I2C2_SDA / TM0 / EPWM0_CH2 / EBI_AD11 / RGMII0_PPS / RMII0_PPS
5	I/O	PL.13 / EPWM0_SYNC_OUT / UART7_nRTS / ECAP1_IC1 / UART14_TXD / SPI0_CLK / I2S1_BCLK / SC1_DAT / EBI_AD1 / HSUSBH_OVC / I2C2_SCL / TM0_EXT / EPWM0_CH3 / EBI_AD12 / RGMII1_PPS / RMII1_PPS
6	I/O	PL.14 / EPWM0_CH2 / UART7_RXD / CAN1_RXD / SPI0_MOSI / I2S1_DI / SC1_RST / EBI_AD2 / TM2 / INT0 / EBI_AD13
7	I/O	PL.15 / EPWM0_CH1 / UART7_TXD / TRACE_CLK / CAN1_TXD / SPI0_MISO / I2S1_DO / SC1_PWR / EBI_AD3 / TM2_EXT / INT2 / EBI_AD14
8	P	V_{DD_OTP}
9	O	RTC_RPWR
10	P	V_{BAT}
11	I	RTC_nRWAKE
12	I	X32_IN
13	O	X32_OUT
14	P	V_{DD_HSUSB1}
15	A	HSUSB1_D-
16	A	HSUSB1_D+
17	P	V_{DD_CORE}
18	P	V_{DD_HSUSB1}
19	A	HSUSB0_D-
20	A	HSUSB0_D+
21	P	V_{DD_CORE}
22	P	V_{DD_HSUSB0}
23	P	V_{DD_CORE}
24	I/O	PA.0 / UART1_nCTS / UART16_RXD / NAND_DATA0 / EBI_AD0 / EBI_ADR0
25	I/O	PA.1 / UART1_nRTS / UART16_TXD / NAND_DATA1 / EBI_AD1 / EBI_ADR1
26	I/O	PA.2 / UART1_RXD / NAND_DATA2 / EBI_AD2 / EBI_ADR2
27	I/O	PA.3 / UART1_TXD / NAND_DATA3 / EBI_AD3 / EBI_ADR3
28	I/O	PA.4 / UART3_nCTS / UART2_RXD / NAND_DATA4 / EBI_AD4 / EBI_ADR4

Pin	Type	MA35D16F787C / MA35D16F987C (LQFP-EP 216-Pin, MCP with 128 / 512 MB DDR) Pin Function
29	I/O	PA.5 / UART3_nRTS / UART2_TXD / NAND_DATA5 / EBI_AD5 / EBI_ADR5
30	I/O	PA.6 / UART3_RXD / NAND_DATA6 / EBI_AD6 / EBI_ADR6
31	I/O	PA.7 / UART3_TXD / NAND_DATA7 / EBI_AD7 / EBI_ADR7
32	I/O	PA.8 / UART5_nCTS / UART4_RXD / NAND_RDY0 / EBI_AD8 / EBI_ADR8
33	I/O	PA.9 / UART5_nRTS / UART4_TXD / NAND_nRE / EBI_AD9 / EBI_ADR9
34	I/O	PA.10 / UART5_RXD / NAND_nWE / EBI_AD10 / EBI_ADR10
35	I/O	PA.11 / UART5_TXD / NAND_CLE / EBI_AD11 / EBI_ADR11
36	I/O	PA.12 / UART7_nCTS / UART8_RXD / NAND_ALE / EBI_AD12 / EBI_ADR12
37	I/O	PA.13 / UART7_nRTS / UART8_TXD / NAND_nCS0 / EBI_AD13 / EBI_ADR13
38	P	V_{DDIO1}
39	I/O	PA.14 / UART7_RXD / CAN3_RXD / NAND_nWP / EBI_AD14 / EBI_ADR14
40	I/O	PG.0 / EPWM0_CH0 / UART7_TXD / CAN3_TXD / SPI0_SS0 / EADC0_ST / EBI_AD15 / I2S1_MCLK / QEI0_INDEX / TM1 / CLKO / INT0 / EBI_ADR15
41	I/O	PA.15 / EPWM0_CH2 / UART9_nCTS / UART6_RXD / I2C4_SDA / CAN2_RXD / EBI_ALE / QEI0_A / TM1 / RGMII0_PPS / RMII0_PPS **Note:** This pin is dedicated as PMIC_nIRQ input function from external PMIC by default.
42	I/O	PG.1 / EPWM0_CH3 / UART9_nRTS / UART6_TXD / I2C4_SCL / CAN2_TXD / EBI_nCS0 / QEI0_B / TM1_EXT / RGMII1_PPS / RMII1_PPS
43	I/O	PG.2 / EPWM0_CH4 / UART9_RXD / CAN0_RXD / SPI0_SS1 / EBI_ADR16 / EBI_nCS2 / QEI0_A / TM3 / INT1
44	I/O	PG.3 / EPWM0_CH5 / UART9_TXD / CAN0_TXD / SPI0_I2SMCLK / EBI_ADR17 / EBI_nCS1 / EBI_MCLK / QEI0_B / TM3_EXT / I2S1_MCLK
45	I/O	PG.4 / EPWM1_CH0 / UART5_nCTS / UART6_RXD / SPI3_SS0 / QEI1_INDEX / EBI_ADR18 / EBI_nCS0 / I2S1_DO / SC1_CLK / TM4 / INT2 / ECAP1_IC2
46	I/O	PG.5 / EPWM1_CH1 / UART5_nRTS / UART6_TXD / SPI3_CLK / ECAP0_IC0 / EBI_ADR19 / EBI_ALE / I2S1_DI / SC1_DAT / TM4_EXT
47	I/O	PG.6 / EPWM1_CH2 / UART5_RXD / CAN1_RXD / SPI3_MOSI / ECAP0_IC1 / EBI_nRD / I2S1_BCLK / SC1_RST / TM7 / INT3
48	I/O	PG.7 / EPWM1_CH3 / UART5_TXD / CAN1_TXD / SPI3_MISO / ECAP0_IC2 / EBI_nWR / I2S1_LRCK / SC1_PWR / TM7_EXT
49	P	V_{DD_CORE}
50	I/O	PG.11 / JTAG_TDO / I2S0_MCLK / NAND_RDY1 / EBI_nWRH / EBI_nCS1 / EBI_AD0
51	I/O	PG.12 / JTAG_TCK/SW_CLK / I2S0_LRCK / EBI_nWRL / EBI_AD1
52	I/O	PG.13 / JTAG_TMS/SW_DIO / I2S0_BCLK / EBI_MCLK / EBI_AD2
53	I/O	PG.14 / JTAG_TDI / I2S0_DI / NAND_nCS1 / EBI_ALE / EBI_AD3
54	I/O	PG.15 / JTAG_nTRST / I2S0_DO / EBI_nCS0 / EBI_AD4
55	P	V_{DD_CORE}
56	I/O	PE.14 / UART0_TXD

Pin	Type	MA35D16F787C / MA35D16F987C (LQFP-EP 216-Pin, MCP with 128 / 512 MB DDR) Pin Function
57	I/O	PE.15 / UART0_RXD
58	I/O	PD.6 / EPWM0_SYNC_IN / UART1_RXD / QSPI1_MOSI1 / I2C0_SDA / I2S0_MCLK / EPWM0_CH0 / EBI_AD5 / SPI3_SS1 / TRACE_CLK **Note:** This pin is dedicated as I2C0_SDA function for controlling external PMIC by default.
59	I/O	PD.7 / EPWM0_SYNC_OUT / UART1_TXD / QSPI1_MISO1 / I2C0_SCL / I2S1_MCLK / EPWM0_CH1 / EBI_AD6 / SC1_nCD / EADC0_ST **Note:** This pin is dedicated as I2C0_SCL function for controlling external PMIC by default.
60	I/O	PD.8 / EPWM0_BRAKE0 / UART16_nCTS / UART15_RXD / QSPI1_SS0 / I2S1_LRCK / EPWM0_CH2 / EBI_AD7 / SC1_CLK / TM0
61	I/O	PD.9 / EPWM0_BRAKE1 / UART16_nRTS / UART15_TXD / QSPI1_CLK / I2S1_BCLK / EPWM0_CH3 / EBI_AD8 / SC1_DAT / TM0_EXT
62	I/O	PD.10 / EPWM1_BRAKE0 / UART16_RXD / QSPI1_MOSI0 / I2S1_DI / EPWM0_CH4 / EBI_AD9 / SC1_RST / TM2
63	I/O	PD.11 / EPWM1_BRAKE1 / UART16_TXD / QSPI1_MISO0 / I2S1_DO / EPWM0_CH5 / EBI_AD10 / SC1_PWR / TM2_EXT
64	P	V_{DDIO1}
65	I/O	PK.9 / I2C3_SCL / CCAP0_SCLK / EBI_AD0 / EBI_ADR0
66	I/O	PK.10 / CAN1_RXD / CCAP0_PIXCLK / EBI_AD1 / EBI_ADR1
67	I/O	PK.11 / CAN1_TXD / CCAP0_HSYNC / EBI_AD2 / EBI_ADR2
68	I/O	PM.0 / I2C4_SDA / CCAP0_VSYNC / EBI_AD3 / EBI_ADR3
69	I/O	PM.1 / I2C4_SCL / SPI3_I2SMCLK / CCAP0_SFIELD / EBI_AD4 / EBI_ADR4
70	I/O	PM.2 / CAN3_RXD / CCAP0_DATA0 / EBI_AD5 / EBI_ADR5
71	I/O	PM.3 / CAN3_TXD / CCAP0_DATA1 / EBI_AD6 / EBI_ADR6
72	I/O	PM.4 / I2C5_SDA / CCAP0_DATA2 / EBI_AD7 / EBI_ADR7
73	I/O	PM.5 / I2C5_SCL / CCAP0_DATA3 / EBI_AD8 / EBI_ADR8
74	I/O	PM.6 / CAN0_RXD / CCAP0_DATA4 / EBI_AD9 / EBI_ADR9
75	I/O	PM.7 / CAN0_TXD / CCAP0_DATA5 / EBI_AD10 / EBI_ADR10
76	P	V_{DDIO2}
77	I/O	PM.8 / I2C0_SDA / CCAP0_DATA6 / EBI_AD11 / EBI_ADR11
78	I/O	PM.9 / I2C0_SCL / CCAP0_DATA7 / EBI_AD12 / EBI_ADR12
79	I/O	PM.10 / EPWM1_CH2 / CAN2_RXD / SPI3_SS0 / CCAP0_DATA8 / SPI2_I2SMCLK / EBI_AD13 / EBI_ADR13
80	I/O	PM.11 / EPWM1_CH3 / CAN2_TXD / SPI3_SS1 / CCAP0_DATA9 / SPI2_SS1 / EBI_AD14 / EBI_ADR14
81	P	V_{DD_CORE}
82	I/O	PJ.4 / I2C3_SDA / SD1_WP
83	I/O	PJ.5 / I2C3_SCL / SD1_nCD
84	P	V_{DDIO3}

Pin	Type	MA35D16F787C / MA35D16F987C (LQFP-EP 216-Pin, MCP with 128 / 512 MB DDR) Pin Function
85	I/O	PJ.6 / CAN3_RXD / SD1_CMD/eMMC1_CMD
86	I/O	PJ.7 / CAN3_TXD / SD1_CLK/eMMC1_CLK
87	I/O	PJ.8 / I2C4_SDA / SD1_DAT0/eMMC1_DAT0
88	I/O	PJ.9 / I2C4_SCL / SD1_DAT1/eMMC1_DAT1
89	I/O	PJ.10 / CAN0_RXD / SD1_DAT2/eMMC1_DAT2
90	I/O	PJ.11 / CAN0_TXD / SD1_DAT3/eMMC1_DAT3
91	I/O	PG.8 / EPWM1_CH4 / UART12_RXD / CAN3_RXD / SPI2_SS0 / LCM_VSYNC/LCM_MPU_RD/EN / I2C3_SDA / EBI_AD7 / EBI_nCS0
92	I/O	PG.9 / EPWM1_CH5 / UART12_TXD / CAN3_TXD / SPI2_CLK / LCM_HSYNC/LCM_MPU_WR/RW / I2C3_SCL / EBI_AD8 / EBI_nCS1
93	I/O	PG.10 / UART12_nRTS / UART13_TXD / SPI2_MOSI / LCM_CLK / EBI_AD9 / EBI_nWRH
94	I/O	PK.4 / UART12_nCTS / UART13_RXD / SPI2_MISO / LCM_DEN/LCM_MPU_RS / EBI_AD10 / EBI_nWRL
95	I/O	PI.8 / UART4_nCTS / UART3_RXD / LCM_DATA0/LCM_MPU_D0 / EBI_AD11
96	I/O	PI.9 / UART4_nRTS / UART3_TXD / LCM_DATA1/LCM_MPU_D1 / EBI_AD12
97	I/O	PI.10 / UART4_RXD / LCM_DATA2/LCM_MPU_D2 / EBI_AD13
98	I/O	PI.11 / UART4_TXD / LCM_DATA3/LCM_MPU_D3 / EBI_AD14
99	I/O	PI.12 / UART6_nCTS / UART5_RXD / LCM_DATA4/LCM_MPU_D4
100	I/O	PI.13 / UART6_nRTS / UART5_TXD / LCM_DATA5/LCM_MPU_D5
101	I/O	PI.14 / UART6_RXD / LCM_DATA6/LCM_MPU_D6
102	I/O	PI.15 / UART6_TXD / LCM_DATA7/LCM_MPU_D7
103	I/O	PH.0 / UART8_nCTS / UART7_RXD / LCM_DATA8/LCM_MPU_D8
104	I/O	PH.1 / UART8_nRTS / UART7_TXD / LCM_DATA9/LCM_MPU_D9
105	I/O	PH.2 / UART8_RXD / LCM_DATA10/LCM_MPU_D10
106	P	V_{DDIO4}
107	I/O	PH.3 / UART8_TXD / LCM_DATA11/LCM_MPU_D11
108	I/O	PH.4 / UART10_nCTS / UART9_RXD / LCM_DATA12/LCM_MPU_D12
109	I/O	PH.5 / UART10_nRTS / UART9_TXD / LCM_DATA13/LCM_MPU_D13
110	I/O	PH.6 / UART10_RXD / LCM_DATA14/LCM_MPU_D14
111	I/O	PH.7 / UART10_TXD / LCM_DATA15/LCM_MPU_D15
112	I/O	PC.12 / UART12_nCTS / UART11_RXD / LCM_DATA16/LCM_MPU_D16
113	I/O	PC.13 / UART12_nRTS / UART11_TXD / LCM_DATA17/LCM_MPU_D17
114	I/O	PC.14 / UART12_RXD / LCM_DATA18/LCM_MPU_CS
115	I/O	PC.15 / UART12_TXD / LCM_DATA19 / LCM_MPU_TE / LCM_MPU_VSYNC
116	I/O	PH.12 / UART14_nCTS / UART13_RXD / LCM_DATA20

Pin	Type	MA35D16F787C / MA35D16F987C (LQFP-EP 216-Pin, MCP with 128 / 512 MB DDR) Pin Function
117	I/O	PH.13 / UART14_nRTS / UART13_TXD / LCM_DATA21
118	I/O	PH.14 / UART14_RXD / LCM_DATA22
119	I/O	PH.15 / UART14_TXD / LCM_DATA23
120	P	V_{DD_CORE}
121	P	V_{DDIO5}
122	I/O	PD.0 / UART3_nCTS / UART4_RXD / QSPI0_SS0
123	I/O	PD.1 / UART3_nRTS / UART4_TXD / QSPI0_CLK
124	I/O	PD.2 / UART3_RXD / QSPI0_MOSI0
125	I/O	PD.3 / UART3_TXD / QSPI0_MISO0
126	I/O	PD.4 / UART1_nCTS / UART2_RXD / I2C2_SDA / QSPI0_MOSI1
127	I/O	PD.5 / UART1_nRTS / UART2_TXD / I2C2_SCL / QSPI0_MISO1
128	P	V_{SS}
129	P	MV_{DD}
130	P	MV_{DD}
131	P	V_{DD_CORE}
132	P	$MV_{DD\_DPHYPLL}$
133	P	MZQ_SDRAM
134	P	MZQ_DDRPHY
135	P	MV_{DD}
136	P	MV_{REF}
137	P	V_{DD_CORE}
138	P	MV_{DD}
139	P	$MV_{DD\_DPHYPLL}$
140	P	V_{DD_CORE}
141	P	MV_{DD}
142	I/O	PC.0 / I2C4_SDA / SD0_CMD/eMMC0_CMD
143	I/O	PC.1 / I2C4_SCL / SD0_CLK/eMMC0_CLK
144	I/O	PC.2 / CAN0_RXD / SD0_DAT0/eMMC0_DAT0
145	I/O	PC.3 / CAN0_TXD / SD0_DAT1/eMMC0_DAT1
146	I/O	PC.4 / I2C5_SDA / SD0_DAT2/eMMC0_DAT2
147	I/O	PC.5 / I2C5_SCL / SD0_DAT3/eMMC0_DAT3
148	P	V_{DDIO6}
149	I/O	PC.6 / CAN1_RXD / SD0_nCD

Pin	Type	MA35D16F787C / MA35D16F987C (LQFP-EP 216-Pin, MCP with 128 / 512 MB DDR) Pin Function
150	I/O	PC.7 / CAN1_TXD / SD0_WP
151	P	V_{DD_CORE}
152	I/O	PN.0 / I2C2_SDA / CCAP1_DATA0
153	I/O	PN.1 / I2C2_SCL / CCAP1_DATA1
154	I/O	PN.2 / CAN0_RXD / CCAP1_DATA2
155	I/O	PN.3 / CAN0_TXD / CCAP1_DATA3
156	I/O	PN.4 / I2C1_SDA / CCAP1_DATA4
157	I/O	PN.5 / I2C1_SCL / CCAP1_DATA5
158	P	V_{DDIO7}
159	I/O	PN.6 / CAN1_RXD / CCAP1_DATA6
160	I/O	PN.7 / CAN1_TXD / CCAP1_DATA7
161	I/O	PN.10 / CAN2_RXD / CCAP1_SCLK
162	I/O	PN.11 / CAN2_TXD / CCAP1_PIXCLK
163	I/O	PN.12 / UART6_nCTS / UART12_RXD / I2C5_SDA / CCAP1_HSYNC
164	I/O	PN.13 / UART6_nRTS / UART12_TXD / I2C5_SCL / CCAP1_VSYNC
165	I/O	PN.14 / UART6_RXD / CAN3_RXD / SPI1_SS1 / CCAP1_SFIELD / SPI1_I2SMCLK
166	I/O	PN.15 / EPWM2_CH4 / UART6_TXD / CAN3_TXD / I2S0_MCLK / SPI1_SS1 / SPI1_I2SMCLK / SC0_nCD / EADC0_ST / CLKO / TM6
167	I/O	PK.12 / EPWM2_CH0 / UART1_nCTS / UART13_RXD / I2C4_SDA / I2S0_LRCK / SPI1_SS0 / SC0_CLK / TM10 / INT2
168	P	AV_{DDL_PLL0}
169	I	XT1_IN
170	O	XT1_OUT
171	P	V_{DDIO10}
172	P	AV_{DDL_PLL1}
173	P	V_{DD_PLL1}
174	P	AV_{DDH_PLL2}
175	I/O	PE.0 / UART9_nCTS / UART8_RXD / CCAP1_DATA0 / RGMII0_MDC / RMII0_MDC
176	I/O	PE.1 / UART9_nRTS / UART8_TXD / CCAP1_DATA1 / RGMII0_MDIO / RMII0_MDIO
177	I/O	PE.2 / UART9_RXD / CCAP1_DATA2 / RGMII0_TXCTL / RMII0_TXEN
178	I/O	PE.3 / UART9_TXD / CCAP1_DATA3 / RGMII0_TXD0 / RMII0_TXD0
179	P	V_{DDIO8}
180	P	V_{DD_CORE}
181	I/O	PE.4 / UART4_nCTS / UART3_RXD / CCAP1_DATA4 / RGMII0_TXD1 / RMII0_TXD1

Pin	Type	MA35D16F787C / MA35D16F987C (LQFP-EP 216-Pin, MCP with 128 / 512 MB DDR) Pin Function
182	I/O	PE.5 / UART4_nRTS / UART3_TXD / CCAP1_DATA5 / RGMII0_RXCLK / RMII0_REFCLK
183	I/O	PE.6 / UART4_RXD / CCAP1_DATA6 / RGMII0_RXCTL / RMII0_CRSDV
184	I/O	PE.7 / UART4_TXD / CCAP1_DATA7 / RGMII0_RXD0 / RMII0_RXD0
185	I/O	PE.8 / UART13_nCTS / UART12_RXD / CCAP1_SCLK / RGMII0_RXD1 / RMII0_RXD1
186	I/O	PE.9 / UART13_nRTS / UART12_TXD / CCAP1_PIXCLK / RGMII0_RXD2 / RMII0_RXERR
187	I/O	PE.10 / UART15_nCTS / UART14_RXD / SPI1_SS0 / CCAP1_HSYNC / RGMII0_RXD3
188	I/O	PE.11 / UART15_nRTS / UART14_TXD / SPI1_CLK / CCAP1_VSYNC / RGMII0_TXCLK
189	I/O	PE.12 / UART15_RXD / SPI1_MOSI / CCAP1_DATA8 / RGMII0_TXD2
190	I/O	PE.13 / UART15_TXD / SPI1_MISO / CCAP1_DATA9 / RGMII0_TXD3
191	P	V_{DDIO9}
192	I/O	PF.0 / UART2_nCTS / UART1_RXD / RGMII0_RXD3 / RGMII1_MDC / RMII1_MDC / KPI_COL0
193	I/O	PF.1 / UART2_nRTS / UART1_TXD / RGMII0_TXCLK / RGMII1_MDIO / RMII1_MDIO / KPI_COL1
194	I/O	PF.2 / UART2_RXD / RGMII0_TXD2 / RGMII1_TXCTL / RMII1_TXEN / KPI_COL2
195	I/O	PF.3 / UART2_TXD / RGMII0_TXD3 / RGMII1_TXD0 / RMII1_TXD0 / KPI_COL3
196	I/O	PF.4 / UART11_nCTS / UART10_RXD / I2S0_LRCK / SPI1_SS0 / RGMII1_TXD1 / RMII1_TXD1 / CAN2_RXD / KPI_ROW0
197	I/O	PF.5 / UART11_nRTS / UART10_TXD / I2S0_BCLK / SPI1_CLK / RGMII1_RXCLK / RMII1_REFCLK / CAN2_TXD / KPI_ROW1
198	I/O	PF.6 / UART11_RXD / I2S0_DI / SPI1_MOSI / RGMII1_RXCTL / RMII1_CRSDV / I2C4_SDA / SC0_CLK / KPI_ROW2
199	I/O	PF.7 / UART11_TXD / I2S0_DO / SPI1_MISO / RGMII1_RXD0 / RMII1_RXD0 / I2C4_SCL / SC0_DAT / KPI_ROW3
200	I/O	PF.8 / UART13_RXD / I2C5_SDA / SPI0_SS0 / RGMII1_RXD1 / RMII1_RXD1 / SC0_RST / KPI_COL4
201	I/O	PF.9 / UART13_TXD / I2C5_SCL / SPI0_SS1 / RGMII1_RXD2 / RMII1_RXERR / SC0_PWR / KPI_COL5
202	P	V_{DD_CORE}
203	P	AV_{DD_EADC0}
204	I/O	PB.8 / EPWM2_BRAKE0 / UART2_nCTS / UART1_RXD / I2C2_SDA / SPI0_SS1 / SPI0_I2SMCLK / ADC0_CH0 / EBI_nCS0 / TM4 / QEI2_INDEX / KPI_ROW6
205	I/O	PB.9 / EPWM2_CH4 / UART2_nRTS / UART1_TXD / I2C2_SCL / SPI0_CLK / I2S0_MCLK / CCAP1_HSYNC / ADC0_CH1 / EBI_ALE / EBI_AD13 / TM0_EXT / I2S1_MCLK / SC0_nCD / QEI2_A / KPI_ROW7
206	I/O	PB.10 / EPWM2_CH5 / UART2_RXD / CAN0_RXD / SPI0_MOSI / EBI_MCLK / CCAP1_VSYNC / ADC0_CH2 / EBI_ADR15 / EBI_AD14 / TM5 / I2C1_SDA / INT1 / QEI2_B
207	I/O	PB.11 / EPWM2_BRAKE1 / UART2_TXD / CAN0_TXD / SPI0_MISO / I2S1_MCLK / CCAP1_SFIELD / ADC0_CH3 / EBI_nCS2 / EBI_ALE / TM5_EXT / I2C1_SCL / INT2 / QEI2_INDEX
208	P	AV_{DD_ADC0}
209	P	AV_{SS}

Pin	Type	MA35D16F787C / MA35D16F987C (LQFP-EP 216-Pin, MCP with 128 / 512 MB DDR) Pin Function
210	P	V_{DD_CORE}
211	I/O	PB.12 / EPWM2_CH0 / UART4_nCTS / UART3_RXD / I2C3_SDA / CAN2_RXD / I2S1_LRCK / ADC0_CH4 / EBI_ADR16 / ECAP2_IC0
212	I/O	PB.13 / EPWM2_CH1 / UART4_nRTS / UART3_TXD / I2C3_SCL / CAN2_TXD / I2S1_BCLK / ADC0_CH5 / EBI_ADR17 / ECAP2_IC1
213	I/O	PB.14 / EPWM2_CH2 / UART4_RXD / CAN1_RXD / I2C4_SDA / I2S1_DI / ADC0_CH6 / EBI_ADR18 / ECAP2_IC2
214	I/O	PB.15 / EPWM2_CH3 / UART4_TXD / CAN1_TXD / I2C4_SCL / I2S1_DO / ADC0_CH7 / EBI_ADR19
215	P	V_{DDIO0}
216	P	V_{DD_CORE}
EPAD	P	V_{SS}

4.2.2 MA35D1 Series BGA 312-Ball Pinout Function Table

Pin	Type	MA35D16A887C (BGA 312-Ball, MCP with 256 Mbytes DDR3L) Pin Function
A1	P	V_{SS}
A2	I/O	PB.9 / EPWM2_CH4 / UART2_nRTS / UART1_TXD / I2C2_SCL / SPI0_CLK / I2S0_MCLK / CCAP1_HSYNC / ADC0_CH1 / EBI_ALE / EBI_AD13 / TM0_EXT / I2S1_MCLK / SC0_nCD / QEI2_A / KPI_ROW7
A3	A	EADC0_CH6
A4	A	EADC0_CH2
A5	I/O	PF.11 / UART13_nRTS / I2S0_BCLK / SPI1_CLK / RGMII1_TXCLK / SC0_DAT / KPI_COL7
A6	I/O	PF.5 / UART11_nRTS / UART10_TXD / I2S0_BCLK / SPI1_CLK / RGMII1_RXCLK / RMII1_REFCLK / CAN2_TXD / KPI_ROW1
A7	I/O	PF.6 / UART11_RXD / I2S0_DI / SPI1_MOSI / RGMII1_RXCTL / RMII1_CRSDV / I2C4_SDA / SC0_CLK / KPI_ROW2
A8	I/O	PF.1 / UART2_nRTS / UART1_TXD / RGMII0_TXCLK / RGMII1_MDIO / RMII1_MDIO / KPI_COL1
A9	I/O	PE.11 / UART15_nRTS / UART14_TXD / SPI1_CLK / CCAP1_VSYNC / RGMII0_TXCLK
A10	I/O	PE.8 / UART13_nCTS / UART12_RXD / CCAP1_SCLK / RGMII0_RXD1 / RMII0_RXD1
A11	I/O	PE.5 / UART4_nRTS / UART3_TXD / CCAP1_DATA5 / RGMII0_RXCLK / RMII0_REFCLK
A12	I/O	PE.2 / UART9_RXD / CCAP1_DATA2 / RGMII0_TXCTL / RMII0_TXEN
A13	I	XT1_IN
A14	I/O	PN.14 / UART6_RXD / CAN3_RXD / SPI1_SS1 / CCAP1_SFIELD / SPI1_I2SMCLK
A15	I/O	PN.12 / UART6_nCTS / UART12_RXD / I2C5_SDA / CCAP1_HSYNC
A16	I/O	PN.11 / CAN2_TXD / CCAP1_PIXCLK
A17	I/O	PN.5 / I2C1_SCL / CCAP1_DATA5
A18	P	V_{SS}
B1	I/O	PB.12 / EPWM2_CH0 / UART4_nCTS / UART3_RXD / I2C3_SDA / CAN2_RXD / I2S1_LRCK / ADC0_CH4 / EBI_ADR16 / ECAP2_IC0
B2	I/O	PB.11 / EPWM2_BRAKE1 / UART2_TXD / CAN0_TXD / SPI0_MISO / I2S1_MCLK / CCAP1_SFIELD / ADC0_CH3 / EBI_nCS2 / EBI_ALE / TM5_EXT / I2C1_SCL / INT2 / QEI2_INDEX
B3	I/O	PB.8 / EPWM2_BRAKE0 / UART2_nCTS / UART1_RXD / I2C2_SDA / SPI0_SS1 / SPI0_I2SMCLK / ADC0_CH0 / EBI_nCS0 / TM4 / QEI2_INDEX / KPI_ROW6
B4	A	EADC0_CH5
B5	A	EADC0_CH1
B6	I/O	PF.13 / I2S0_DO / SPI1_MISO / RGMII1_TXD3 / SC0_PWR / KPI_ROW5
B7	I/O	PF.7 / UART11_TXD / I2S0_DO / SPI1_MISO / RGMII1_RXD0 / RMII1_RXD0 / I2C4_SCL / SC0_DAT / KPI_ROW3
B8	I/O	PF.2 / UART2_RXD / RGMII0_TXD2 / RGMII1_TXCTL / RMII1_TXEN / KPI_COL2
B9	I/O	PE.12 / UART15_RXD / SPI1_MOSI / CCAP1_DATA8 / RGMII0_TXD2
B10	I/O	PE.9 / UART13_nRTS / UART12_TXD / CCAP1_PIXCLK / RGMII0_RXD2 / RMII0_RXERR

Pin	Type	MA35D16A887C (BGA 312-Ball, MCP with 256 Mbytes DDR3L) Pin Function
B11	I/O	PE.6 / UART4_RXD / CCAP1_DATA6 / RGMII0_RXCTL / RMII0_CRSDV
B12	I/O	PE.1 / UART9_nRTS / UART8_TXD / CCAP1_DATA1 / RGMII0_MDIO / RMII0_MDIO
B13	O	XT1_OUT
B14	I/O	PN.13 / UART6_nRTS / UART12_TXD / I2C5_SCL / CCAP1_VSYNC
B15	I/O	PN.10 / CAN2_RXD / CCAP1_SCLK
B16	I/O	PN.7 / CAN1_TXD / CCAP1_DATA7
B17	I/O	PN.0 / I2C2_SDA / CCAP1_DATA0
B18	I/O	PN.2 / CAN0_RXD / CCAP1_DATA2
C1	I/O	PB.15 / EPWM2_CH3 / UART4_TXD / CAN1_TXD / I2C4_SCL / I2S1_DO / ADC0_CH7 / EBI_ADR19
C2	I/O	PB.13 / EPWM2_CH1 / UART4_nRTS / UART3_TXD / I2C3_SCL / CAN2_TXD / I2S1_BCLK / ADC0_CH5 / EBI_ADR17 / ECAP2_IC1
C3	A	EADC0_CH7
C4	A	EADC0_CH4
C5	A	EADC0_CH0
C6	I/O	PF.12 / I2S0_DI / SPI1_MOSI / RGMII1_TXD2 / SC0_RST / KPI_ROW4
C7	I/O	PF.9 / UART13_TXD / I2C5_SCL / SPI0_SS1 / RGMII1_RXD2 / RMII1_RXERR / SC0_PWR / KPI_COL5
C8	I/O	PF.3 / UART2_TXD / RGMII0_TXD3 / RGMII1_TXD0 / RMII1_TXD0 / KPI_COL3
C9	I/O	PE.13 / UART15_TXD / SPI1_MISO / CCAP1_DATA9 / RGMII0_TXD3
C10	I/O	PE.7 / UART4_TXD / CCAP1_DATA7 / RGMII0_RXD0 / RMII0_RXD0
C11	I/O	PE.4 / UART4_nCTS / UART3_RXD / CCAP1_DATA4 / RGMII0_TXD1 / RMII0_TXD1
C12	I/O	PE.0 / UART9_nCTS / UART8_RXD / CCAP1_DATA0 / RGMII0_MDC / RMII0_MDC
C13	I/O	PK.12 / EPWM2_CH0 / UART1_nCTS / UART13_RXD / I2C4_SDA / I2S0_LRCK / SPI1_SS0 / SC0_CLK / TM10 / INT2
C14	I/O	PK.14 / EPWM2_CH2 / UART1_RXD / CAN3_RXD / I2S0_DI / SPI1_MOSI / SC0_RST / I2C5_SDA / TM11 / INT3
C15	I/O	PN.6 / CAN1_RXD / CCAP1_DATA6
C16	I/O	PN.4 / I2C1_SDA / CCAP1_DATA4
C17	I/O	PN.1 / I2C2_SCL / CCAP1_DATA1
C18	I/O	PN.3 / CAN0_TXD / CCAP1_DATA3
D1	I/O	PB.14 / EPWM2_CH2 / UART4_RXD / CAN1_RXD / I2C4_SDA / I2S1_DI / ADC0_CH6 / EBI_ADR18 / ECAP2_IC2
D2	I/O	PB.10 / EPWM2_CH5 / UART2_RXD / CAN0_RXD / SPI0_MOSI / EBI_MCLK / CCAP1_VSYNC / ADC0_CH2 / EBI_ADR15 / EBI_AD14 / TM5 / I2C1_SDA / INT1 / QEI2_B
D3	A	EADC0_CH3
D4	P	V_{SS}

Pin	Type	MA35D16A887C (BGA 312-Ball, MCP with 256 Mbytes DDR3L) Pin Function
D5	I/O	PF.14 / EPWM2_BRAKE0 / EADC0_ST / RGMII1_PPS / RMII1_PPS / SPI0_I2SMCLK / SPI1_I2SMCLK / CCAP1_SFIELD / RGMII0_PPS / RMII0_PPS / TM0 / INT0 / SPI1_SS1 / QEI2_INDEX / I2S0_MCLK
D6	I/O	PF.10 / UART13_nCTS / I2S0_LRCK / SPI1_SS0 / RGMII1_RXD3 / SC0_CLK / KPI_COL6
D7	I/O	PF.8 / UART13_RXD / I2C5_SDA / SPI0_SS0 / RGMII1_RXD1 / RMII1_RXD1 / SC0_RST / KPI_COL4
D8	I/O	PF.4 / UART11_nCTS / UART10_RXD / I2S0_LRCK / SPI1_SS0 / RGMII1_TXD1 / RMII1_TXD1 / CAN2_RXD / KPI_ROW0
D9	I/O	PF.0 / UART2_nCTS / UART1_RXD / RGMII0_RXD3 / RGMII1_MDC / RMII1_MDC / KPI_COL0
D10	I/O	PE.10 / UART15_nCTS / UART14_RXD / SPI1_SS0 / CCAP1_HSYNC / RGMII0_RXD3
D11	I/O	PE.3 / UART9_TXD / CCAP1_DATA3 / RGMII0_TXD0 / RMII0_TXD0
D12	I/O	PK.15 / EPWM2_CH3 / UART1_TXD / CAN3_TXD / I2S0_DO / SPI1_MISO / SC0_PWR / I2C5_SCL / TM11_EXT
D13	I/O	PN.15 / EPWM2_CH4 / UART6_TXD / CAN3_TXD / I2S0_MCLK / SPI1_SS1 / SPI1_I2SMCLK / SC0_nCD / EADC0_ST / CLKO / TM6
D14	I/O	PK.13 / EPWM2_CH1 / UART1_nRTS / UART13_TXD / I2C4_SCL / I2S0_BCLK / SPI1_CLK / SC0_DAT / TM10_EXT
D15	P	V_{SS}
D16	P	V_{SS}
D17	P	V_{SS}
D18	I/O	PC.1 / I2C4_SCL / SD0_CLK/eMMC0_CLK
E1	I/O	PL.12 / EPWM0_SYNC_IN / UART7_nCTS / ECAP1_IC0 / UART14_RXD / SPI0_SS0 / I2S1_LRCK / SC1_CLK / EBI_AD0 / HSUSBH_PWREN / I2C2_SDA / TM0 / EPWM0_CH2 / EBI_AD11 / RGMII0_PPS / RMII0_PPS
E2	I/O	PL.14 / EPWM0_CH2 / UART7_RXD / CAN1_RXD / SPI0_MOSI / I2S1_DI / SC1_RST / EBI_AD2 / TM2 / INT0 / EBI_AD13
E3	I/O	PL.13 / EPWM0_SYNC_OUT / UART7_nRTS / ECAP1_IC1 / UART14_TXD / SPI0_CLK / I2S1_BCLK / SC1_DAT / EBI_AD1 / HSUSBH_OVC / I2C2_SCL / TM0_EXT / EPWM0_CH3 / EBI_AD12 / RGMII1_PPS / RMII1_PPS
E4	I/O	PF.15 / HSUSB0_VBUSVLD
E7	O	RTC_RPWR
E8	I/O	PH.9 / CLK_32KOUT / TAMPER1
E9	I/O	PH.8 / TAMPER0
E10	P	V_{DDIO9}
E11	P	V_{DDIO8}
E12	P	AV_{DDL_PLL2}
E15	P	V_{SS}
E16	P	V_{SS}
E17	I/O	PC.7 / CAN1_TXD / SD0_WP
E18	I/O	PC.2 / CAN0_RXD / SD0_DAT0/eMMC0_DAT0

Pin	Type	MA35D16A887C (BGA 312-Ball, MCP with 256 Mbytes DDR3L) Pin Function
F1	P	V_{SS}
F2	P	V_{SS}
F3	I/O	PL.15 / EPWM0_CH1 / UART7_TXD / TRACE_CLK / CAN1_TXD / SPI0_MISO / I2S1_DO / SC1_PWR / EBI_AD3 / TM2_EXT / INT2 / EBI_AD14
F4	I/O	PA.3 / UART1_TXD / NAND_DATA3 / EBI_AD3 / EBI_ADR3
F6	P	V_{DD_HSUSB1}
F7	P	V_{BAT}
F8	P	AV_{DD}
F9	I	V_{REF_EADC0}
F10	P	AV_{DDH_PLL2}
F11	P	AV_{DDL_PLL1}
F12	P	V_{DD_PLL1}
F13	P	V_{DDIO7}
F15	I/O	PD.15 / EPWM0_SYNC_OUT / UART11_nRTS / CAN3_TXD / TRACE_DATA3 / EBI_ALE / EBI_AD7 / ECAP0_IC2 / TM6_EXT / I2S1_DO
F16	I/O	PI.6 / EPWM0_BRAKE0 / UART14_RXD / CAN1_RXD / I2S1_DI / EBI_ADR6 / QEI1_INDEX / INT2
F17	I/O	PC.6 / CAN1_RXD / SD0_nCD
F18	I/O	PC.0 / I2C4_SDA / SD0_CMD/eMMC0_CMD
G1	I	X32_IN
G2	O	X32_OUT
G3	I/O	PA.0 / UART1_nCTS / UART16_RXD / NAND_DATA0 / EBI_AD0 / EBI_ADR0
G4	I/O	PA.5 / UART3_nRTS / UART2_TXD / NAND_DATA5 / EBI_AD5 / EBI_ADR5
G5	I	RTC_nRWAKE
G6	P	V_{DD_OTP}
G7	P	V_{DD_HSUSB0}
G8	P	AV_{DD_ADC0}
G9	P	AV_{DD_EADC0}
G10	P	AV_{DDH_PLL1}
G11	P	AV_{DDL_PLL0}
G12	P	V_{DDIO10}
G13	P	V_{DDIO6}
G14	I/O	PD.13 / EPWM0_BRAKE1 / UART11_RXD / UART10_TXD / I2C4_SCL / TRACE_DATA1 / EBI_nCS2 / EBI_AD5 / ECAP0_IC0 / TM5_EXT / I2S1_BCLK
G15	I/O	PA.15 / EPWM0_CH2 / UART9_nCTS / UART6_RXD / I2C4_SDA / CAN2_RXD / EBI_ALE / QEI0_A / TM1 / RGMII0_PPS / RMII0_PPS **Note:** This pin is dedicated as PMIC_nIRQ input function from external PMIC by default.

Pin	Type	MA35D16A887C (BGA 312-Ball, MCP with 256 Mbytes DDR3L) Pin Function
G16	I/O	PK.1 / EPWM0_SYNC_OUT / UART16_nRTS / UART15_TXD / I2C4_SCL / EADC0_ST / EBI_ADR9 / TM7_EXT / ECAP0_IC2
G17	I/O	PC.5 / I2C5_SCL / SD0_DAT3/eMMC0_DAT3
G18	I/O	PC.3 / CAN0_TXD / SD0_DAT1/eMMC0_DAT1
H1	A	HSUSB1_D+
H2	A	HSUSB1_D-
H3	I/O	PA.1 / UART1_nRTS / UART16_TXD / NAND_DATA1 / EBI_AD1 / EBI_ADR1
H4	I/O	PA.7 / UART3_TXD / NAND_DATA7 / EBI_AD7 / EBI_ADR7
H5	I	nRESET / WDT_nRST
H6	P	V_{DD_CORE}
H7	P	AV_{DDL_ROSC}
H8	P	V_{DD_CORE}
H9	P	AV_{SS}
H10	P	AV_{SS_PLL}
H11	P	V_{SS}
H12	P	V_{DD_CORE}
H13	P	MV_{DD}
H14	P	MV_{REF}
H15	I/O	PI.1 / EPWM0_CH1 / UART12_nRTS / UART11_TXD / I2C2_SCL / SPI3_CLK / SC0_CLK / EBI_ADR1 / TM0_EXT / ECAP1_IC1
H16	I/O	PK.0 / EPWM0_SYNC_IN / UART16_nCTS / UART15_RXD / I2C4_SDA / I2S1_MCLK / EBI_ADR8 / TM7 / ECAP0_IC1
H17	I/O	PL.6 / EPWM0_CH0 / UART2_RXD / CAN0_RXD / QSPI1_MOSI1 / TRACE_CLK / EBI_AD5 / TM3 / ECAP1_IC0 / INT0
H18	I/O	PC.4 / I2C5_SDA / SD0_DAT2/eMMC0_DAT2
J1	A	HSUSB0_D+
J2	A	HSUSB0_D-
J3	I/O	PA.6 / UART3_RXD / NAND_DATA6 / EBI_AD6 / EBI_ADR6
J4	I/O	PA.8 / UART5_nCTS / UART4_RXD / NAND_RDY0 / EBI_AD8 / EBI_ADR8
J5	I	HSUSB0_ID
J6	P	V_{DD_CORE}
J7	P	V_{DD_CORE}
J8	P	V_{SS}
J9	P	V_{SS}
J10	P	V_{SS}

Pin	Type	MA35D16A887C (BGA 312-Ball, MCP with 256 Mbytes DDR3L) Pin Function
J11	P	V_{SS}
J12	P	V_{DD_CORE}
J13	P	MV_{DD}
J14	P	MZQ_DDRPHY
J15	I/O	PI.2 / EPWM0_CH2 / UART12_RXD / CAN0_RXD / SPI3_MOSI / SC0_DAT / EBI_ADR2 / TM1 / ECAP1_IC2
J16	I/O	PK.3 / EPWM1_CH1 / UART16_TXD / CAN2_TXD / SPI3_SS1 / SC1_nCD / EBI_ADR11 / QEI0_B
J17	I/O	PL.7 / EPWM0_CH1 / UART2_TXD / CAN0_TXD / QSPI1_MISO1 / EBI_AD6 / TM3_EXT / ECAP1_IC1 / INT1
J18	I/O	PL.5 / EPWM1_CH5 / UART2_nRTS / UART1_TXD / I2C4_SCL / SPI3_MISO / QSPI1_MISO0 / I2S1_MCLK / EBI_nWR / SC0_nCD / TM9_EXT / ECAP0_IC2
K1	I/O	PA.2 / UART1_RXD / NAND_DATA2 / EBI_AD2 / EBI_ADR2
K2	I/O	PA.4 / UART3_nCTS / UART2_RXD / NAND_DATA4 / EBI_AD4 / EBI_ADR4
K3	I/O	PA.9 / UART5_nRTS / UART4_TXD / NAND_nRE / EBI_AD9 / EBI_ADR9
K4	I/O	PA.12 / UART7_nCTS / UART8_RXD / NAND_ALE / EBI_AD12 / EBI_ADR12
K5	I/O	PA.10 / UART5_RXD / NAND_nWE / EBI_AD10 / EBI_ADR10
K6	P	V_{DD_CORE}
K7	P	V_{DD_CORE}
K8	P	V_{SS}
K9	P	V_{SS}
K10	P	V_{SS}
K11	P	V_{SS}
K12	P	V_{DD_CORE}
K13	P	MV_{DD}
K14	P	MZQ_SDRAM
K15	I/O	PI.0 / EPWM0_CH0 / UART12_nCTS / UART11_RXD / I2C2_SDA / SPI3_SS0 / SC0_nCD / EBI_ADR0 / TM0 / ECAP1_IC0
K16	I/O	PK.2 / EPWM1_CH0 / UART16_RXD / CAN2_RXD / SPI3_I2SMCLK / SC0_PWR / EBI_ADR10 / QEI0_A
K17	I/O	PL.8 / EPWM0_CH2 / UART14_nCTS / UART13_RXD / I2C5_SDA / SPI3_SS0 / EPWM0_CH4 / I2S1_LRCK / EBI_AD7 / SC0_CLK / TM4 / ECAP1_IC2 / INT2
K18	I/O	PL.4 / EPWM1_CH4 / UART2_nCTS / UART1_RXD / I2C4_SDA / SPI3_MOSI / QSPI1_MOSI0 / I2S0_MCLK / EBI_nRD / SC1_nCD / TM9 / ECAP0_IC1
L1	I/O	PA.13 / UART7_nRTS / UART8_TXD / NAND_nCS0 / EBI_AD13 / EBI_ADR13
L2	I/O	PA.11 / UART5_TXD / NAND_CLE / EBI_AD11 / EBI_ADR11
L3	I/O	PG.2 / EPWM0_CH4 / UART9_RXD / CAN0_RXD / SPI0_SS1 / EBI_ADR16 / EBI_nCS2 / QEI0_A / TM3 / INT1

Pin	Type	MA35D16A887C (BGA 312-Ball, MCP with 256 Mbytes DDR3L) Pin Function
L4	I/O	PG.4 / EPWM1_CH0 / UART5_nCTS / UART6_RXD / SPI3_SS0 / QEI1_INDEX / EBI_ADR18 / EBI_nCS0 / I2S1_DO / SC1_CLK / TM4 / INT2 / ECAP1_IC2
L5	I/O	PG.6 / EPWM1_CH2 / UART5_RXD / CAN1_RXD / SPI3_MOSI / ECAP0_IC1 / EBI_nRD / I2S1_BCLK / SC1_RST / TM7 / INT3
L6	P	V_{DDIO0}
L7	P	V_{DD_CPU}
L8	P	V_{SS}
L9	P	V_{SS}
L10	P	V_{SS}
L11	P	V_{SS}
L12	P	V_{DD_CORE}
L13	P	MV_{DD}
L14	I/O	PD.14 / EPWM0_SYNC_IN / UART11_nCTS / CAN3_RXD / TRACE_DATA2 / EBI_MCLK / EBI_AD6 / ECAP0_IC1 / TM6 / I2S1_DI / INT3
L15	I/O	PI.3 / EPWM0_CH3 / UART12_TXD / CAN0_TXD / SPI3_MISO / SC0_RST / EBI_ADR3 / TM1_EXT
L16	I/O	PJ.12 / EPWM1_CH2 / UART2_nCTS / UART1_RXD / I2C5_SDA / SPI3_SS0 / SC1_CLK / EBI_ADR12 / TM2 / QEI0_INDEX
L17	I/O	PL.9 / EPWM0_CH3 / UART14_nRTS / UART13_TXD / I2C5_SCL / SPI3_CLK / EPWM1_CH4 / I2S1_BCLK / EBI_AD8 / SC0_DAT / TM4_EXT / QEI0_A / INT3
L18	I/O	PL.3 / EPWM1_CH3 / UART11_TXD / CAN3_TXD / SPI2_CLK / QSPI1_CLK / I2S0_DO / EBI_AD14 / SC1_PWR / TM7_EXT / ECAP0_IC0
M1	I/O	PG.1 / EPWM0_CH3 / UART9_nRTS / UART6_TXD / I2C4_SCL / CAN2_TXD / EBI_nCS0 / QEI0_B / TM1_EXT / RGMII1_PPS / RMII1_PPS
M2	I/O	PG.0 / EPWM0_CH0 / UART7_TXD / CAN3_TXD / SPI0_SS0 / EADC0_ST / EBI_AD15 / I2S1_MCLK / QEI0_INDEX / TM1 / CLKO / INT0 / EBI_ADR15
M3	I/O	PG.5 / EPWM1_CH1 / UART5_nRTS / UART6_TXD / SPI3_CLK / ECAP0_IC0 / EBI_ADR19 / EBI_ALE / I2S1_DI / SC1_DAT / TM4_EXT
M4	I/O	PG.3 / EPWM0_CH5 / UART9_TXD / CAN0_TXD / SPI0_I2SMCLK / EBI_ADR17 / EBI_nCS1 / EBI_MCLK / QEI0_B / TM3_EXT / I2S1_MCLK
M5	I/O	PA.14 / UART7_RXD / CAN3_RXD / NAND_nWP / EBI_AD14 / EBI_ADR14
M6	P	V_{DDIO1}
M7	P	V_{DD_CPU}
M8	P	V_{SS}
M9	P	V_{SS}
M10	P	V_{SS}
M11	P	V_{SS}
M12	P	$MV_{DD\_DPHYPLL}$
M13	P	V_{DDIO5}

Pin	Type	MA35D16A887C (BGA 312-Ball, MCP with 256 Mbytes DDR3L) Pin Function
M14	I/O	PD.12 / EPWM0_BRAKE0 / UART11_TXD / UART10_RXD / I2C4_SDA / TRACE_DATA0 / EBI_nCS1 / EBI_AD4 / QEI0_INDEX / TM5 / I2S1_LRCK / INT1
M15	I/O	PI.5 / EPWM0_CH5 / UART14_nRTS / UART13_TXD / I2C3_SCL / I2S1_BCLK / EBI_ADR5 / INT1
M16	I/O	PJ.13 / EPWM1_CH3 / UART2_nRTS / UART1_TXD / I2C5_SCL / SPI3_MOSI / SC1_DAT / EBI_ADR13 / TM2_EXT
M17	I/O	PL.10 / EPWM0_CH4 / UART14_RXD / CAN3_RXD / SPI3_MOSI / EPWM0_CH5 / I2S1_DI / EBI_AD9 / SC0_RST / EBI_nWRH / QEI0_B
M18	I/O	PL.0 / EPWM1_CH0 / UART11_nCTS / UART10_RXD / I2C3_SDA / SPI2_MOSI / QSPI1_MOSI1 / I2S0_LRCK / EBI_AD11 / SC1_CLK / TM5 / QEI1_A
N1	I/O	PM.13 / EPWM1_CH5 / UART10_nRTS / TRACE_DATA1 / UART11_TXD / I2C2_SCL / EBI_AD9 / ECAP1_IC0 / TM8_EXT
N2	I/O	PM.14 / EPWM1_BRAKE0 / UART10_RXD / TRACE_DATA2 / CAN2_RXD / I2C3_SDA / EBI_AD10 / ECAP1_IC1 / TM10 / INT1
N3	I/O	PM.12 / EPWM1_CH4 / UART10_nCTS / TRACE_DATA0 / UART11_RXD / I2C2_SDA / SC1_nCD / EBI_AD8 / I2S1_MCLK / TM8
N4	I/O	PG.7 / EPWM1_CH3 / UART5_TXD / CAN1_TXD / SPI3_MISO / ECAP0_IC2 / EBI_nWR / I2S1_LRCK / SC1_PWR / TM7_EXT
N6	P	V_{DDIO2}
N7	P	V_{DD_CPU}
N8	P	V_{DD_CPU}
N9	P	V_{DD_CORE}
N10	P	V_{DD_CORE}
N11	P	V_{DD_CORE}
N12	P	V_{DDIO3}
N13	P	V_{DDIO4}
N15	I/O	PI.4 / EPWM0_CH4 / UART14_nCTS / UART13_RXD / I2C3_SDA / SPI2_SS1 / I2S1_LRCK / EBI_ADR4 / INT0
N16	I/O	PJ.15 / EPWM1_CH5 / UART2_TXD / CAN3_TXD / SPI3_CLK / EADC0_ST / SC1_PWR / EBI_ADR15 / TM3_EXT / INT1
N17	I/O	PL.11 / EPWM0_CH5 / UART14_TXD / CAN3_TXD / SPI3_MISO / EPWM1_CH5 / I2S1_DO / EBI_AD10 / SC0_PWR / EBI_nWRL / QEI0_INDEX
N18	I/O	PL.1 / EPWM1_CH1 / UART11_nRTS / UART10_TXD / I2C3_SCL / SPI2_MISO / QSPI1_MISO1 / I2S0_BCLK / EBI_AD12 / SC1_DAT / TM5_EXT / QEI1_B
P1	I/O	PM.15 / EPWM1_BRAKE1 / UART10_TXD / TRACE_DATA3 / CAN2_TXD / I2C3_SCL / EBI_AD11 / ECAP1_IC2 / TM10_EXT / INT2
P2	I/O	PG.12 / JTAG_TCK/SW_CLK / I2S0_LRCK / EBI_nWRL / EBI_AD1
P3	I/O	PG.15 / JTAG_nTRST / I2S0_DO / EBI_nCS0 / EBI_AD4
P4	I/O	PG.11 / JTAG_TDO / I2S0_MCLK / NAND_RDY1 / EBI_nWRH / EBI_nCS1 / EBI_AD0
P7	I/O	PM.1 / I2C4_SCL / SPI3_I2SMCLK / CCAP0_SFIELD / EBI_AD4 / EBI_ADR4
P8	I/O	PJ.5 / I2C3_SCL / SD1_nCD

Pin	Type	MA35D16A887C (BGA 312-Ball, MCP with 256 Mbytes DDR3L) Pin Function
P9	I/O	PJ.4 / I2C3_SDA / SD1_WP
P10	I/O	PK.5 / EPWM1_CH1 / UART12_nRTS / UART13_TXD / I2C4_SCL / SPI2_CLK / I2S1_DI / SC0_DAT / EADC0_ST / TM8_EXT / INT1
P11	I/O	PK.6 / EPWM1_CH2 / UART12_RXD / CAN0_RXD / SPI2_MOSI / I2S1_BCLK / SC0_RST / TM6 / INT2
P12	I/O	PK.7 / EPWM1_CH3 / UART12_TXD / CAN0_TXD / SPI2_MISO / I2S1_LRCK / SC0_PWR / CLKO / TM6_EXT / INT3
P15	I/O	PI.7 / EPWM0_BRAKE1 / UART14_TXD / CAN1_TXD / I2S1_DO / EBI_ADR7 / ECAP0_IC0 / INT3
P16	I/O	PJ.14 / EPWM1_CH4 / UART2_RXD / CAN3_RXD / SPI3_MISO / SC1_RST / EBI_ADR14 / TM3
P17	I/O	PK.8 / EPWM1_CH0 / I2C3_SDA / SPI3_CLK / EADC0_ST / EBI_AD15 / EBI_MCLK / EBI_ADR15 / TM8 / QEI1_INDEX
P18	I/O	PL.2 / EPWM1_CH2 / UART11_RXD / CAN3_RXD / SPI2_SS0 / QSPI1_SS1 / I2S0_DI / EBI_AD13 / SC1_RST / TM7 / QEI1_INDEX
R1	I/O	PG.14 / JTAG_TDI / I2S0_DI / NAND_nCS1 / EBI_ALE / EBI_AD3
R2	I/O	PG.13 / JTAG_TMS/SW_DIO / I2S0_BCLK / EBI_MCLK / EBI_AD2
R3	I/O	PD.7 / EPWM0_SYNC_OUT / UART1_TXD / QSPI1_MISO1 / I2C0_SCL / I2S1_MCLK / EPWM0_CH1 / EBI_AD6 / SC1_nCD / EADC0_ST **Note:** This pin is dedicated as I2C0_SCL function for controlling external PMIC by default.
R4	P	V_{SS}
R5	I/O	PM.11 / EPWM1_CH3 / CAN2_TXD / SPI3_SS1 / CCAP0_DATA9 / SPI2_SS1 / EBI_AD14 / EBI_ADR14
R6	I/O	PM.9 / I2C0_SCL / CCAP0_DATA7 / EBI_AD12 / EBI_ADR12
R7	I/O	PJ.1 / EPWM1_BRAKE1 / UART8_nRTS / UART7_TXD / I2C2_SCL / SPI2_CLK / eMMC1_DAT5 / I2S0_BCLK / SC0_DAT / EBI_AD12 / EBI_ADR17 / EBI_nCS1 / EBI_AD8
R8	I/O	PJ.3 / EPWM1_CH5 / UART8_TXD / CAN1_TXD / SPI2_MISO / eMMC1_DAT7 / I2S0_DO / SC0_PWR / EBI_AD14 / EBI_ADR19 / EBI_nWRL / EBI_AD10
R9	I/O	PJ.9 / I2C4_SCL / SD1_DAT1/eMMC1_DAT1
R10	I/O	PK.4 / UART12_nCTS / UART13_RXD / SPI2_MISO / LCM_DEN/LCM_MPU_RS / EBI_AD10 / EBI_nWRL
R11	I/O	PI.9 / UART4_nRTS / UART3_TXD / LCM_DATA1/LCM_MPU_D1 / EBI_AD12
R12	I/O	PI.14 / UART6_RXD / LCM_DATA6/LCM_MPU_D6
R13	I/O	PH.3 / UART8_TXD / LCM_DATA11/LCM_MPU_D11
R14	I/O	PH.7 / UART10_TXD / LCM_DATA15/LCM_MPU_D15
R15	P	V_{SS}
R16	I/O	PC.14 / UART12_RXD / LCM_DATA18/LCM_MPU_CS
R17	I/O	PH.12 / UART14_nCTS / UART13_RXD / LCM_DATA20
R18	I/O	PH.14 / UART14_RXD / LCM_DATA22
T1	I/O	PE.14 / UART0_TXD
T2	I/O	PE.15 / UART0_RXD

Pin	Type	MA35D16A887C (BGA 312-Ball, MCP with 256 Mbytes DDR3L) Pin Function
T3	I/O	PD.11 / EPWM1_BRAKE1 / UART16_TXD / QSPI1_MISO0 / I2S1_DO / EPWM0_CH5 / EBI_AD10 / SC1_PWR / TM2_EXT
T4	I/O	PK.11 / CAN1_TXD / CCAP0_HSYNC / EBI_AD2 / EBI_ADR2
T5	I/O	PM.3 / CAN3_TXD / CCAP0_DATA1 / EBI_AD6 / EBI_ADR6
T6	I/O	PM.7 / CAN0_TXD / CCAP0_DATA5 / EBI_AD10 / EBI_ADR10
T7	I/O	PM.8 / I2C0_SDA / CCAP0_DATA6 / EBI_AD11 / EBI_ADR11
T8	I/O	PJ.2 / EPWM1_CH4 / UART8_RXD / CAN1_RXD / SPI2_MOSI / eMMC1_DAT6 / I2S0_DI / SC0_RST / EBI_AD13 / EBI_ADR18 / EBI_nWRH / EBI_AD9
T9	I/O	PJ.6 / CAN3_RXD / SD1_CMD/eMMC1_CMD
T10	I/O	PG.8 / EPWM1_CH4 / UART12_RXD / CAN3_RXD / SPI2_SS0 / LCM_VSYNC/LCM_MPU_RD/EN / I2C3_SDA / EBI_AD7 / EBI_nCS0
T11	I/O	PI.8 / UART4_nCTS / UART3_RXD / LCM_DATA0/LCM_MPU_D0 / EBI_AD11
T12	I/O	PI.13 / UART6_nRTS / UART5_TXD / LCM_DATA5/LCM_MPU_D5
T13	I/O	PH.2 / UART8_RXD / LCM_DATA10/LCM_MPU_D10
T14	I/O	PH.6 / UART10_RXD / LCM_DATA14/LCM_MPU_D14
T15	I/O	PD.5 / UART1_nRTS / UART2_TXD / I2C2_SCL / QSPI0_MISO1
T16	I/O	PC.12 / UART12_nCTS / UART11_RXD / LCM_DATA16/LCM_MPU_D16
T17	I/O	PC.13 / UART12_nRTS / UART11_TXD / LCM_DATA17/LCM_MPU_D17
T18	I/O	PH.15 / UART14_TXD / LCM_DATA23
U1	I/O	PD.6 / EPWM0_SYNC_IN / UART1_RXD / QSPI1_MOSI1 / I2C0_SDA / I2S0_MCLK / EPWM0_CH0 / EBI_AD5 / SPI3_SS1 / TRACE_CLK **Note:** This pin is dedicated as I2C0_SDA function for controlling external PMIC by default.
U2	I/O	PD.8 / EPWM0_BRAKE0 / UART16_nCTS / UART15_RXD / QSPI1_SS0 / I2S1_LRCK / EPWM0_CH2 / EBI_AD7 / SC1_CLK / TM0
U3	I/O	PD.10 / EPWM1_BRAKE0 / UART16_RXD / QSPI1_MOSI0 / I2S1_DI / EPWM0_CH4 / EBI_AD9 / SC1_RST / TM2
U4	I/O	PM.0 / I2C4_SDA / CCAP0_VSYNC / EBI_AD3 / EBI_ADR3
U5	I/O	PM.4 / I2C5_SDA / CCAP0_DATA2 / EBI_AD7 / EBI_ADR7
U6	I/O	PM.5 / I2C5_SCL / CCAP0_DATA3 / EBI_AD8 / EBI_ADR8
U7	I/O	PM.10 / EPWM1_CH2 / CAN2_RXD / SPI3_SS0 / CCAP0_DATA8 / SPI2_I2SMCLK / EBI_AD13 / EBI_ADR13
U8	I/O	PJ.11 / CAN0_TXD / SD1_DAT3/eMMC1_DAT3
U9	I/O	PJ.8 / I2C4_SDA / SD1_DAT0/eMMC1_DAT0
U10	I/O	PG.9 / EPWM1_CH5 / UART12_TXD / CAN3_TXD / SPI2_CLK / LCM_HSYNC/LCM_MPU_WR/RW / I2C3_SCL / EBI_AD8 / EBI_nCS1
U11	I/O	PI.15 / UART6_TXD / LCM_DATA7/LCM_MPU_D7
U12	I/O	PI.12 / UART6_nCTS / UART5_RXD / LCM_DATA4/LCM_MPU_D4
U13	I/O	PH.1 / UART8_nRTS / UART7_TXD / LCM_DATA9/LCM_MPU_D9

Pin	Type	MA35D16A887C (BGA 312-Ball, MCP with 256 Mbytes DDR3L) Pin Function
U14	I/O	PH.5 / UART10_nRTS / UART9_TXD / LCM_DATA13/LCM_MPU_D13
U15	I/O	PD.3 / UART3_TXD / QSPI0_MISO0
U16	I/O	PD.0 / UART3_nCTS / UART4_RXD / QSPI0_SS0
U17	I/O	PC.15 / UART12_TXD / LCM_DATA19 / LCM_MPU_TE / LCM_MPU_VSYNC
U18	I/O	PH.13 / UART14_nRTS / UART13_TXD / LCM_DATA21
V1	P	V_{SS}
V2	I/O	PD.9 / EPWM0_BRAKE1 / UART16_nRTS / UART15_TXD / QSPI1_CLK / I2S1_BCLK / EPWM0_CH3 / EBI_AD8 / SC1_DAT / TM0_EXT
V3	I/O	PK.9 / I2C3_SCL / CCAP0_SCLK / EBI_AD0 / EBI_ADR0
V4	I/O	PK.10 / CAN1_RXD / CCAP0_PIXCLK / EBI_AD1 / EBI_ADR1
V5	I/O	PM.2 / CAN3_RXD / CCAP0_DATA0 / EBI_AD5 / EBI_ADR5
V6	I/O	PM.6 / CAN0_RXD / CCAP0_DATA4 / EBI_AD9 / EBI_ADR9
V7	I/O	PJ.0 / EPWM1_BRAKE0 / UART8_nCTS / UART7_RXD / I2C2_SDA / SPI2_SS0 / eMMC1_DAT4 / I2S0_LRCK / SC0_CLK / EBI_AD11 / EBI_ADR16 / EBI_nCS0 / EBI_AD7
V8	I/O	PJ.7 / CAN3_TXD / SD1_CLK/eMMC1_CLK
V9	I/O	PJ.10 / CAN0_RXD / SD1_DAT2/eMMC1_DAT2
V10	I/O	PG.10 / UART12_nRTS / UART13_TXD / SPI2_MOSI / LCM_CLK / EBI_AD9 / EBI_nWRH
V11	I/O	PI.10 / UART4_RXD / LCM_DATA2/LCM_MPU_D2 / EBI_AD13
V12	I/O	PI.11 / UART4_TXD / LCM_DATA3/LCM_MPU_D3 / EBI_AD14
V13	I/O	PH.0 / UART8_nCTS / UART7_RXD / LCM_DATA8/LCM_MPU_D8
V14	I/O	PH.4 / UART10_nCTS / UART9_RXD / LCM_DATA12/LCM_MPU_D12
V15	I/O	PD.4 / UART1_nCTS / UART2_RXD / I2C2_SDA / QSPI0_MOSI1
V16	I/O	PD.2 / UART3_RXD / QSPI0_MOSI0
V17	I/O	PD.1 / UART3_nRTS / UART4_TXD / QSPI0_CLK
V18	P	V_{SS}

4.2.3 MA35D1 Series BGA 364-Ball Pinout Function Table

Pin	Type	MA35D16A087C (BGA 364-Ball, non-MCP) Pin Function
A1	P	V_{SS}
A2	A	EADC0_CH3
A3	I/O	PF.11 / UART13_nRTS / I2S0_BCLK / SPI1_CLK / RGMII1_TXCLK / SC0_DAT / KPI_COL7
A4	I/O	PF.10 / UART13_nCTS / I2S0_LRCK / SPI1_SS0 / RGMII1_RXD3 / SC0_CLK / KPI_COL6
A5	I/O	PF.5 / UART11_nRTS / UART10_TXD / I2S0_BCLK / SPI1_CLK / RGMII1_RXCLK / RMII1_REFCLK / CAN2_TXD / KPI_ROW1
A6	I/O	PF.3 / UART2_TXD / RGMII0_TXD3 / RGMII1_TXD0 / RMII1_TXD0 / KPI_COL3
A7	I/O	PF.1 / UART2_nRTS / UART1_TXD / RGMII0_TXCLK / RGMII1_MDIO / RMII1_MDIO / KPI_COL1
A8	I/O	PE.11 / UART15_nRTS / UART14_TXD / SPI1_CLK / CCAP1_VSYNC / RGMII0_TXCLK
A9	I/O	PE.9 / UART13_nRTS / UART12_TXD / CCAP1_PIXCLK / RGMII0_RXD2 / RMII0_RXERR
A10	I/O	PE.5 / UART4_nRTS / UART3_TXD / CCAP1_DATA5 / RGMII0_RXCLK / RMII0_REFCLK
A11	I/O	PE.3 / UART9_TXD / CCAP1_DATA3 / RGMII0_TXD0 / RMII0_TXD0
A12	I/O	PN.7 / CAN1_TXD / CCAP1_DATA7
A13	I/O	PN.1 / I2C2_SCL / CCAP1_DATA1
A14	I/O	PN.11 / CAN2_TXD / CCAP1_PIXCLK
A15	I	XT1_IN
A16	I/O	PN.6 / CAN1_RXD / CCAP1_DATA6
A17	I/O	PN.2 / CAN0_RXD / CCAP1_DATA2
A18	I/O	PN.13 / UART6_nRTS / UART12_TXD / I2C5_SCL / CCAP1_VSYNC
A19	I/O	PC.1 / I2C4_SCL / SD0_CLK/eMMC0_CLK
A20	P	V_{SS}
B1	A	EADC0_CH7
B2	A	EADC0_CH6
B3	A	EADC0_CH2
B4	I/O	PF.13 / I2S0_DO / SPI1_MISO / RGMII1_TXD3 / SC0_PWR / KPI_ROW5
B5	I/O	PF.14 / EPWM2_BRAKE0 / EADC0_ST / RGMII1_PPS / RMII1_PPS / SPI0_I2SMCLK / SPI1_I2SMCLK / CCAP1_SFIELD / RGMII0_PPS / RMII0_PPS / TM0 / INT0 / SPI1_SS1 / QEI2_INDEX / I2S0_MCLK
B6	I/O	PF.12 / I2S0_DI / SPI1_MOSI / RGMII1_TXD2 / SC0_RST / KPI_ROW4
B7	I/O	PF.9 / UART13_TXD / I2C5_SCL / SPI0_SS1 / RGMII1_RXD2 / RMII1_RXERR / SC0_PWR / KPI_COL5
B8	I/O	PF.7 / UART11_TXD / I2S0_DO / SPI1_MISO / RGMII1_RXD0 / RMII1_RXD0 / I2C4_SCL / SC0_DAT / KPI_ROW3
B9	I/O	PE.13 / UART15_TXD / SPI1_MISO / CCAP1_DATA9 / RGMII0_TXD3
B10	I/O	PE.7 / UART4_TXD / CCAP1_DATA7 / RGMII0_RXD0 / RMII0_RXD0

Pin	Type	MA35D16A087C (BGA 364-Ball, non-MCP) Pin Function
B11	I/O	PE.8 / UART13_nCTS / UART12_RXD / CCAP1_SCLK / RGMII0_RXD1 / RMII0_RXD1
B12	I/O	PE.1 / UART9_nRTS / UART8_TXD / CCAP1_DATA1 / RGMII0_MDIO / RMII0_MDIO
B13	I/O	PK.15 / EPWM2_CH3 / UART1_TXD / CAN3_TXD / I2S0_DO / SPI1_MISO / SC0_PWR / I2C5_SCL / TM11_EXT
B14	I/O	PN.12 / UART6_nCTS / UART12_RXD / I2C5_SDA / CCAP1_HSYNC
B15	O	XT1_OUT
B16	I/O	PN.4 / I2C1_SDA / CCAP1_DATA4
B17	I/O	PN.0 / I2C2_SDA / CCAP1_DATA0
B18	I/O	PC.2 / CAN0_RXD / SD0_DAT0/eMMC0_DAT0
B19	I/O	PC.5 / I2C5_SCL / SD0_DAT3/eMMC0_DAT3
B20	I/O	PC.3 / CAN0_TXD / SD0_DAT1/eMMC0_DAT1
C1	I/O	PB.15 / EPWM2_CH3 / UART4_TXD / CAN1_TXD / I2C4_SCL / I2S1_DO / ADC0_CH7 / EBI_ADR19
C2	I/O	PB.12 / EPWM2_CH0 / UART4_nCTS / UART3_RXD / I2C3_SDA / CAN2_RXD / I2S1_LRCK / ADC0_CH4 / EBI_ADR16 / ECAP2_IC0
C3	I/O	PB.9 / EPWM2_CH4 / UART2_nRTS / UART1_TXD / I2C2_SCL / SPI0_CLK / I2S0_MCLK / CCAP1_HSYNC / ADC0_CH1 / EBI_ALE / EBI_AD13 / TM0_EXT / I2S1_MCLK / SC0_nCD / QEI2_A / KPI_ROW7
C4	I/O	PB.11 / EPWM2_BRAKE1 / UART2_TXD / CAN0_TXD / SPI0_MISO / I2S1_MCLK / CCAP1_SFIELD / ADC0_CH3 / EBI_nCS2 / EBI_ALE / TM5_EXT / I2C1_SCL / INT2 / QEI2_INDEX
C5	A	EADC0_CH5
C6	A	EADC0_CH1
C7	I/O	PF.8 / UART13_RXD / I2C5_SDA / SPI0_SS0 / RGMII1_RXD1 / RMII1_RXD1 / SC0_RST / KPI_COL4
C8	I/O	PF.6 / UART11_RXD / I2S0_DI / SPI1_MOSI / RGMII1_RXCTL / RMII1_CRSDV / I2C4_SDA / SC0_CLK / KPI_ROW2
C9	I/O	PF.4 / UART11_nCTS / UART10_RXD / I2S0_LRCK / SPI1_SS0 / RGMII1_TXD1 / RMII1_TXD1 / CAN2_RXD / KPI_ROW0
C10	I/O	PF.2 / UART2_RXD / RGMII0_TXD2 / RGMII1_TXCTL / RMII1_TXEN / KPI_COL2
C11	I/O	PE.10 / UART15_nCTS / UART14_RXD / SPI1_SS0 / CCAP1_HSYNC / RGMII0_RXD3
C12	I/O	PE.2 / UART9_RXD / CCAP1_DATA2 / RGMII0_TXCTL / RMII0_TXEN
C13	I/O	PK.14 / EPWM2_CH2 / UART1_RXD / CAN3_RXD / I2S0_DI / SPI1_MOSI / SC0_RST / I2C5_SDA / TM11 / INT3
C14	I/O	PN.10 / CAN2_RXD / CCAP1_SCLK
C15	I/O	PN.5 / I2C1_SCL / CCAP1_DATA5
C16	P	V_{SS}
C17	P	V_{SS}
C18	I/O	PC.0 / I2C4_SDA / SD0_CMD/eMMC0_CMD
C19	P	V_{SS}

Pin	Type	MA35D16A087C (BGA 364-Ball, non-MCP) Pin Function
C20	I/O	MD14
D1	P	V_{SS}
D2	P	V_{SS}
D3	I/O	PL.12 / EPWM0_SYNC_IN / UART7_nCTS / ECAP1_IC0 / UART14_RXD / SPI0_SS0 / I2S1_LRCK / SC1_CLK / EBI_AD0 / HSUSBH_PWREN / I2C2_SDA / TM0 / EPWM0_CH2 / EBI_AD11 / RGMII0_PPS / RMII0_PPS
D4	I/O	PB.14 / EPWM2_CH2 / UART4_RXD / CAN1_RXD / I2C4_SDA / I2S1_DI / ADC0_CH6 / EBI_ADR18 / ECAP2_IC2
D5	I/O	PB.13 / EPWM2_CH1 / UART4_nRTS / UART3_TXD / I2C3_SCL / CAN2_TXD / I2S1_BCLK / ADC0_CH5 / EBI_ADR17 / ECAP2_IC1
D6	I/O	PF.15 / HSUSB0_VBUSVLD
D7	I/O	PL.15 / EPWM0_CH1 / UART7_TXD / TRACE_CLK / CAN1_TXD / SPI0_MISO / I2S1_DO / SC1_PWR / EBI_AD3 / TM2_EXT / INT2 / EBI_AD14
D8	I/O	PF.0 / UART2_nCTS / UART1_RXD / RGMII0_RXD3 / RGMII1_MDC / RMII1_MDC / KPI_COL0
D9	I/O	PE.6 / UART4_RXD / CCAP1_DATA6 / RGMII0_RXCTL / RMII0_CRSDV
D10	I/O	PE.12 / UART15_RXD / SPI1_MOSI / CCAP1_DATA8 / RGMII0_TXD2
D11	I/O	PE.4 / UART4_nCTS / UART3_RXD / CCAP1_DATA4 / RGMII0_TXD1 / RMII0_TXD1
D12	I/O	PE.0 / UART9_nCTS / UART8_RXD / CCAP1_DATA0 / RGMII0_MDC / RMII0_MDC
D13	P	V_{SS}
D14	I/O	PN.3 / CAN0_TXD / CCAP1_DATA3
D15	I/O	PC.4 / I2C5_SDA / SD0_DAT2/eMMC0_DAT2
D16	P	V_{SS}
D17	P	V_{SS}
D18	P	V_{SS}
D19	I/O	MD15
D20	I/O	MD12
E1	I	X32_IN
E2	O	X32_OUT
E3	O	RTC_RPWR
E4	I/O	PL.14 / EPWM0_CH2 / UART7_RXD / CAN1_RXD / SPI0_MOSI / I2S1_DI / SC1_RST / EBI_AD2 / TM2 / INT0 / EBI_AD13
E5	I/O	PH.9 / CLK_32KOUT / TAMPER1
E6	I/O	PL.13 / EPWM0_SYNC_OUT / UART7_nRTS / ECAP1_IC1 / UART14_TXD / SPI0_CLK / I2S1_BCLK / SC1_DAT / EBI_AD1 / HSUSBH_OVC / I2C2_SCL / TM0_EXT / EPWM0_CH3 / EBI_AD12 / RGMII1_PPS / RMII1_PPS
E7	I	nRESET / WDT_nRST
E8	I/O	PB.10 / EPWM2_CH5 / UART2_RXD / CAN0_RXD / SPI0_MOSI / EBI_MCLK / CCAP1_VSYNC / ADC0_CH2 / EBI_ADR15 / EBI_AD14 / TM5 / I2C1_SDA / INT1 / QEI2_B

Pin	Type	MA35D16A087C (BGA 364-Ball, non-MCP) Pin Function
E9	I/O	PB.8 / EPWM2_BRAKE0 / UART2_nCTS / UART1_RXD / I2C2_SDA / SPI0_SS1 / SPI0_I2SMCLK / ADC0_CH0 / EBI_nCS0 / TM4 / QEI2_INDEX / KPI_ROW6
E10	A	EADC0_CH4
E11	A	EADC0_CH0
E12	I/O	PN.14 / UART6_RXD / CAN3_RXD / SPI1_SS1 / CCAP1_SFIELD / SPI1_I2SMCLK
E13	I/O	PK.13 / EPWM2_CH1 / UART1_nRTS / UART13_TXD / I2C4_SCL / I2S0_BCLK / SPI1_CLK / SC0_DAT / TM10_EXT
E14	I/O	PN.15 / EPWM2_CH4 / UART6_TXD / CAN3_TXD / I2S0_MCLK / SPI1_SS1 / SPI1_I2SMCLK / SC0_nCD / EADC0_ST / CLKO / TM6
E15	I/O	PK.12 / EPWM2_CH0 / UART1_nCTS / UART13_RXD / I2C4_SDA / I2S0_LRCK / SPI1_SS0 / SC0_CLK / TM10 / INT2
E16	I/O	PC.7 / CAN1_TXD / SD0_WP
E17	O	MBA1
E18	O	MBA2
E19	I/O	MD13
E20	O	MDMask1
F1	A	HSUSB1_D+
F2	A	HSUSB1_D-
F3	I	HSUSB0_ID
F4	I	RTC_nRWAKE
F5	I/O	PH.8 / TAMPER0
F16	I/O	PC.6 / CAN1_RXD / SD0_nCD
F17	O	MA10
F18	O	MA5
F19	I/O	MDQS1_P
F20	I/O	MDQS1_N
G1	A	HSUSB0_D+
G2	A	HSUSB0_D-
G3	I/O	PA.0 / UART1_nCTS / UART16_RXD / NAND_DATA0 / EBI_AD0 / EBI_ADR0
G4	I/O	PA.5 / UART3_nRTS / UART2_TXD / NAND_DATA5 / EBI_AD5 / EBI_ADR5
G5	I/O	PA.1 / UART1_nRTS / UART16_TXD / NAND_DATA1 / EBI_AD1 / EBI_ADR1
G7	P	V_{DDIO8}
G8	P	V_{DD_HSUSB1}
G9	P	V_{BAT}
G10	I	V_{REF_EADC0}

Pin	Type	MA35D16A087C (BGA 364-Ball, non-MCP) Pin Function
G11	P	AV_{DDH_PLL2}
G12	P	AV_{DDL_PLL2}
G13	P	V_{DDIO7}
G14	P	V_{DDIO6}
G16	P	V_{SS}
G17	O	MA3
G18	O	MA12
G19	I/O	MD9
G20	I/O	MD10
H1	I/O	PA.2 / UART1_RXD / NAND_DATA2 / EBI_AD2 / EBI_ADR2
H2	I/O	PA.4 / UART3_nCTS / UART2_RXD / NAND_DATA4 / EBI_AD4 / EBI_ADR4
H3	I/O	PA.9 / UART5_nRTS / UART4_TXD / NAND_nRE / EBI_AD9 / EBI_ADR9
H4	I/O	PA.6 / UART3_RXD / NAND_DATA6 / EBI_AD6 / EBI_ADR6
H5	I/O	PA.3 / UART1_TXD / NAND_DATA3 / EBI_AD3 / EBI_ADR3
H7	P	V_{DDIO9}
H8	P	V_{DD_HSUSB0}
H9	P	AV_{DD}
H10	P	AV_{DD_EADC0}
H11	P	AV_{DDH_PLL1}
H12	P	AV_{DDL_PLL1}
H13	P	AV_{DDL_PLL0}
H14	P	V_{DD_PLL1}
H16	O	MCS1n
H17	O	MA0
H18	O	MA1
H19	I/O	MD11
H20	I/O	MD8
J1	I/O	PA.11 / UART5_TXD / NAND_CLE / EBI_AD11 / EBI_ADR11
J2	I/O	PA.7 / UART3_TXD / NAND_DATA7 / EBI_AD7 / EBI_ADR7
J3	I/O	PA.13 / UART7_nRTS / UART8_TXD / NAND_nCS0 / EBI_AD13 / EBI_ADR13
J4	I/O	PD.13 / EPWM0_BRAKE1 / UART11_RXD / UART10_TXD / I2C4_SCL / TRACE_DATA1 / EBI_nCS2 / EBI_AD5 / ECAP0_IC0 / TM5_EXT / I2S1_BCLK
J5	I/O	PA.8 / UART5_nCTS / UART4_RXD / NAND_RDY0 / EBI_AD8 / EBI_ADR8
J7	P	V_{DD_OTP}

Pin	Type	MA35D16A087C (BGA 364-Ball, non-MCP) Pin Function
J8	P	V_{DD_CORE}
J9	P	AV_{DD_ADC0}
J10	P	AV_{SS}
J11	P	AV_{SS_PLL}
J12	P	V_{SS}
J13	P	V_{DD_CORE}
J14	P	V_{DDIO10}
J16	O	MCKE1
J17	O	MBA0
J18	O	MCASn
J19	I/O	MDQS0_P
J20	I/O	MDQS0_N
K1	I/O	PG.0 / EPWM0_CH0 / UART7_TXD / CAN3_TXD / SPI0_SS0 / EADC0_ST / EBI_AD15 / I2S1_MCLK / QEI0_INDEX / TM1 / CLKO / INT0 / EBI_ADR15
K2	I/O	PD.15 / EPWM0_SYNC_OUT / UART11_nRTS / CAN3_TXD / TRACE_DATA3 / EBI_ALE / EBI_AD7 / ECAP0_IC2 / TM6_EXT / I2S1_DO
K3	I/O	PD.12 / EPWM0_BRAKE0 / UART11_TXD / UART10_RXD / I2C4_SDA / TRACE_DATA0 / EBI_nCS1 / EBI_AD4 / QEI0_INDEX / TM5 / I2S1_LRCK / INT1
K4	I/O	PA.12 / UART7_nCTS / UART8_RXD / NAND_ALE / EBI_AD12 / EBI_ADR12
K5	I/O	PA.10 / UART5_RXD / NAND_nWE / EBI_AD10 / EBI_ADR10
K7	P	V_{DD_CORE}
K8	P	AV_{DDL_ROSC}
K9	P	V_{SS}
K10	P	V_{SS}
K11	P	V_{SS}
K12	P	V_{SS}
K13	P	MV_{DD}
K14	P	$MV_{DD\_DPHYPLL}$
K16	O	MCKE0
K17	O	MRASn
K18	O	MWEn
K19	I/O	MD2
K20	I/O	MD3
L1	I/O	PG.1 / EPWM0_CH3 / UART9_nRTS / UART6_TXD / I2C4_SCL / CAN2_TXD / EBI_nCS0 / QEI0_B / TM1_EXT / RGMII1_PPS / RMII1_PPS

Pin	Type	MA35D16A087C (BGA 364-Ball, non-MCP) Pin Function
L2	I/O	PD.14 / EPWM0_SYNC_IN / UART11_nCTS / CAN3_RXD / TRACE_DATA2 / EBI_MCLK / EBI_AD6 / ECAP0_IC1 / TM6 / I2S1_DI / INT3
L3	I/O	PG.4 / EPWM1_CH0 / UART5_nCTS / UART6_RXD / SPI3_SS0 / QEI1_INDEX / EBI_ADR18 / EBI_nCS0 / I2S1_DO / SC1_CLK / TM4 / INT2 / ECAP1_IC2
L4	I/O	PG.2 / EPWM0_CH4 / UART9_RXD / CAN0_RXD / SPI0_SS1 / EBI_ADR16 / EBI_nCS2 / QEI0_A / TM3 / INT1
L5	I/O	PA.14 / UART7_RXD / CAN3_RXD / NAND_nWP / EBI_AD14 / EBI_ADR14
L7	P	V_{DD_CORE}
L8	P	V_{DD_CORE}
L9	P	V_{SS}
L10	P	V_{SS}
L11	P	V_{SS}
L12	P	V_{SS}
L13	P	MV_{DD}
L14	P	MV_{REF_DQ}
L16	O	MODT1
L17	O	MA2
L18	O	MA6
L19	I/O	MD1
L20	I/O	MD0
M1	I/O	PG.3 / EPWM0_CH5 / UART9_TXD / CAN0_TXD / SPI0_I2SMCLK / EBI_ADR17 / EBI_nCS1 / EBI_MCLK / QEI0_B / TM3_EXT / I2S1_MCLK
M2	I/O	PG.7 / EPWM1_CH3 / UART5_TXD / CAN1_TXD / SPI3_MISO / ECAP0_IC2 / EBI_nWR / I2S1_LRCK / SC1_PWR / TM7_EXT
M3	I/O	PM.12 / EPWM1_CH4 / UART10_nCTS / TRACE_DATA0 / UART11_RXD / I2C2_SDA / SC1_nCD / EBI_AD8 / I2S1_MCLK / TM8
M4	I/O	PG.6 / EPWM1_CH2 / UART5_RXD / CAN1_RXD / SPI3_MOSI / ECAP0_IC1 / EBI_nRD / I2S1_BCLK / SC1_RST / TM7 / INT3
M5	I/O	PA.15 / EPWM0_CH2 / UART9_nCTS / UART6_RXD / I2C4_SDA / CAN2_RXD / EBI_ALE / QEI0_A / TM1 / RGMII0_PPS / RMII0_PPS **Note:** This pin is dedicated as PMIC_nIRQ input function from external PMIC by default.
M7	P	V_{DD_CORE}
M8	P	V_{DD_CPU}
M9	P	V_{SS}
M10	P	V_{SS}
M11	P	V_{SS}
M12	P	V_{SS}
M13	P	MV_{DD}

Pin	Type	MA35D16A087C (BGA 364-Ball, non-MCP) Pin Function
M14	P	MV_{REF_CA}
M16	O	MODT0
M17	O	MA11
M18	O	MA4
M19	O	MCK_N
M20	O	MCK_P
N1	I/O	PG.5 / EPWM1_CH1 / UART5_nRTS / UART6_TXD / SPI3_CLK / ECAP0_IC0 / EBI_ADR19 / EBI_ALE / I2S1_DI / SC1_DAT / TM4_EXT
N2	I/O	PM.13 / EPWM1_CH5 / UART10_nRTS / TRACE_DATA1 / UART11_TXD / I2C2_SCL / EBI_AD9 / ECAP1_IC0 / TM8_EXT
N3	I/O	PG.13 / JTAG_TMS/SW_DIO / I2S0_BCLK / EBI_MCLK / EBI_AD2
N4	I/O	PG.11 / JTAG_TDO / I2S0_MCLK / NAND_RDY1 / EBI_nWRH / EBI_nCS1 / EBI_AD0
N5	I/O	PM.14 / EPWM1_BRAKE0 / UART10_RXD / TRACE_DATA2 / CAN2_RXD / I2C3_SDA / EBI_AD10 / ECAP1_IC1 / TM10 / INT1
N7	P	V_{DDIO0}
N8	P	V_{DD_CPU}
N9	P	V_{DD_CPU}
N10	P	V_{DD_CPU}
N11	P	V_{DD_CORE}
N12	P	V_{DD_CORE}
N13	P	MV_{DD}
N14	P	MZQ_DDRPHY
N16	O	MRESETn
N17	O	MA7
N18	O	MA9
N19	O	MDMask0
N20	I/O	MD6
P1	I/O	PM.15 / EPWM1_BRAKE1 / UART10_TXD / TRACE_DATA3 / CAN2_TXD / I2C3_SCL / EBI_AD11 / ECAP1_IC2 / TM10_EXT / INT2
P2	I/O	PG.14 / JTAG_TDI / I2S0_DI / NAND_nCS1 / EBI_ALE / EBI_AD3
P3	I/O	PI.3 / EPWM0_CH3 / UART12_TXD / CAN0_TXD / SPI3_MISO / SC0_RST / EBI_ADR3 / TM1_EXT
P4	I/O	PI.1 / EPWM0_CH1 / UART12_nRTS / UART11_TXD / I2C2_SCL / SPI3_CLK / SC0_CLK / EBI_ADR1 / TM0_EXT / ECAP1_IC1
P5	I/O	PG.15 / JTAG_nTRST / I2S0_DO / EBI_nCS0 / EBI_AD4
P7	P	V_{DDIO1}
P8	P	V_{DDIO2}

Pin	Type	MA35D16A087C (BGA 364-Ball, non-MCP) Pin Function
P9	P	V_{DD_CORE}
P10	P	V_{DD_CORE}
P11	P	V_{DD_CORE}
P12	P	V_{DDIO3}
P13	P	V_{DDIO4}
P14	P	V_{DDIO5}
P16	O	MCS0n
P17	O	MA15
P18	O	MA14
P19	I/O	MD7
P20	I/O	MD4
R1	I/O	PG.12 / JTAG_TCK/SW_CLK / I2S0_LRCK / EBI_nWRL / EBI_AD1
R2	I/O	PI.4 / EPWM0_CH4 / UART14_nCTS / UART13_RXD / I2C3_SDA / SPI2_SS1 / I2S1_LRCK / EBI_ADR4 / INT0
R3	I/O	PI.0 / EPWM0_CH0 / UART12_nCTS / UART11_RXD / I2C2_SDA / SPI3_SS0 / SC0_nCD / EBI_ADR0 / TM0 / ECAP1_IC0
R4	I/O	PK.1 / EPWM0_SYNC_OUT / UART16_nRTS / UART15_TXD / I2C4_SCL / EADC0_ST / EBI_ADR9 / TM7_EXT / ECAP0_IC2
R5	I/O	PK.3 / EPWM1_CH1 / UART16_TXD / CAN2_TXD / SPI3_SS1 / SC1_nCD / EBI_ADR11 / QEI0_B
R16	P	V_{SS}
R17	O	MA13
R18	O	MA8
R19	P	V_{SS}
R20	I/O	MD5
T1	I/O	PI.2 / EPWM0_CH2 / UART12_RXD / CAN0_RXD / SPI3_MOSI / SC0_DAT / EBI_ADR2 / TM1 / ECAP1_IC2
T2	I/O	PJ.14 / EPWM1_CH4 / UART2_RXD / CAN3_RXD / SPI3_MISO / SC1_RST / EBI_ADR14 / TM3
T3	I/O	PI.5 / EPWM0_CH5 / UART14_nRTS / UART13_TXD / I2C3_SCL / I2S1_BCLK / EBI_ADR5 / INT1
T4	I/O	PJ.15 / EPWM1_CH5 / UART2_TXD / CAN3_TXD / SPI3_CLK / EADC0_ST / SC1_PWR / EBI_ADR15 / TM3_EXT / INT1
T5	I/O	PJ.13 / EPWM1_CH3 / UART2_nRTS / UART1_TXD / I2C5_SCL / SPI3_MOSI / SC1_DAT / EBI_ADR13 / TM2_EXT
T6	I/O	PL.7 / EPWM0_CH1 / UART2_TXD / CAN0_TXD / QSPI1_MISO1 / EBI_AD6 / TM3_EXT / ECAP1_IC1 / INT1
T7	I/O	PD.8 / EPWM0_BRAKE0 / UART16_nCTS / UART15_RXD / QSPI1_SS0 / I2S1_LRCK / EPWM0_CH2 / EBI_AD7 / SC1_CLK / TM0
T8	I/O	PL.1 / EPWM1_CH1 / UART11_nRTS / UART10_TXD / I2C3_SCL / SPI2_MISO / QSPI1_MISO1 / I2S0_BCLK / EBI_AD12 / SC1_DAT / TM5_EXT / QEI1_B

Pin	Type	MA35D16A087C (BGA 364-Ball, non-MCP) Pin Function
T9	I/O	PM.1 / I2C4_SCL / SPI3_I2SMCLK / CCAP0_SFIELD / EBI_AD4 / EBI_ADR4
T10	I/O	PL.0 / EPWM1_CH0 / UART11_nCTS / UART10_RXD / I2C3_SDA / SPI2_MOSI / QSPI1_MOSI1 / I2S0_LRCK / EBI_AD11 / SC1_CLK / TM5 / QEI1_A
T11	I/O	PL.5 / EPWM1_CH5 / UART2_nRTS / UART1_TXD / I2C4_SCL / SPI3_MISO / QSPI1_MISO0 / I2S1_MCLK / EBI_nWR / SC0_nCD / TM9_EXT / ECAP0_IC2
T12	I/O	PJ.4 / I2C3_SDA / SD1_WP
T13	I/O	PJ.5 / I2C3_SCL / SD1_nCD
T14	I/O	PK.6 / EPWM1_CH2 / UART12_RXD / CAN0_RXD / SPI2_MOSI / I2S1_BCLK / SC0_RST / TM6 / INT2
T15	I/O	PK.5 / EPWM1_CH1 / UART12_nRTS / UART13_TXD / I2C4_SCL / SPI2_CLK / I2S1_DI / SC0_DAT / EADC0_ST / TM8_EXT / INT1
T16	I/O	PK.7 / EPWM1_CH3 / UART12_TXD / CAN0_TXD / SPI2_MISO / I2S1_LRCK / SC0_PWR / CLKO / TM6_EXT / INT3
T17	P	V_{SS}
T18	P	V_{SS}
T19	I/O	PD.0 / UART3_nCTS / UART4_RXD / QSPI0_SS0
T20	P	V_{SS}
U1	I/O	PI.6 / EPWM0_BRAKE0 / UART14_RXD / CAN1_RXD / I2S1_DI / EBI_ADR6 / QEI1_INDEX / INT2
U2	I/O	PJ.12 / EPWM1_CH2 / UART2_nCTS / UART1_RXD / I2C5_SDA / SPI3_SS0 / SC1_CLK / EBI_ADR12 / TM2 / QEI0_INDEX
U3	I/O	PI.7 / EPWM0_BRAKE1 / UART14_TXD / CAN1_TXD / I2S1_DO / EBI_ADR7 / ECAP0_IC0 / INT3
U4	I/O	PL.9 / EPWM0_CH3 / UART14_nRTS / UART13_TXD / I2C5_SCL / SPI3_CLK / EPWM1_CH4 / I2S1_BCLK / EBI_AD8 / SC0_DAT / TM4_EXT / QEI0_A / INT3
U5	I/O	PL.11 / EPWM0_CH5 / UART14_TXD / CAN3_TXD / SPI3_MISO / EPWM1_CH5 / I2S1_DO / EBI_AD10 / SC0_PWR / EBI_nWRL / QEI0_INDEX
U6	I/O	PE.15 / UART0_RXD
U7	I/O	PM.11 / EPWM1_CH3 / CAN2_TXD / SPI3_SS1 / CCAP0_DATA9 / SPI2_SS1 / EBI_AD14 / EBI_ADR14
U8	I/O	PK.11 / CAN1_TXD / CCAP0_HSYNC / EBI_AD2 / EBI_ADR2
U9	I/O	PM.3 / CAN3_TXD / CCAP0_DATA1 / EBI_AD6 / EBI_ADR6
U10	I/O	PM.5 / I2C5_SCL / CCAP0_DATA3 / EBI_AD8 / EBI_ADR8
U11	I/O	PM.9 / I2C0_SCL / CCAP0_DATA7 / EBI_AD12 / EBI_ADR12
U12	I/O	PJ.9 / I2C4_SCL / SD1_DAT1/eMMC1_DAT1
U13	I/O	PG.9 / EPWM1_CH5 / UART12_TXD / CAN3_TXD / SPI2_CLK / LCM_HSYNC/LCM_MPU_WR/RW / I2C3_SCL / EBI_AD8 / EBI_nCS1
U14	I/O	PI.10 / UART4_RXD / LCM_DATA2/LCM_MPU_D2 / EBI_AD13
U15	I/O	PH.0 / UART8_nCTS / UART7_RXD / LCM_DATA8/LCM_MPU_D8
U16	I/O	PH.7 / UART10_TXD / LCM_DATA15/LCM_MPU_D15

Pin	Type	MA35D16A087C (BGA 364-Ball, non-MCP) Pin Function
U17	I/O	PC.12 / UART12_nCTS / UART11_RXD / LCM_DATA16/LCM_MPU_D16
U18	I/O	PH.13 / UART14_nRTS / UART13_TXD / LCM_DATA21
U19	I/O	PD.5 / UART1_nRTS / UART2_TXD / I2C2_SCL / QSPI0_MISO1
U20	I/O	PD.3 / UART3_TXD / QSPI0_MISO0
V1	I/O	PK.0 / EPWM0_SYNC_IN / UART16_nCTS / UART15_RXD / I2C4_SDA / I2S1_MCLK / EBI_ADR8 / TM7 / ECAP0_IC1
V2	I/O	PK.2 / EPWM1_CH0 / UART16_RXD / CAN2_RXD / SPI3_I2SMCLK / SC0_PWR / EBI_ADR10 / QEI0_A
V3	I/O	PD.9 / EPWM0_BRAKE1 / UART16_nRTS / UART15_TXD / QSPI1_CLK / I2S1_BCLK / EPWM0_CH3 / EBI_AD8 / SC1_DAT / TM0_EXT
V4	I/O	PD.11 / EPWM1_BRAKE1 / UART16_TXD / QSPI1_MISO0 / I2S1_DO / EPWM0_CH5 / EBI_AD10 / SC1_PWR / TM2_EXT
V5	I/O	PL.3 / EPWM1_CH3 / UART11_TXD / CAN3_TXD / SPI2_CLK / QSPI1_CLK / I2S0_DO / EBI_AD14 / SC1_PWR / TM7_EXT / ECAP0_IC0
V6	I/O	PK.9 / I2C3_SCL / CCAP0_SCLK / EBI_AD0 / EBI_ADR0
V7	I/O	PM.7 / CAN0_TXD / CCAP0_DATA5 / EBI_AD10 / EBI_ADR10
V8	I/O	PM.2 / CAN3_RXD / CCAP0_DATA0 / EBI_AD5 / EBI_ADR5
V9	I/O	PM.4 / I2C5_SDA / CCAP0_DATA2 / EBI_AD7 / EBI_ADR7
V10	I/O	PM.6 / CAN0_RXD / CCAP0_DATA4 / EBI_AD9 / EBI_ADR9
V11	I/O	PJ.7 / CAN3_TXD / SD1_CLK/eMMC1_CLK
V12	I/O	PI.8 / UART4_nCTS / UART3_RXD / LCM_DATA0/LCM_MPU_D0 / EBI_AD11
V13	I/O	PK.4 / UART12_nCTS / UART13_RXD / SPI2_MISO / LCM_DEN/LCM_MPU_RS / EBI_AD10 / EBI_nWRL
V14	I/O	PI.12 / UART6_nCTS / UART5_RXD / LCM_DATA4/LCM_MPU_D4
V15	I/O	PI.14 / UART6_RXD / LCM_DATA6/LCM_MPU_D6
V16	I/O	PH.5 / UART10_nRTS / UART9_TXD / LCM_DATA13/LCM_MPU_D13
V17	I/O	PC.15 / UART12_TXD / LCM_DATA19 / LCM_MPU_TE / LCM_MPU_VSYNC
V18	I/O	PD.2 / UART3_RXD / QSPI0_MOSI0
V19	I/O	PH.12 / UART14_nCTS / UART13_RXD / LCM_DATA20
V20	I/O	PD.1 / UART3_nRTS / UART4_TXD / QSPI0_CLK
W1	I/O	PE.14 / UART0_TXD
W2	I/O	PL.6 / EPWM0_CH0 / UART2_RXD / CAN0_RXD / QSPI1_MOSI1 / TRACE_CLK / EBI_AD5 / TM3 / ECAP1_IC0 / INT0
W3	I/O	PL.8 / EPWM0_CH2 / UART14_nCTS / UART13_RXD / I2C5_SDA / SPI3_SS0 / EPWM0_CH4 / I2S1_LRCK / EBI_AD7 / SC0_CLK / TM4 / ECAP1_IC2 / INT2
W4	I/O	PD.6 / EPWM0_SYNC_IN / UART1_RXD / QSPI1_MOSI1 / I2C0_SDA / I2S0_MCLK / EPWM0_CH0 / EBI_AD5 / SPI3_SS1 / TRACE_CLK **Note:** This pin is dedicated as I2C0_SDA function for controlling external PMIC by default.

Pin	Type	MA35D16A087C (BGA 364-Ball, non-MCP) Pin Function
W5	I/O	PL.2 / EPWM1_CH2 / UART11_RXD / CAN3_RXD / SPI2_SS0 / QSPI1_SS1 / I2S0_DI / EBI_AD13 / SC1_RST / TM7 / QEI1_INDEX
W6	I/O	PL.4 / EPWM1_CH4 / UART2_nCTS / UART1_RXD / I2C4_SDA / SPI3_MOSI / QSPI1_MOSI0 / I2S0_MCLK / EBI_nRD / SC1_nCD / TM9 / ECAP0_IC1
W7	I/O	PM.0 / I2C4_SDA / CCAP0_VSYNC / EBI_AD3 / EBI_ADR3
W8	I/O	PM.10 / EPWM1_CH2 / CAN2_RXD / SPI3_SS0 / CCAP0_DATA8 / SPI2_I2SMCLK / EBI_AD13 / EBI_ADR13
W9	I/O	PJ.1 / EPWM1_BRAKE1 / UART8_nRTS / UART7_TXD / I2C2_SCL / SPI2_CLK / eMMC1_DAT5 / I2S0_BCLK / SC0_DAT / EBI_AD12 / EBI_ADR17 / EBI_nCS1 / EBI_AD8
W10	I/O	PJ.11 / CAN0_TXD / SD1_DAT3/eMMC1_DAT3
W11	I/O	PJ.6 / CAN3_RXD / SD1_CMD/eMMC1_CMD
W12	I/O	PJ.10 / CAN0_RXD / SD1_DAT2/eMMC1_DAT2
W13	I/O	PG.10 / UART12_nRTS / UART13_TXD / SPI2_MOSI / LCM_CLK / EBI_AD9 / EBI_nWRH
W14	I/O	PC.14 / UART12_RXD / LCM_DATA18/LCM_MPU_CS
W15	I/O	PI.13 / UART6_nRTS / UART5_TXD / LCM_DATA5/LCM_MPU_D5
W16	I/O	PH.1 / UART8_nRTS / UART7_TXD / LCM_DATA9/LCM_MPU_D9
W17	I/O	PH.6 / UART10_RXD / LCM_DATA14/LCM_MPU_D14
W18	I/O	PC.13 / UART12_nRTS / UART11_TXD / LCM_DATA17/LCM_MPU_D17
W19	I/O	PH.15 / UART14_TXD / LCM_DATA23
W20	I/O	PH.14 / UART14_RXD / LCM_DATA22
Y1	P	V_{SS}
Y2	I/O	PL.10 / EPWM0_CH4 / UART14_RXD / CAN3_RXD / SPI3_MOSI / EPWM0_CH5 / I2S1_DI / EBI_AD9 / SC0_RST / EBI_nWRH / QEI0_B
Y3	I/O	PD.7 / EPWM0_SYNC_OUT / UART1_TXD / QSPI1_MISO1 / I2C0_SCL / I2S1_MCLK / EPWM0_CH1 / EBI_AD6 / SC1_nCD / EADC0_ST **Note:** This pin is dedicated as I2C0_SCL function for controlling external PMIC by default.
Y4	I/O	PD.10 / EPWM1_BRAKE0 / UART16_RXD / QSPI1_MOSI0 / I2S1_DI / EPWM0_CH4 / EBI_AD9 / SC1_RST / TM2
Y5	I/O	PK.8 / EPWM1_CH0 / I2C3_SDA / SPI3_CLK / EADC0_ST / EBI_AD15 / EBI_MCLK / EBI_ADR15 / TM8 / QEI1_INDEX
Y6	I/O	PK.10 / CAN1_RXD / CCAP0_PIXCLK / EBI_AD1 / EBI_ADR1
Y7	I/O	PM.8 / I2C0_SDA / CCAP0_DATA6 / EBI_AD11 / EBI_ADR11
Y8	I/O	PJ.3 / EPWM1_CH5 / UART8_TXD / CAN1_TXD / SPI2_MISO / eMMC1_DAT7 / I2S0_DO / SC0_PWR / EBI_AD14 / EBI_ADR19 / EBI_nWRL / EBI_AD10
Y9	I/O	PJ.0 / EPWM1_BRAKE0 / UART8_nCTS / UART7_RXD / I2C2_SDA / SPI2_SS0 / eMMC1_DAT4 / I2S0_LRCK / SC0_CLK / EBI_AD11 / EBI_ADR16 / EBI_nCS0 / EBI_AD7
Y10	I/O	PJ.2 / EPWM1_CH4 / UART8_RXD / CAN1_RXD / SPI2_MOSI / eMMC1_DAT6 / I2S0_DI / SC0_RST / EBI_AD13 / EBI_ADR18 / EBI_nWRH / EBI_AD9
Y11	I/O	PJ.8 / I2C4_SDA / SD1_DAT0/eMMC1_DAT0

Pin	Type	MA35D16A087C (BGA 364-Ball, non-MCP) Pin Function
Y12	I/O	PG.8 / EPWM1_CH4 / UART12_RXD / CAN3_RXD / SPI2_SS0 / LCM_VSYNC/LCM_MPU_RD/EN / I2C3_SDA / EBI_AD7 / EBI_nCS0
Y13	I/O	PH.2 / UART8_RXD / LCM_DATA10/LCM_MPU_D10
Y14	I/O	PI.9 / UART4_nRTS / UART3_TXD / LCM_DATA1/LCM_MPU_D1 / EBI_AD12
Y15	I/O	PI.11 / UART4_TXD / LCM_DATA3/LCM_MPU_D3 / EBI_AD14
Y16	I/O	PI.15 / UART6_TXD / LCM_DATA7/LCM_MPU_D7
Y17	I/O	PH.3 / UART8_TXD / LCM_DATA11/LCM_MPU_D11
Y18	I/O	PH.4 / UART10_nCTS / UART9_RXD / LCM_DATA12/LCM_MPU_D12
Y19	I/O	PD.4 / UART1_nCTS / UART2_RXD / I2C2_SDA / QSPI0_MOSI1
Y20	P	V_{SS}

4.2.4 MA35D1 Series Multi-function Description Table

Group	Pin Name	Type	Description
ADC0	ADC0_CH0	A	ADC0 channel 0 analog input.
	ADC0_CH1	A	ADC0 channel 1 analog input.
	ADC0_CH2	A	ADC0 channel 2 analog input.
	ADC0_CH3	A	ADC0 channel 3 analog input.
	ADC0_CH4	A	ADC0 channel 4 analog input.
	ADC0_CH5	A	ADC0 channel 5 analog input.
	ADC0_CH6	A	ADC0 channel 6 analog input.
	ADC0_CH7	A	ADC0 channel 7 analog input.
CAN0	CAN0_RXD	I	CAN0 bus receiver input.
	CAN0_TXD	O	CAN0 bus transmitter output.
CAN1	CAN1_RXD	I	CAN1 bus receiver input.
	CAN1_TXD	O	CAN1 bus transmitter output.
CAN2	CAN2_RXD	I	CAN2 bus receiver input.
	CAN2_TXD	O	CAN2 bus transmitter output.
CAN3	CAN3_RXD	I	CAN3 bus receiver input.
	CAN3_TXD	O	CAN3 bus transmitter output.
CCAP0	CCAP0_DATA0	I	Video Image/Camera capture 0 data input bus bit 0. (YUV DATA [0])
	CCAP0_DATA1	I	Video Image/Camera capture 0 data input bus bit 1. (YUV DATA [1])
	CCAP0_DATA2	I	Video Image/Camera capture 0 data input bus bit 2. (YUV DATA [2])
	CCAP0_DATA3	I	Video Image/Camera capture 0 data input bus bit 3. (YUV DATA [3])
	CCAP0_DATA4	I	Video Image/Camera capture 0 data input bus bit 4. (YUV DATA [4])
	CCAP0_DATA5	I	Video Image/Camera capture 0 data input bus bit 5. (YUV DATA [5])
	CCAP0_DATA6	I	Video Image/Camera capture 0 data input bus bit 6. (YUV DATA [6])
	CCAP0_DATA7	I	Video Image/Camera capture 0 data input bus bit 7. (YUV DATA [7])
	CCAP0_DATA8	I	Video Image/Camera capture 0 data input bus bit 8.
	CCAP0_DATA9	I	Video Image/Camera capture 0 data input bus bit 9.
	CCAP0_HSYNC	I	Video Image/Camera capture 0 interface HSYNC input pin.
	CCAP0_PIXCLK	I	Video Image/Camera capture 0 interface pixel clock input pin.
	CCAP0_SCLK	O	Video Image/Camera capture 0 interface sensor clock output pin.
	CCAP0_SFIELD	I	Video Image/Camera capture 0 interface SFIELD input pin.
	CCAP0_VSYNC	I	Video Image/Camera capture 0 interface VSYNC input pin.
CCAP1	CCAP1_DATA0	I	Video Image/Camera capture 1 data input bus bit 0. (YUV DATA [0])

Group	Pin Name	Type	Description
	CCAP1_DATA1	I	Video Image/Camera capture 1 data input bus bit 1. (YUV DATA [1])
	CCAP1_DATA2	I	Video Image/Camera capture 1 data input bus bit 2. (YUV DATA [2])
	CCAP1_DATA3	I	Video Image/Camera capture 1 data input bus bit 3. (YUV DATA [3])
	CCAP1_DATA4	I	Video Image/Camera capture 1 data input bus bit 4. (YUV DATA [4])
	CCAP1_DATA5	I	Video Image/Camera capture 1 data input bus bit 5. (YUV DATA [5])
	CCAP1_DATA6	I	Video Image/Camera capture 1 data input bus bit 6. (YUV DATA [6])
	CCAP1_DATA7	I	Video Image/Camera capture 1 data input bus bit 7. (YUV DATA[7])
	CCAP1_DATA8	I	Video Image/Camera capture 1 data input bus bit 8.
	CCAP1_DATA9	I	Video Image/Camera capture 1 data input bus bit 9.
	CCAP1_HSYNC	I	Video Image/Camera capture 1 interface HSYNC input pin.
	CCAP1_PIXCLK	I	Video Image/Camera capture 1 interface pixel clock input pin.
	CCAP1_SCLK	O	Video Image/Camera capture 1 interface sensor clock output pin.
	CCAP1_SFIELD	I	Video Image/Camera capture 1 interface SFIELD input pin.
	CCAP1_VSYNC	I	Video Image/Camera capture 1 interface VSYNC input pin.
CLKO	CLKO	O	Clock output pin.
CLK	CLK_32KOUT	O	32 kHz clock output pin.
EADC0	EADC0_CH0	A	EADC0 channel 0 analog input.
	EADC0_CH1	A	EADC0 channel 1 analog input.
	EADC0_CH2	A	EADC0 channel 2 analog input.
	EADC0_CH3	A	EADC0 channel 3 analog input.
	EADC0_CH4	A	EADC0 channel 4 analog input.
	EADC0_CH5	A	EADC0 channel 5 analog input.
	EADC0_CH6	A	EADC0 channel 6 analog input.
	EADC0_CH7	A	EADC0 channel 7 analog input.
	EADC0_ST	I	EADC0 external trigger input.
EBI	EBI_AD0	I/O	EBI address/data bus bit 0.
	EBI_AD1	I/O	EBI address/data bus bit 1.
	EBI_AD2	I/O	EBI address/data bus bit 2.
	EBI_AD3	I/O	EBI address/data bus bit 3.
	EBI_AD4	I/O	EBI address/data bus bit 4.
	EBI_AD5	I/O	EBI address/data bus bit 5.
	EBI_AD6	I/O	EBI address/data bus bit 6.
	EBI_AD7	I/O	EBI address/data bus bit 7.

Group	Pin Name	Type	Description
	EBI_AD8	I/O	EBI address/data bus bit 8.
	EBI_AD9	I/O	EBI address/data bus bit 9.
	EBI_AD10	I/O	EBI address/data bus bit 10.
	EBI_AD11	I/O	EBI address/data bus bit 11.
	EBI_AD12	I/O	EBI address/data bus bit 12.
	EBI_AD13	I/O	EBI address/data bus bit 13.
	EBI_AD14	I/O	EBI address/data bus bit 14.
	EBI_AD15	I/O	EBI address/data bus bit 15.
	EBI_ADR0	O	EBI address bus bit 0.
	EBI_ADR1	O	EBI address bus bit 1.
	EBI_ADR2	O	EBI address bus bit 2.
	EBI_ADR3	O	EBI address bus bit 3.
	EBI_ADR4	O	EBI address bus bit 4.
	EBI_ADR5	O	EBI address bus bit 5.
	EBI_ADR6	O	EBI address bus bit 6.
	EBI_ADR7	O	EBI address bus bit 7.
	EBI_ADR8	O	EBI address bus bit 8.
	EBI_ADR9	O	EBI address bus bit 9.
	EBI_ADR10	O	EBI address bus bit 10.
	EBI_ADR11	O	EBI address bus bit 11.
	EBI_ADR12	O	EBI address bus bit 12.
	EBI_ADR13	O	EBI address bus bit 13.
	EBI_ADR14	O	EBI address bus bit 14.
	EBI_ADR15	O	EBI address bus bit 15.
	EBI_ADR16	O	EBI address bus bit 16.
	EBI_ADR17	O	EBI address bus bit 17.
	EBI_ADR18	O	EBI address bus bit 18.
	EBI_ADR19	O	EBI address bus bit 19.
	EBI_ALE	O	EBI address latch enable output pin.
	EBI_MCLK	O	EBI external clock output pin.
	EBI_nCS0	O	EBI chip select 0 output pin.
	EBI_nCS1	O	EBI chip select 1 output pin.
	EBI_nCS2	O	EBI chip select 2 output pin.

Group	Pin Name	Type	Description
	EBI_nRD	O	EBI read enable output pin.
	EBI_nWR	O	EBI write enable output pin.
	EBI_nWRH	O	EBI high byte write enable output pin.
	EBI_nWRL	O	EBI low byte write enable output pin.
ECAP0	ECAP0_IC0	I	Enhanced capture unit 0 input 0 pin.
	ECAP0_IC1	I	Enhanced capture unit 0 input 1 pin.
	ECAP0_IC2	I	Enhanced capture unit 0 input 2 pin.
ECAP1	ECAP1_IC0	I	Enhanced capture unit 1 input 0 pin.
	ECAP1_IC1	I	Enhanced capture unit 1 input 1 pin.
	ECAP1_IC2	I	Enhanced capture unit 1 input 2 pin.
ECAP2	ECAP2_IC0	I	Enhanced capture unit 2 input 0 pin.
	ECAP2_IC1	I	Enhanced capture unit 2 input 1 pin.
	ECAP2_IC2	I	Enhanced capture unit 2 input 2 pin.
EPWM0	EPWM0_BRAKE0	I	EPWM0 Brake 0 input pin.
	EPWM0_BRAKE1	I	EPWM0 Brake 1 input pin.
	EPWM0_CH0	I/O	EPWM0 channel 0 output/capture input.
	EPWM0_CH1	I/O	EPWM0 channel 1 output/capture input.
	EPWM0_CH2	I/O	EPWM0 channel 2 output/capture input.
	EPWM0_CH3	I/O	EPWM0 channel 3 output/capture input.
	EPWM0_CH4	I/O	EPWM0 channel 4 output/capture input.
	EPWM0_CH5	I/O	EPWM0 channel 5 output/capture input.
	EPWM0_SYNC_IN	I	EPWM0 counter synchronous trigger input pin.
	EPWM0_SYNC_OUT	O	EPWM0 counter synchronous trigger output pin.
EPWM1	EPWM1_BRAKE0	I	EPWM1 Brake 0 input pin.
	EPWM1_BRAKE1	I	EPWM1 Brake 1 input pin.
	EPWM1_CH0	I/O	EPWM1 channel 0 output/capture input.
	EPWM1_CH1	I/O	EPWM1 channel 1 output/capture input.
	EPWM1_CH2	I/O	EPWM1 channel 2 output/capture input.
	EPWM1_CH3	I/O	EPWM1 channel 3 output/capture input.
	EPWM1_CH4	I/O	EPWM1 channel 4 output/capture input.
	EPWM1_CH5	I/O	EPWM1 channel 5 output/capture input.
EPWM2	EPWM2_BRAKE0	I	EPWM2 Brake 0 input pin.
	EPWM2_BRAKE1	I	EPWM2 Brake 1 input pin.

Group	Pin Name	Type	Description
	EPWM2_CH0	I/O	EPWM2 channel 0 output/capture input.
	EPWM2_CH1	I/O	EPWM2 channel 1 output/capture input.
	EPWM2_CH2	I/O	EPWM2 channel 2 output/capture input.
	EPWM2_CH3	I/O	EPWM2 channel 3 output/capture input.
	EPWM2_CH4	I/O	EPWM2 channel 4 output/capture input.
	EPWM2_CH5	I/O	EPWM2 channel 5 output/capture input.
HSUSB0	HSUSB0_VBUSVLD	I	HSUSB0 external V_{BUS} status pin.
HSUSBH	HSUSBH_OVC	I	HSUSB host bus power overcurrent detector pin.
	HSUSBH_PWREN	O	HSUSB host external V_{BUS} regulator enable pin.
I2C0	I2C0_SCL	I/O	I2C0 clock pin.
	I2C0_SDA	I/O	I2C0 data input/output pin.
I2C1	I2C1_SCL	I/O	I2C1 clock pin.
	I2C1_SDA	I/O	I2C1 data input/output pin.
I2C2	I2C2_SCL	I/O	I2C2 clock pin.
	I2C2_SDA	I/O	I2C2 data input/output pin.
I2C3	I2C3_SCL	I/O	I2C3 clock pin.
	I2C3_SDA	I/O	I2C3 data input/output pin.
I2C4	I2C4_SCL	I/O	I2C4 clock pin.
	I2C4_SDA	I/O	I2C4 data input/output pin.
I2C5	I2C5_SCL	I/O	I2C5 clock pin.
	I2C5_SDA	I/O	I2C5 data input/output pin.
I2S0	I2S0_BCLK	O	I2S0 bit clock output pin.
	I2S0_DI	I	I2S0 data input pin.
	I2S0_DO	O	I2S0 data output pin.
	I2S0_LRCK	O	I2S0 left right channel clock output pin.
	I2S0_MCLK	O	I2S0 master clock output pin.
I2S1	I2S1_BCLK	O	I2S1 bit clock output pin.
	I2S1_DI	I	I2S1 data input pin.
	I2S1_DO	O	I2S1 data output pin.
	I2S1_LRCK	O	I2S1 left right channel clock output pin.
	I2S1_MCLK	O	I2S1 master clock output pin.
INT0	INT0	I	External interrupt 0 input pin.
INT1	INT1	I	External interrupt 1 input pin.

Group	Pin Name	Type	Description
INT2	INT2	I	External interrupt 2 input pin.
INT3	INT3	I	External interrupt 3 input pin.
JTAG	JTAG_TCK/SW_CLK	I	JTAG clock input pin. Serial wire clock input pin.
	JTAG_TDI	I	JTAG data input pin.
	JTAG_TDO	O	JTAG data output pin.
	JTAG_TMS/SW_DIO	I I/O	JTAG test mode selection input pin. Serial wire data pin.
	JTAG_nTRST	I	JTAG reset input pin.
KPI	KPI_COL0	I	Keypad Interface Column 0 input pin.
	KPI_COL1	I	Keypad Interface Column 1 input pin.
	KPI_COL2	I	Keypad Interface Column 2 input pin.
	KPI_COL3	I	Keypad Interface Column 3 input pin.
	KPI_COL4	I	Keypad Interface Column 4 input pin.
	KPI_COL5	I	Keypad Interface Column 5 input pin.
	KPI_COL6	I	Keypad Interface Column 6 input pin.
	KPI_COL7	I	Keypad Interface Column 7 input pin.
	KPI_ROW0	O	Keypad Interface Row 0 output pin.
	KPI_ROW1	O	Keypad Interface Row 1 output pin.
	KPI_ROW2	O	Keypad Interface Row 2 output pin.
	KPI_ROW3	O	Keypad Interface Row 3 output pin.
	KPI_ROW4	O	Keypad Interface Row 4 output pin.
	KPI_ROW5	O	Keypad Interface Row 5 output pin.
	KPI_ROW6	O	Keypad Interface Row 6 output pin.
	KPI_ROW7	O	Keypad Interface Row 7 output pin.
LCM	LCM_CLK	O	TFT LCD Module Pixel Clock output pin in Sync-type mode.
	LCM_DATA0/LCM_MPU_D0	I/O	TFT LCD Module Pixel Data output bit 0 in Sync-type mode. TFT LCD Module Command/Data input/output bit 0 in MPU-type mode.
	LCM_DATA1/LCM_MPU_D1	I/O	TFT LCD Module Pixel Data output bit 1 in Sync-type mode. TFT LCD Module Command/Data input/output bit 1 in MPU-type mode.
	LCM_DATA10/LCM_MPU_D10	I/O	TFT LCD Module Pixel Data output bit 10 in Sync-type mode. TFT LCD Module Command/Data input/output bit 10 in MPU-type mode.
	LCM_DATA11/LCM_MPU_D11	I/O	TFT LCD Module Pixel Data output bit 11 in Sync-type mode. TFT LCD Module Command/Data input/output bit 11 in MPU-type mode.
	LCM_DATA12/LCM_M	I/O	TFT LCD Module Pixel Data output bit 12 in Sync-type mode.

Group	Pin Name	Type	Description
	PU_D12		TFT LCD Module Command/Data input/output bit 12 in MPU-type mode.
	LCM_DATA13/LCM_MPU_D13	I/O	TFT LCD Module Pixel Data output bit 13 in Sync-type mode. TFT LCD Module Command/Data input/output bit 13 in MPU-type mode.
	LCM_DATA14/LCM_MPU_D14	I/O	TFT LCD Module Pixel Data output bit 14 in Sync-type mode. TFT LCD Module Command/Data input/output bit 14 in MPU-type mode.
	LCM_DATA15/LCM_MPU_D15	I/O	TFT LCD Module Pixel Data output bit 15 in Sync-type mode. TFT LCD Module Command/Data input/output bit 15 in MPU-type mode.
	LCM_DATA16/LCM_MPU_D16	I/O	TFT LCD Module Pixel Data output bit 16 in Sync-type mode. TFT LCD Module Command/Data input/output bit 16 in MPU-type mode.
	LCM_DATA17/LCM_MPU_D17	I/O	TFT LCD Module Pixel Data output bit 17 in Sync-type mode. TFT LCD Module Command/Data input/output bit 17 in MPU-type mode.
	LCM_DATA18/LCM_MPU_CS	O	TFT LCD Module Pixel Data output bit 18 in Sync-type mode. TFT LCD Module Chip Select output pin in MPU-type mode.
	LCM_DATA19	O	TFT LCD Module Pixel Data output bit 19 in Sync-type mode.
	LCM_DATA2/LCM_MPU_D2	I/O	TFT LCD Module Pixel Data output bit 2 in Sync-type mode. TFT LCD Module Command/Data input/output bit 2 in MPU-type mode.
	LCM_DATA20	O	TFT LCD Module Pixel Data output bit 20 in Sync-type mode.
	LCM_DATA21	O	TFT LCD Module Pixel Data output bit 21 in Sync-type mode.
	LCM_DATA22	O	TFT LCD Module Pixel Data output bit 22 in Sync-type mode.
	LCM_DATA23	O	TFT LCD Module Pixel Data output bit 23 in Sync-type mode.
	LCM_DATA3/LCM_MPU_D3	I/O	TFT LCD Module Pixel Data output bit 3 in Sync-type mode. TFT LCD Module Command/Data input/output bit 3 in MPU-type mode.
	LCM_DATA4/LCM_MPU_D4	I/O	TFT LCD Module Pixel Data output bit 4 in Sync-type mode. TFT LCD Module Command/Data input/output bit 4 in MPU-type mode.
	LCM_DATA5/LCM_MPU_D5	I/O	TFT LCD Module Pixel Data output bit 5 in Sync-type mode. TFT LCD Module Command/Data input/output bit 5 in MPU-type mode.
	LCM_DATA6/LCM_MPU_D6	I/O	TFT LCD Module Pixel Data output bit 6 in Sync-type mode. TFT LCD Module Command/Data input/output bit 6 in MPU-type mode.
	LCM_DATA7/LCM_MPU_D7	I/O	TFT LCD Module Pixel Data output bit 7 in Sync-type mode. TFT LCD Module Command/Data input/output bit 7 in MPU-type mode.
	LCM_DATA8/LCM_MPU_D8	I/O	TFT LCD Module Pixel Data output bit 8 in Sync-type mode. TFT LCD Module Command/Data input/output bit 8 in MPU-type mode.
	LCM_DATA9/LCM_MPU_D9	I/O	TFT LCD Module Pixel Data output bit 9 in Sync-type mode. TFT LCD Module Command/Data input/output bit 9 in MPU-type mode.
	LCM_DEN/LCM_MPU_RS	O	TFT LCD Module Data Enable/Display Control Signal output pin in Sync-type mode. TFT LCD Module Register Select (RS) output pin in MPU-type mode.
	LCM_HSYNC/LCM_MPU_WR/RW	O	TFT LCD Module Horizontal/Line sync. output in Sync-type mode. TFT LCD Module Write(WR)/ReadWrite(RW) output pin in MPU-type

Group	Pin Name	Type	Description
			mode.
	LCM_MPU_TE	I	TFT LCD Module TE input pin in MPU-type mode.
	LCM_MPU_VSYNC	O	TFT LCD Module VSYNC output pin in MPU-type mode.
	LCM_VSYNC/LCM_MPU_RD/EN	O	TFT LCD Module Vertical/Frame sync. output pin in Sync-type mode. TFT LCD Module Read(RD)/Enable(EN) output pin in MPU-type mode.
NAND	NAND_ALE	O	NAND Flash address latch enable output pin.
	NAND_CLE	O	NAND Flash command latch enable output pin.
	NAND_DATA0	I/O	NAND Flash date bus bit 0.
	NAND_DATA1	I/O	NAND Flash date bus bit 1.
	NAND_DATA2	I/O	NAND Flash date bus bit 2.
	NAND_DATA3	I/O	NAND Flash date bus bit 3.
	NAND_DATA4	I/O	NAND Flash date bus bit 4.
	NAND_DATA5	I/O	NAND Flash date bus bit 5.
	NAND_DATA6	I/O	NAND Flash date bus bit 6.
	NAND_DATA7	I/O	NAND Flash date bus bit 7.
	NAND_RDY0	I	NAND Flash ready/busy 0 input pin.
	NAND_RDY1	I	NAND Flash ready/busy 1 input pin.
	NAND_nCS0	O	NAND Flash chip select 0 pin.
	NAND_nCS1	O	NAND Flash chip select 1 pin.
	NAND_nRE	O	NAND Flash read enable output pin.
	NAND_nWE	O	NAND Flash write enable output pin.
	NAND_nWP	I	NAND Flash write protect input pin.
QEI0	QEI0_A	I	Quadrature encoder 0 phase A input.
	QEI0_B	I	Quadrature encoder 0 phase B input.
	QEI0_INDEX	I	Quadrature encoder 0 index input.
QEI1	QEI1_A	I	Quadrature encoder 1 phase A input.
	QEI1_B	I	Quadrature encoder 1 phase B input.
	QEI1_INDEX	I	Quadrature encoder 1 index input.
QEI2	QEI2_A	I	Quadrature encoder 2 phase A input.
	QEI2_B	I	Quadrature encoder 2 phase B input.
	QEI2_INDEX	I	Quadrature encoder 2 index input.
QSPI0	QSPI0_CLK	I/O	Quad SPI0 serial clock pin.
	QSPI0_MISO0	I/O	Quad SPI0 MISO0 (Master In, Slave Out) pin.
	QSPI0_MISO1	I/O	Quad SPI0 MISO1 (Master In, Slave Out) pin.

Group	Pin Name	Type	Description
	QSPI0_MOSI0	I/O	Quad SPI0 MOSI0 (Master Out, Slave In) pin.
	QSPI0_MOSI1	I/O	Quad SPI0 MOSI1 (Master Out, Slave In) pin.
	QSPI0_SS0	I/O	Quad SPI0 slave select 0 pin.
QSPI1	QSPI1_CLK	I/O	Quad SPI1 serial clock pin.
	QSPI1_MISO0	I/O	Quad SPI1 MISO0 (Master In, Slave Out) pin.
	QSPI1_MISO1	I/O	Quad SPI1 MISO1 (Master In, Slave Out) pin.
	QSPI1_MOSI0	I/O	Quad SPI1 MOSI0 (Master Out, Slave In) pin.
	QSPI1_MOSI1	I/O	Quad SPI1 MOSI1 (Master Out, Slave In) pin.
	QSPI1_SS0	I/O	Quad SPI1 slave select 0 pin.
	QSPI1_SS1	I/O	Quad SPI1 slave select 1 pin.
RGMII0	RGMII0_MDC	O	RGMII0 PHY Management Clock output pin.
	RGMII0_MDIO	I/O	RGMII0 PHY Management Data pin.
	RGMII0_PPS	O	RGMII0 Pulse Per Second output pin.
	RGMII0_RXCLK	I	RGMII0 Mode RX Clock input pin.
	RGMII0_RXCTL	I	RGMII0 Receive Control input pin.
	RGMII0_RXD0	I	RGMII0 Receive Data bus bit 0.
	RGMII0_RXD1	I	RGMII0 Receive Data bus bit 1.
	RGMII0_RXD2	I	RGMII0 Receive Data bus bit 2.
	RGMII0_RXD3	I	RGMII0 Receive Data bus bit 3.
	RGMII0_TXCLK	O	RGMII0 Mode TX Clock output pin.
	RGMII0_TXCTL	O	RGMII0 Transmit Control output pin.
	RGMII0_TXD0	O	RGMII0 Transmit Data bus bit 0.
	RGMII0_TXD1	O	RGMII0 Transmit Data bus bit 1.
	RGMII0_TXD2	O	RGMII0 Transmit Data bus bit 2.
	RGMII0_TXD3	O	RGMII0 Transmit Data bus bit 3.
RGMII1	RGMII1_MDC	O	RGMII1 PHY Management Clock output pin.
	RGMII1_MDIO	I/O	RGMII1 PHY Management Data pin.
	RGMII1_PPS	O	RGMII1 Pulse Per Second output pin.
	RGMII1_RXCLK	I	RGMII1 Mode RX Clock input pin.
	RGMII1_RXCTL	I	RGMII1 Receive Control input pin.
	RGMII1_RXD0	I	RGMII1 Receive Data bus bit 0.
	RGMII1_RXD1	I	RGMII1 Receive Data bus bit 1.
	RGMII1_RXD2	I	RGMII1 Receive Data bus bit 2.

Group	Pin Name	Type	Description
	RGMII1_RXD3	I	RGMII1 Receive Data bus bit 3.
	RGMII1_TXCLK	O	RGMII1 Mode TX Clock output pin.
	RGMII1_TXCTL	O	RGMII1 Transmit Control output pin.
	RGMII1_TXD0	O	RGMII1 Transmit Data bus bit 0.
	RGMII1_TXD1	O	RGMII1 Transmit Data bus bit 1.
	RGMII1_TXD2	O	RGMII1 Transmit Data bus bit 2.
	RGMII1_TXD3	O	RGMII1 Transmit Data bus bit 3.
RMII0	RMII0_CRSDV	I	RMII0 Carrier Sense/Receive Data input pin.
	RMII0_MDC	O	RMII0 PHY Management Clock output pin.
	RMII0_MDIO	I/O	RMII0 PHY Management Data pin.
	RMII0_PPS	O	RMII0 Pulse Per Second output pin.
	RMII0_REFCLK	I	RMII0 Reference Clock input pin.
	RMII0_RXD0	I	RMII0 Receive Data bus bit 0.
	RMII0_RXD1	I	RMII0 Receive Data bus bit 1.
	RMII0_RXERR	I	RMII0 Receive Data Error input pin.
	RMII0_TXD0	O	RMII0 Transmit Data bus bit 0.
	RMII0_TXD1	O	RMII0 Transmit Data bus bit 1.
	RMII0_TXEN	O	RMII0 Transmit Enable output pin.
RMII1	RMII1_CRSDV	I	RMII1 Carrier Sense/Receive Data input pin.
	RMII1_MDC	O	RMII1 PHY Management Clock output pin.
	RMII1_MDIO	I/O	RMII1 PHY Management Data pin.
	RMII1_PPS	O	RMII1 Pulse Per Second output pin.
	RMII1_REFCLK	I	RMII1 Reference Clock input pin.
	RMII1_RXD0	I	RMII1 Receive Data bus bit 0.
	RMII1_RXD1	I	RMII1 Receive Data bus bit 1.
	RMII1_RXERR	I	RMII1 Receive Data Error input pin.
	RMII1_TXD0	O	RMII1 Transmit Data bus bit 0.
	RMII1_TXD1	O	RMII1 Transmit Data bus bit 1.
	RMII1_TXEN	O	RMII1 Transmit Enable output pin.
SC0	SC0_CLK	O	Smart Card 0 clock pin.
	SC0_DAT	I/O	Smart Card 0 data pin.
	SC0_PWR	O	Smart Card 0 power pin.
	SC0_RST	O	Smart Card 0 reset pin.

Group	Pin Name	Type	Description
	SC0_nCD	I	Smart Card 0 card detect pin.
SC1	SC1_CLK	O	Smart Card 1 clock pin.
	SC1_DAT	I/O	Smart Card 1 data pin.
	SC1_PWR	O	Smart Card 1 power pin.
	SC1_RST	O	Smart Card 1 reset pin.
	SC1_nCD	I	Smart Card 1 card detect pin.
SD0	SD0_CLK/eMMC0_CLK	O	SD/SDIO0 clock output pin. eMMC0 clock output pin.
	SD0_CMD/eMMC0_CMD	I/O	SD/SDIO0 command/response pin. eMMC0 command/response pin.
	SD0_DAT0/eMMC0_DAT0	I/O	SD/SDIO0 data line bit 0. eMMC0 data line bit 0.
	SD0_DAT1/eMMC0_DAT1	I/O	SD/SDIO0 data line bit 1. eMMC0 data line bit 1.
	SD0_DAT2/eMMC0_DAT2	I/O	SD/SDIO0 data line bit 2. eMMC0 data line bit 2.
	SD0_DAT3/eMMC0_DAT3	I/O	SD/SDIO0 data line bit 3. eMMC0 data line bit 3.
	SD0_WP	I	SD/SDIO0 write protect input.
	SD0_nCD	I	SD/SDIO0 card detect input pin.
SD1	SD1_CLK/eMMC1_CLK	O	SD/SDIO1 clock output pin. eMMC1 clock output pin.
	SD1_CMD/eMMC1_CMD	I/O	SD/SDIO1 command/response pin. eMMC1 command/response pin.
	SD1_DAT0/eMMC1_DAT0	I/O	SD/SDIO1 data line bit 0. eMMC1 data line bit 0.
	SD1_DAT1/eMMC1_DAT1	I/O	SD/SDIO1 data line bit 1. eMMC1 data line bit 1.
	SD1_DAT2/eMMC1_DAT2	I/O	SD/SDIO1 data line bit 2. eMMC1 data line bit 2.
	SD1_DAT3/eMMC1_DAT3	I/O	SD/SDIO1 data line bit 3. eMMC1 data line bit 3.
	SD1_WP	I	SD/SDIO1 write protect input.
	SD1_nCD	I	SD/SDIO1 card detect input pin.
SPI0	SPI0_CLK	I/O	SPI0 serial clock pin.
	SPI0_I2SMCLK	I/O	SPI0 I^{2}S master clock output pin.
	SPI0_MISO	I/O	SPI0 MISO (Master In, Slave Out) pin.

Group	Pin Name	Type	Description
	SPI0_MOSI	I/O	SPI0 MOSI (Master Out, Slave In) pin.
	SPI0_SS0	I/O	SPI0 slave select 0 pin.
	SPI0_SS1	I/O	SPI0 slave select 1 pin.
SPI1	SPI1_CLK	I/O	SPI1 serial clock pin.
	SPI1_I2SMCLK	I/O	SPI1 I^2S master clock output pin.
	SPI1_MISO	I/O	SPI1 MISO (Master In, Slave Out) pin.
	SPI1_MOSI	I/O	SPI1 MOSI (Master Out, Slave In) pin.
	SPI1_SS0	I/O	SPI1 slave select 0 pin.
	SPI1_SS1	I/O	SPI1 slave select 1 pin.
SPI2	SPI2_CLK	I/O	SPI2 serial clock pin.
	SPI2_I2SMCLK	I/O	SPI2 I^2S master clock output pin.
	SPI2_MISO	I/O	SPI2 MISO (Master In, Slave Out) pin.
	SPI2_MOSI	I/O	SPI2 MOSI (Master Out, Slave In) pin.
	SPI2_SS0	I/O	SPI2 slave select 0 pin.
	SPI2_SS1	I/O	SPI2 slave select 1 pin.
SPI3	SPI3_CLK	I/O	SPI3 serial clock pin.
	SPI3_I2SMCLK	I/O	SPI3 I^2S master clock output pin.
	SPI3_MISO	I/O	SPI3 MISO (Master In, Slave Out) pin.
	SPI3_MOSI	I/O	SPI3 MOSI (Master Out, Slave In) pin.
	SPI3_SS0	I/O	SPI3 slave select 0 pin.
	SPI3_SS1	I/O	SPI3 slave select 1 pin.
TAMPER0	TAMPER0	I/O	TAMPER detector loop pin 0.
TAMPER1	TAMPER1	I/O	TAMPER detector loop pin 1.
TM0	TM0	I/O	Timer0 event counter input/toggle output pin.
	TM0_EXT	I/O	Timer0 external capture input/toggle output pin.
TM1	TM1	I/O	Timer1 event counter input/toggle output pin.
	TM1_EXT	I/O	Timer1 external capture input/toggle output pin.
TM2	TM2	I/O	Timer2 event counter input/toggle output pin.
	TM2_EXT	I/O	Timer2 external capture input/toggle output pin.
TM3	TM3	I/O	Timer3 event counter input/toggle output pin.
	TM3_EXT	I/O	Timer3 external capture input/toggle output pin.
TM4	TM4	I/O	Timer4 event counter input/toggle output pin.
	TM4_EXT	I/O	Timer4 external capture input/toggle output pin.

Group	Pin Name	Type	Description
TM5	TM5	I/O	Timer5 event counter input/toggle output pin.
	TM5_EXT	I/O	Timer5 external capture input/toggle output pin.
TM6	TM6	I/O	Timer6 event counter input/toggle output pin.
	TM6_EXT	I/O	Timer6 external capture input/toggle output pin.
TM7	TM7	I/O	Timer7 event counter input/toggle output pin.
	TM7_EXT	I/O	Timer7 external capture input/toggle output pin.
TM8	TM8	I/O	Timer8 event counter input/toggle output pin.
	TM8_EXT	I/O	Timer8 external capture input/toggle output pin.
TM9	TM9	I/O	Timer9 event counter input/toggle output pin.
	TM9_EXT	I/O	Timer9 external capture input/toggle output pin.
TM10	TM10	I/O	Timer10 event counter input/toggle output pin.
	TM10_EXT	I/O	Timer10 external capture input/toggle output pin.
TM11	TM11	I/O	Timer11 event counter input/toggle output pin.
	TM11_EXT	I/O	Timer11 external capture input/toggle output pin.
TRACE	TRACE_CLK	O	ETM Trace Clock output pin.
	TRACE_DATA0	O	ETM Trace Data 0 output pin.
	TRACE_DATA1	O	ETM Trace Data 1 output pin.
	TRACE_DATA2	O	ETM Trace Data 2 output pin.
	TRACE_DATA3	O	ETM Trace Data 3 output pin.
UART0	UART0_RXD	I	UART0 data receiver input pin.
	UART0_TXD	O	UART0 data transmitter output pin.
UART1	UART1_RXD	I	UART1 data receiver input pin.
	UART1_TXD	O	UART1 data transmitter output pin.
	UART1_nCTS	I	UART1 clear to Send input pin.
	UART1_nRTS	O	UART1 request to Send output pin.
UART2	UART2_RXD	I	UART2 data receiver input pin.
	UART2_TXD	O	UART2 data transmitter output pin.
	UART2_nCTS	I	UART2 clear to Send input pin.
	UART2_nRTS	O	UART2 request to Send output pin.
UART3	UART3_RXD	I	UART3 data receiver input pin.
	UART3_TXD	O	UART3 data transmitter output pin.
	UART3_nCTS	I	UART3 clear to Send input pin.
	UART3_nRTS	O	UART3 request to Send output pin.

Group	Pin Name	Type	Description
UART4	UART4_RXD	I	UART4 data receiver input pin.
	UART4_TXD	O	UART4 data transmitter output pin.
	UART4_nCTS	I	UART4 clear to Send input pin.
	UART4_nRTS	O	UART4 request to Send output pin.
UART5	UART5_RXD	I	UART5 data receiver input pin.
	UART5_TXD	O	UART5 data transmitter output pin.
	UART5_nCTS	I	UART5 clear to Send input pin.
	UART5_nRTS	O	UART5 request to Send output pin.
UART6	UART6_RXD	I	UART6 data receiver input pin.
	UART6_TXD	O	UART6 data transmitter output pin.
	UART6_nCTS	I	UART6 clear to Send input pin.
	UART6_nRTS	O	UART6 request to Send output pin.
UART7	UART7_RXD	I	UART7 data receiver input pin.
	UART7_TXD	O	UART7 data transmitter output pin.
	UART7_nCTS	I	UART7 clear to Send input pin.
	UART7_nRTS	O	UART7 request to Send output pin.
UART8	UART8_RXD	I	UART8 data receiver input pin.
	UART8_TXD	O	UART8 data transmitter output pin.
	UART8_nCTS	I	UART8 clear to Send input pin.
	UART8_nRTS	O	UART8 request to Send output pin.
UART9	UART9_RXD	I	UART9 data receiver input pin.
	UART9_TXD	O	UART9 data transmitter output pin.
	UART9_nCTS	I	UART9 clear to Send input pin.
	UART9_nRTS	O	UART9 request to Send output pin.
UART10	UART10_RXD	I	UART10 data receiver input pin.
	UART10_TXD	O	UART10 data transmitter output pin.
	UART10_nCTS	I	UART10 clear to Send input pin.
	UART10_nRTS	O	UART10 request to Send output pin.
UART11	UART11_RXD	I	UART11 data receiver input pin.
	UART11_TXD	O	UART11 data transmitter output pin.
	UART11_nCTS	I	UART11 clear to Send input pin.
	UART11_nRTS	O	UART11 request to Send output pin.
UART12	UART12_RXD	I	UART12 data receiver input pin.

Group	Pin Name	Type	Description
	UART12_TXD	O	UART12 data transmitter output pin.
	UART12_nCTS	I	UART12 clear to Send input pin.
	UART12_nRTS	O	UART12 request to Send output pin.
UART13	UART13_RXD	I	UART13 data receiver input pin.
	UART13_TXD	O	UART13 data transmitter output pin.
	UART13_nCTS	I	UART13 clear to Send input pin.
	UART13_nRTS	O	UART13 request to Send output pin.
UART14	UART14_RXD	I	UART14 data receiver input pin.
	UART14_TXD	O	UART14 data transmitter output pin.
	UART14_nCTS	I	UART14 clear to Send input pin.
	UART14_nRTS	O	UART14 request to Send output pin.
UART15	UART15_RXD	I	UART15 data receiver input pin.
	UART15_TXD	O	UART15 data transmitter output pin.
	UART15_nCTS	I	UART15 clear to Send input pin.
	UART15_nRTS	O	UART15 request to Send output pin.
UART16	UART16_RXD	I	UART16 data receiver input pin.
	UART16_TXD	O	UART16 data transmitter output pin.
	UART16_nCTS	I	UART16 clear to Send input pin.
	UART16_nRTS	O	UART16 request to Send output pin.
WDT	WDT_nRST	O	Watchdog Timer reset trigger output pin.
eMMC1	eMMC1_DAT4	I/O	eMMC1 data line bit 4.
	eMMC1_DAT5	I/O	eMMC1 data line bit 5.
	eMMC1_DAT6	I/O	eMMC1 data line bit 6.
	eMMC1_DAT7	I/O	eMMC1 data line bit 7.
USB	HSUSB0_D+	A	HSUSB0 differential signal D+.
	HSUSB0_D-	A	HSUSB0 differential signal D-.
	HSUSB0_ID	I	HSUSB0 identification pin.
	HSUSB1_D+	A	HSUSB1 differential signal D+.
	HSUSB1_D-	A	HSUSB1 differential signal D-.
	V_{DD_HSUSB0}	P	3.3V power supply for high speed USB 2.0 port 0 PHY.
	V_{DD_HSUSB1}	P	3.3V power supply for high speed USB 2.0 port 1 PHY.
Analog	AV_{DD}	P	3.3V analog power supply for internal POR33, LVD, LVR and temperature sensor.
	AV_{DDH_PLL1}	P	3.3V analog power supply for PLL group 1.

Group	Pin Name	Type	Description
	AV_{DDH_PLL2}	P	3.3V analog power supply for PLL group 2.
	AV_{DDL_PLL0}	P	Low analog power supply for PLL group 0.
	AV_{DDL_PLL1}	P	Low analog power supply for PLL group 1.
	AV_{DDL_PLL2}	P	Low analog power supply for PLL group 2.
	AV_{DDL_ROSC}	P	Low analog power supply for internal 12 MHz High Speed RC Oscillator (HIRC).
	AV_{DD_ADC0}	P	3.3V analog power supply for ADC0. **Note:** PB.8~PB.15 are belong to this power domain.
	AV_{DD_EADC0}	P	3.3V analog power supply for EADC0. **Note:** EADC0_CH0~EADC0_CH7 are belong to this power domain.
	AV_{SS}	P	Ground pin for analog circuit.
	AV_{SS_PLL}	P	Ground pin for PLL.
	V_{REF_EADC0}	I	Analog EADC0 reference voltage input. **Note:** This pin needs to be connected with 0.1uF and 2.2uF capacitors.
DDR	MA0	O	External DDR SDRAM address bus bit 0.
	MA1	O	External DDR SDRAM address bus bit 1.
	MA10	O	External DDR SDRAM address bus bit 10.
	MA11	O	External DDR SDRAM address bus bit 11.
	MA12	O	External DDR SDRAM address bus bit 12.
	MA13	O	External DDR SDRAM address bus bit 13.
	MA14	O	External DDR SDRAM address bus bit 14.
	MA15	O	External DDR SDRAM address bus bit 15.
	MA2	O	External DDR SDRAM address bus bit 2.
	MA3	O	External DDR SDRAM address bus bit 3.
	MA4	O	External DDR SDRAM address bus bit 4.
	MA5	O	External DDR SDRAM address bus bit 5.
	MA6	O	External DDR SDRAM address bus bit 6.
	MA7	O	External DDR SDRAM address bus bit 7.
	MA8	O	External DDR SDRAM address bus bit 8.
	MA9	O	External DDR SDRAM address bus bit 9.
	MBA0	O	External DDR SDRAM bank address 0 output.
	MBA1	O	External DDR SDRAM bank address 1 output.
	MBA2	O	External DDR SDRAM bank address 2 output.
	MCASn	O	External DDR SDRAM column command output.
	MCKE0	O	External DDR SDRAM clock enable output 0.

Group	Pin Name	Type	Description
	MCKE1	O	External DDR SDRAM clock enable output 1.
	MCK_N	O	External DDR SDRAM negative clock output.
	MCK_P	O	External DDR SDRAM positive clock output.
	MCS0n	O	External DDR SDRAM chip select output 0.
	MCS1n	O	External DDR SDRAM chip select output 1.
	MD0	I/O	External DDR SDRAM data bus bit 0.
	MD1	I/O	External DDR SDRAM data bus bit 1.
	MD10	I/O	External DDR SDRAM data bus bit 10.
	MD11	I/O	External DDR SDRAM data bus bit 11.
	MD12	I/O	External DDR SDRAM data bus bit 12.
	MD13	I/O	External DDR SDRAM data bus bit 13.
	MD14	I/O	External DDR SDRAM data bus bit 14.
	MD15	I/O	External DDR SDRAM data bus bit 15.
	MD2	I/O	External DDR SDRAM data bus bit 2.
	MD3	I/O	External DDR SDRAM data bus bit 3.
	MD4	I/O	External DDR SDRAM data bus bit 4.
	MD5	I/O	External DDR SDRAM data bus bit 5.
	MD6	I/O	External DDR SDRAM data bus bit 6.
	MD7	I/O	External DDR SDRAM data bus bit 7.
	MD8	I/O	External DDR SDRAM data bus bit 8.
	MD9	I/O	External DDR SDRAM data bus bit 9.
	MDMask0	O	External DDR SDRAM write data mask 0 output.
	MDMask1	O	External DDR SDRAM write data mask 1 output.
	MDQS0_N	I/O	External DDR SDRAM data strobe 0 negative.
	MDQS0_P	I/O	External DDR SDRAM data strobe 0 positive.
	MDQS1_N	I/O	External DDR SDRAM data strobe 1 negative.
	MDQS1_P	I/O	External DDR SDRAM data strobe 1 positive.
	MODT0	O	External DDR SDRAM on-die termination control 0.
	MODT1	O	External DDR SDRAM on-die termination control 1.
	MRASn	O	External DDR SDRAM row command output.
	MRESETn	O	External DDR SDRAM reset signal output.
	MV_{DD}	P	Power supply for internal DDR2/DDR3L-type SDRAM or external DDR3/DDR3L-type SDRAM. **Note 1:** Please refer to the part number from MA35D1 selection guide to supply the correct voltage on this pin.

Group	Pin Name	Type	Description
			Note 2: 1.8V for internal DDR2-type SDRAM or 1.35V for internal DDR3L-type SDRAM. **Note 3:** 1.5V for external DDR3-type SDRAM or 1.35V for external DDR3L-type SDRAM.
	$MV_{DD\_DPHYPLL}$	P	2.5V power supply for PLL of DDR PHY.
	MV_{REF}	P	DDR SDRAM reference voltage. (MV_{REF} = 1/2MV_{DD})
	MV_{REF_CA}	P	DDR SDRAM reference voltage for control, command and address. (MV_{REF_CA} = 1/2MV_{DD})
	MV_{REF_DQ}	P	DDR SDRAM reference voltage for DQ data. (MV_{REF_DQ} = 1/2MV_{DD})
	MWEn	O	External DDR SDRAM write command output.
	MZQ_DDRPHY	P	An external 240Ω (1%) pull-down resistor on this pin for DDR PHY.
	MZQ_SDRAM	P	An external 240Ω (1%) pull-down resistor on this pin for internal SDRAM.
RTC	RTC_RPWR	O	RTC wake-up output pin for external Power IC enable pin control.
	RTC_nRWAKE	I	RTC wake-up interrupt Input with internal pull-high. **Note:** Please pull this pin to low if the RTC wake-up interrupt function is unused. In this condition, user also needs to disable the PWRST bit (RTC_PWRCTL[6]) of the RTC Power Control Register by clearing it for saving the RTC power consumption.
	V_{BAT}	P	3.3V power supply by batteries for RTC. **Note:** PH.8~PH.9, RTC_RPWR, RTC_nRWAKE, X32_IN and X32_OUT are belong to this power domain.
	X32_IN	I	External 32.768 kHz crystal input pin.
	X32_OUT	O	External 32.768 kHz crystal output pin.
V_{DDIO}	V_{DDIO0}	P	3.3V digital power supply for I/O group 0. **Note:** nRESET, HSUSB0_ID, PF.15 and PL.12~PL.15 are belong to this power domain.
	V_{DDIO1}	P	3.3V digital power supply for I/O group 1. **Note:** PA.0~PA.15, PD.6~PD.15, PE.14~PE.15, PG.0~PG.7, PG11~PG15, PI0~PI.7, PJ.12~PJ.15, PK0~PK.3, PL.0~PL.11 and PM.12~PM.15 are belong to this power domain.
	V_{DDIO2}	P	1.8V ~ 3.3V digital power supply for I/O group 2. **Note:** PK.8~PK.11 and PM.0~PM.11 are belong to this power domain.
	V_{DDIO3}	P	1.8V ~ 3.3V digital power supply for I/O group 3. **Note:** PJ.0~PJ.11 are belong to this power domain.
	V_{DDIO4}	P	1.8V ~ 3.3V digital power supply for I/O group 4. **Note:** PC.12~PC.15, PG.8~PG.10, PH.0~PH.7, PH.12~PH.15, PI.8~PI.15 and PK.4~PK.7 are belong to this power domain.
	V_{DDIO5}	P	1.8V ~ 3.3V digital power supply for I/O group 5. **Note:** PD.0~PD.5 are belong to this power domain.
	V_{DDIO6}	P	3.3V digital power supply for I/O group 6. **Note:** PC.0~PC.7 are belong to this power domain.
	V_{DDIO7}	P	1.8V ~ 3.3V digital power supply for I/O group 7.

Group	Pin Name	Type	Description
			Note: PK.12~PK.15, PN.0~PN.7 and PN.10~PN.15 are belong to this power domain.
	V_{DDIO8}	P	1.8V ~ 3.3V digital power supply for I/O group 8. **Note:** PE.0~PE.13 are belong to this power domain.
	V_{DDIO9}	P	1.8V ~ 3.3V digital power supply for I/O group 9. **Note:** PF.0~PF.14 are belong to this power domain.
	V_{DDIO10}	P	3.3V digital power supply for I/O group 10. **Note:** XT1_IN and XT1_OUT are belong to this power domain.
Core	V_{DD_CORE}	P	Digital power supply for digital core logic circuit. **Note:** Please refer to the part number from MA35D1 selection guide to supply the correct voltage on this pin.
CPU	V_{DD_CPU}	P	Digital power supply for Cortex-A35 CPU. **Note:** Please refer to the part number from MA35D1 selection guide to supply the correct voltage on this pin.
OTP	V_{DD_OTP}	P	2.5V digital power supply for OTP.
PLL	V_{DD_PLL1}	P	Low digital power supply for PLL group 1.
Ground	V_{SS}	P	Ground pin for digital circuit.
	EPAD	P	Ground pad for digital circuit.
Crystal	XT1_IN	I	External 24 MHz (high speed) crystal input pin.
	XT1_OUT	O	External 24 MHz (high speed) crystal output pin.
Reset	nRESET	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.

5 BLOCK DIAGRAM

5.1 MA35D1 Series Block Diagram

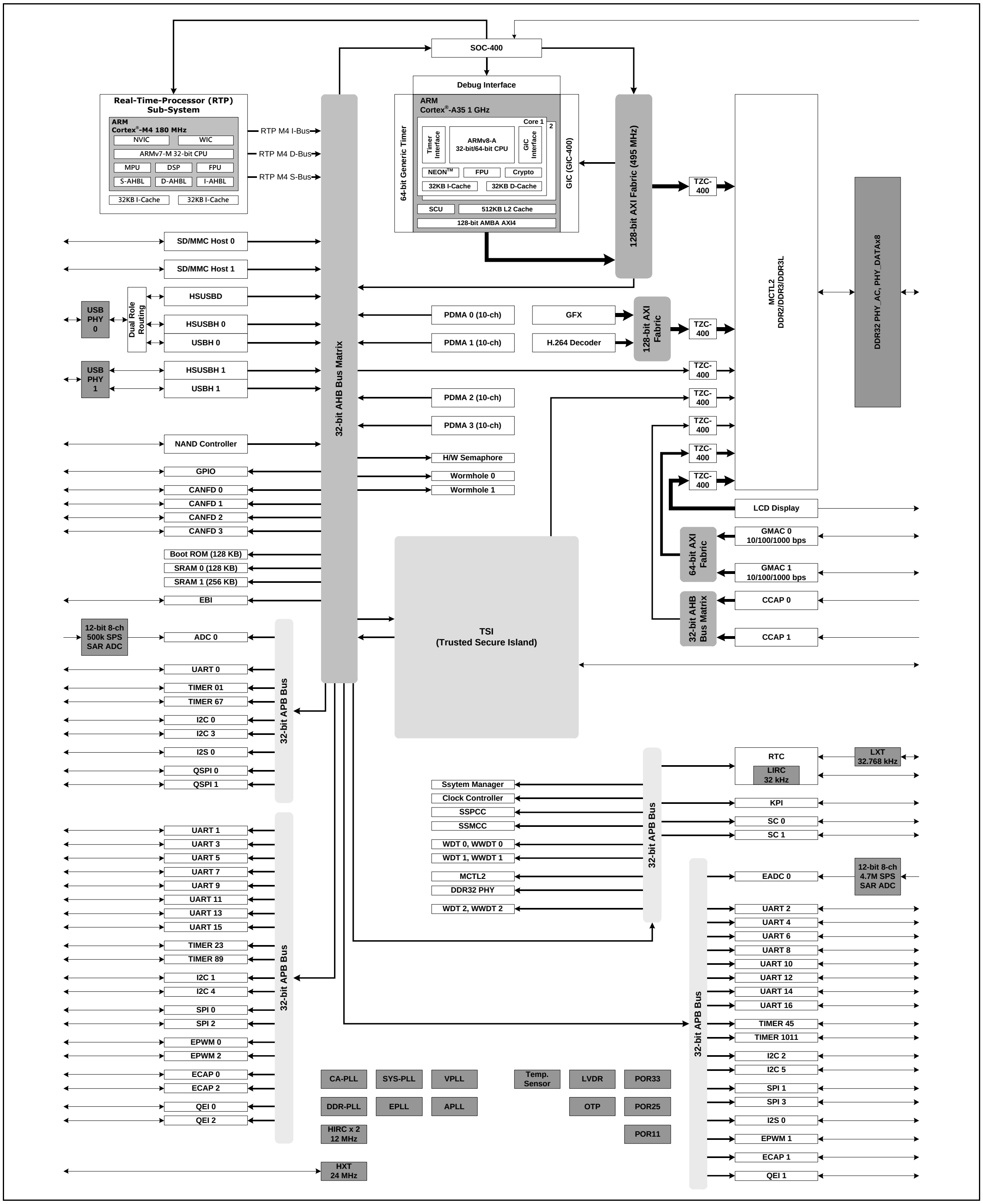


Figure 5-1 MA35D1 Series Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 Arm Cortex-A35 Core

6.1.1 Overview

The Cortex-A35 core is designed to give mid-range instruction execution performance with low power consumption.

In MA35D1 series, the Cortex-A35 core cluster consists of two ARMv8-A compliant cores with 32 KB instruction and 32 KB data L1 cache each, a shared 512 KB L2 cache with Snoop Control Unit (SCU)-L2 cache protection and a 128-bit AXI system bus interface.

For more detailed information, please refer to the "*ARM® Cortex-A35 Processor Technical Reference Manual*" and "*ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile*".

6.1.2 Features

In MA35D1 series, the Cortex-A35 core includes the following features:

- Full implementation of the ARMv8-A A64, A32, and T32 instruction sets.
- Support both the AArch32 and AArch64 execution states at all Exception levels (EL0 to EL3).
- Support in-order pipeline with direct and indirect branch prediction.
- Separate Level 1 (L1) data and instruction side memory systems with a Memory Management Unit (MMU).
  - The MA35D1 series configured with 32 KB instruction and 32 KB data cache.
- Level 2 (L2) memory system with Snoop Control Unit (SCU)-L2 cache protection that provides cluster memory coherency.
  - The MA35D1 series configured with 512 KB shared L2 cache.
- TrustZone.
- Data engine that implements the NEON SIMD and FPU support.
- Cryptographic Extension.
- ARMv8 debug logic.
- Performance Monitoring Unit (PMU).
- Embedded Trace Macrocell (ETM) that supports instruction trace only.
- Generic Interrupt Controller (GIC) CPU interface to connect to an external distributor.
- Generic Timers supporting 64-bit count input from an external system counter.

6.2 Arm Cortex-M4 Core

6.2.1 Overview

The Cortex-M4 core, a configurable, multistage, 32-bit RISC processor, has three AMBA AHB-Lite interfaces for best parallel performance and includes an NVIC component. The processor with optional hardware debug functionality can execute Thumb code and is compatible with other Cortex-M profile processors. The profile supports two modes ,–the Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. The Cortex-M4F core is a processor with the same capability as the Cortex-M4 core and includes floating point arithmetic functionality. The NuMicro MA35D1 series is embedded with Cortex-M4F core. Throughout this document, the name Cortex-M4 refers to both Cortex-M4 and Cortex-M4F cores.

6.2.2 Features

- A low gate count processor core, with low latency interrupt processing that has:
  - A subset of the Thumb instruction set, defined in the ARMv7-M Architecture Reference Manual
  - Banked Stack Pointer (SP)
  - Hardware integer divide instructions, SDIV and UDIV
  - Handler and Thread modes
  - Thumb and Debug states
  - Support for interruptible-continued instructions LDM, STM, PUSH, and POP for low interrupt latency
  - Automatic processor state saving and restoration for low latency Interrupt Service Routine (ISR) entry and exit
  - Support for ARMv7 big-endian byte-invariant or little-endian accesses
  - Support for ARMv7 unaligned accesses
- Floating Point Unit (FPU) in the Cortex-M4F processor providing:
  - 32-bit instructions for single-precision (C float) data-processing operations
  - Combined Multiply and Accumulate instructions for increased precision (Fused MAC)
  - Hardware support for conversion, addition, subtraction, multiplication with optional accumulate, division, and square-root
  - Hardware support for denormals and all IEEE rounding modes
  - 32 dedicated 32-bit single precision registers, also addressable as 16 double-word registers
  - Decoupled three stage pipeline
- Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing. Features include:
  - External interrupts. Configurable from 1 to 240 (the NuMicro MA35D1 series configured with 111 interrupts)
  - Bits of priority, configurable from 3 to 8

- Dynamic reprioritization of interrupts
- Priority grouping which enables selection of preempting interrupt levels and nonpreempting interrupt levels
- Support for tril-chaining and late arrival of interrupts, which enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
- Processor state automatically saved on interrupt entry, and restored on interrupt exit with on instruction overhead
- Support for Wake-up Interrupt Controller (WIC) with Ultra-low Power Sleep mode

- Memory Protection Unit (MPU). An optional MPU for memory protection, including:
  - Eight memory regions
  - Sub Region Disable (SRD), enabling efficient use of memory regions
  - The ability to enable a background region that implements the default memory map attributes
- Low-cost debug solution that features:
  - Debug access to all memory and registers in the system, including access to memory mapped devices, access to internal core registers when the core is halted, and access to debug control registers even while SYSRESETn is asserted.
  - Serial Wire Debug Port(SW-DP) or Serial Wire JTAG Debug Port (SWJ-DP) debug access
  - Optional Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and code patches
  - Optional Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data tracing, and system profiling
  - Optional Instrumentation Trace Macrocell (ITM) for support of printf() style debugging
  - Optional Trace Port Interface Unit (TPIU) for bridging to a Trace Port Analyzer (TPA), including Single Wire Output (SWO) mode
  - Optional Embedded Trace Macrocell (ETM) for instruction trace.
- Bus interfaces:
  - Three Advanced High-performance Bus-Lite (AHB-Lite) interfaces: ICode, Dcode, and System bus interfaces
  - Private Peripheral Bus (PPB) based on Advanced Peripheral Bus (APB) interface
  - Bit-band support that includes atomic bit-band write and read operations.
  - Memory access alignment
  - Write buffer for buffering of write data
  - Exclusive access transfers for multiprocessor systems

6.3 Arm TrustZone for Armv8-A

6.3.1 Overview

Arm TrustZone can be considered as a physical partition that divides the memory system into two worlds: **Secure** world and **Non-secure** world. Each of the world has its resources, such as processor, SRAM, DRAM, GPIO and other peripherals. The Non-secure world, in general, is a rich execution environment (REE) executing complex and various software applications. The Secure world is an isolated execution environment, in which resources are protected and cannot be accessed directly by master in Non-secure world. It is typically used to provide trusted execution environment (TEE) to run trusted software.

A TrustZone-aware PE (processing element), such as Cortex-A35 processor core, can behave as a Secure master or Non-secure master depending on its security state. When the processor is in Secure state, it is a Secure master and can access resources in both Secure world and Non-secure world; while the processor is in Non-secure state, it is a Non-secure master and can access resources in Non-secure world only.

6.3.2 TrustZone of Cortex-A35 Processor

Cortex-A35 is a processor implementing Armv8-A architecture. As depicted in Table 6.3-1, the Cortex-A35 has four exception levels (EL) and two security states. Lower exception level indicates lower privilege. That is, EL3 has the highest permission and can access all resources in the system, while EL0 can only access restricted resources that is managed by EL1, EL2 or EL3. The security state decides whether the PE is currently executed as Secure or Non-secure.

Following TrustZone architecture, Cortex-A35 PE has Secure EL0, EL1 and EL3 (denoted to S.EL0, S.EL1 and S.EL3) and Non-secure EL0, EL1, EL2 (denoted to NS.EL0, NS.EL1 and NS.EL2). Each of them is designed for different function of software. For example, the Linux OS is usually executed at NS.EL1, and user application is executed at NS.EL0. Thus, Linux OS is able to manage the resource for all user applications.

When the PE runs at EL3, it is always in Secure state, denoted as S.EL3. When the PE runs in other exception level, it can be in Secure state or Non-secure state. The security state of the PE is set by SCR_EL3.NS bit, which can be set by S.EL3 software only. In other words, the security state of PE can be changed by S.EL3 software only.

Security State / **Exception Level**	**Secure**		**Non-Secure**	
EL0	S.EL0	Trusted App.	NS.EL0	App.
EL1	S.EL1	Trusted OS (e.g. OPTEE)	NS.EL1	Rich OS (e.g. Linux)
EL2	S.EL2	-	NS.EL2	Hypervisor
EL3	S.EL3	Secure monitor	-	-

Table 6.3-1 Cortex-A35 AArch64 Exception Levels vs. Security States and Typical Function of Each State

6.3.2.1 *Address Space Partition of Armv8-A*

Armv8-A memory system is Virtual Memory System Architecture, VMSA, which means the memory system of Cortex-A35 processor has virtual address (VA) and physical address (PA) and uses memory management unit (MMU) to map VA to PA.

When MMU is enabled, software executed by Cortex-A35 uses VA to access the memory system and MMU uses translation table to map the VA to PA; When MMU is disabled, software uses PA to access the system directly. TrustZone separates the physical memory to Secure space and Non-secure space. The VA of Secure software can be translated to Secure or Non-secure physical address space, while the VA of Non-secure software is always translated to Non-secure physical address space. Thus, Non-secure software can only see Non-secure resources, but can never see Secure resources.

To learn more about TrustZone of Armv8-A, refer to the section 3 “TrustZone in the processor” of the Arm document “TrustZone for Armv8-A”, ARM062-1010708621-28, for more details.

6.3.3 TrustZone System Architecture (SSMCC, SSPCC)

The TrustZone architecture of Cortex-A35 makes the software to view the memory system as Secure world and Non-secure world. However, the TrustZone physical partition is not just all about that. It requires support of the system. As shown in Figure 6-1 the system of this chip, including system bus, bus masters and bus slaves, supports TrustZone.

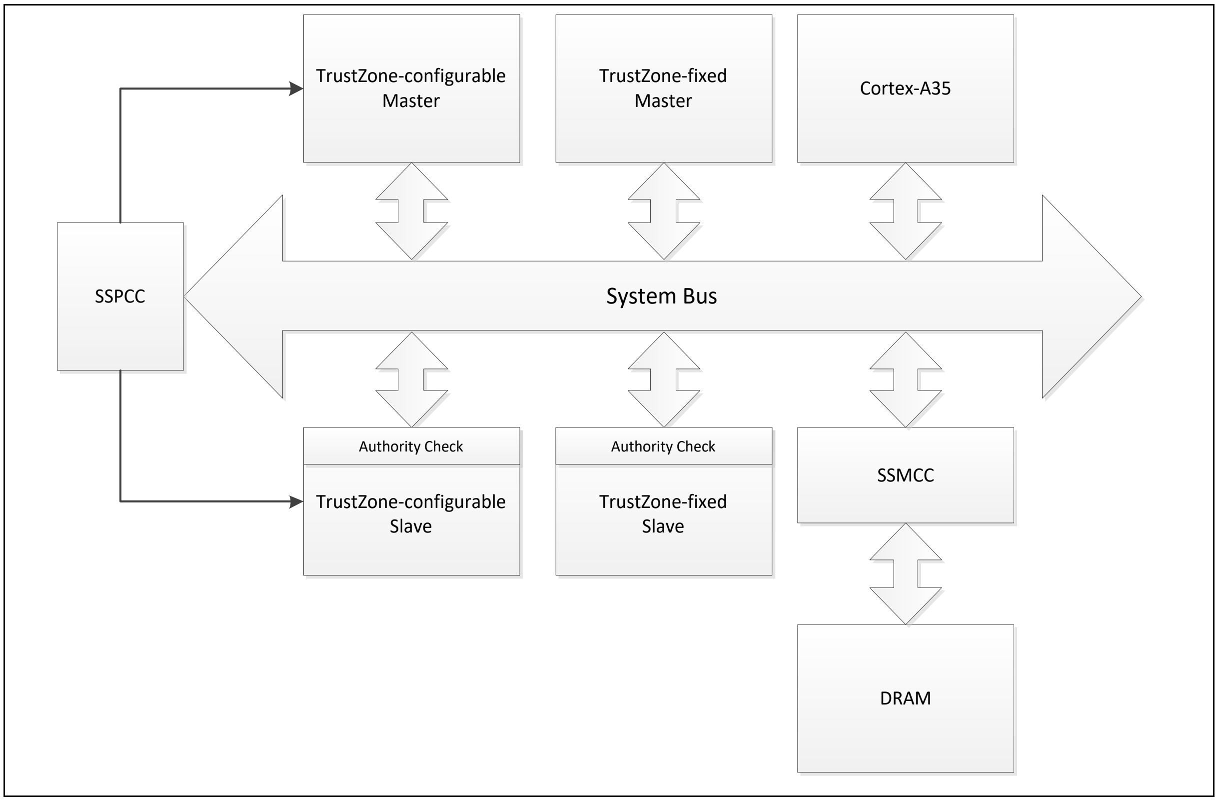


Figure 6-1 TrustZone System Architecture Block Diagram

The system bus takes charge of transferring information between masters and slaves. For each transaction, the system bus transfers the information indicating the security state of the bus master to bus slave, so that the bus slave can do the authority check based on the information.

6.3.3.1 *Security Attribute Configuration*

Bus masters include processors and master peripherals, such as PDMA and GMAC. Except Cortex-A35 processor, whose security state depends on the current exception level and the value of SCR_EL3.NS bit, masters’ security state can be configured by SSPCC (TrustZone-configurable) or be fixed (TrustZone-fixed) to either Secure or Non-secure. For example, PDMA0 can be configured to Secure or Non-secure by SSPCC while GMAC is fixed to Non-secure. Refer to SSPCC section for more details.

A Secure master can access Secure slave and Non-secure slave, while a Non-secure master can only access Non-secure slave. If the Non-secure master tries to access a Secure slave, it will not pass the authority check and will get error response from the slave.

Most of the peripherals in the system are bus slaves, which, similar to bus masters, are also TrustZone-configurable or TrustZone-fixed. Secure software can set the security state of TrustZone-configurable slaves through SSPCC.

The normal memory in the system is also TrustZone-configurable:

- SRAM can be partitioned to Secure or Non-secure regions by setting the boundary through SSPCC.
- DRAM can be partitioned to Secure or Non-secure regions through SSMCC.

Refer to SSPCC and SSMCC section for more details.

6.3.3.2 *Authority Check and Violation Report*

For each transaction, the bus slave will perform the authority check based on the memory access policy, which is:

- Non-secure slave accepts access from both Secure and Non-secure master.
- Secure slave accepts access from Secure master.
- Secure slave will report the violation access event and reply error response when receiving the access from Non-secure master.

The SSPCC receives violation access event from Secure slaves and further generates interrupt to notify the Cortex-A35 if interrupt is enabled.

Unlike other bus slaves, the authority check of DRAM is performed by SSMCC. All transactions to access DRAM will be checked by SSMCC based on the memory access policy. The Secure software should configure SSMCC properly before using DRAM.

6.3.3.3 *Partition Beyond TrustZone*

Apart from TrustZone architecture, this chip has a scale-configurable subsystem for real time processing, called subM system, which is an operating environment for the real-time processor: Cortex-M4. Similar to TrustZone architecture of this chip, some resources are fixed to that subsystem and some resources are configurable. Refer to SSPCC section for more details.

6.4 System Manager

6.4.1 Overview

The system management describes following information and functions.

- System Resets
- System Power Architecture
- System Memory Map
- System Control Registers for Product Identifier (PDID), Power-On Setting, Reset Control for on-chip controllers/peripherals, pin multi-function control and miscellaneous function control.

6.4.2 System Reset

The system reset can be issued by one of the following listed events. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset sources are from peripheral signals while software reset can trigger reset through setting control registers.

- Hardware Reset Sources to reset chip
  - Power-On Reset
  - Low Voltage Reset (LVR)
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
- Hardware Reset Sources to reset RTP Cortex-M4 core
  - RTP Cortex-M4 CPU Lockup Reset
- Software Reset Sources to reset chip
  - CHIP Reset to reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
- Software Reset Sources to reset Cortex-A35 core
  - CPU Reset for Cortex-A35 core 0 only by writing 1 to CA35CR0RST (SYS_IPRST0[1])
  - Warm Reset request for Cortex-A35 core 0 only by writing 1 to the bit RR (RMR[1])
  - CPU Reset for Cortex-A35 core 1 only by writing 1 to CA35CR1RST (SYS_IPRST0[2])
  - Warm Reset request for Cortex-A35 core 1 only by writing 1 to the bit RR (RMR[1])
- Software Reset Sources to reset RTP Cortex-M4 core
  - CPU Reset for RTP Cortex-M4 core only by writing 1 to CM4RST (SYS_IPRST0[3])
  - CPU Reset for RTP Cortex-M4 core only by writing 1 to the bit SYSRESETREQ (AIRCR[2])

6.4.2.1 *Power-On Reset (POR)*

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MPU. When applying the power to MPU, the POR module detects the rising voltage and generates reset signal to system until the voltage is ready for MPU operation. At POR reset, the PORF (SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF (SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6-2 shows the power-on reset waveform.

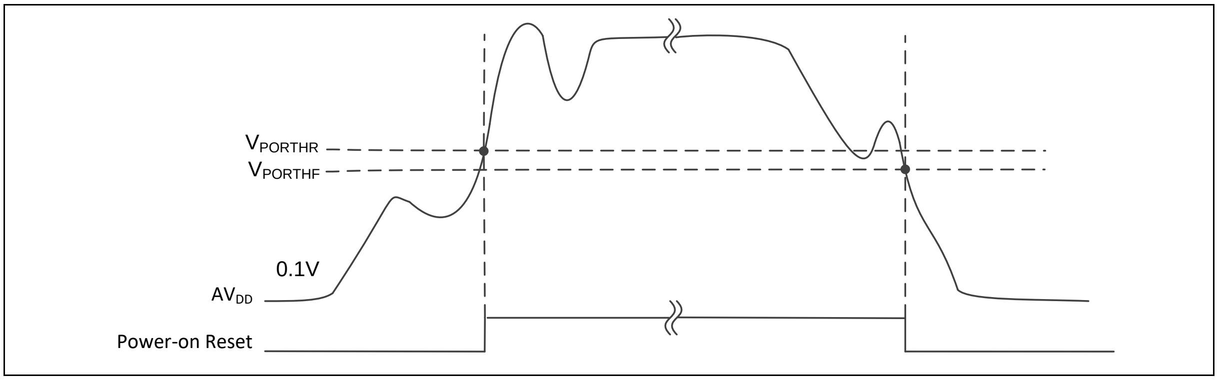


Figure 6-2 Power-on Reset (POR) Waveform

6.4.2.2 *Low Voltage Reset (LVR)*

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_LVRDCR[0]) to 1, after 200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_LVRDCR[3:1]), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_LVRDCR[3:1]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6-3 shows the Low Voltage Reset waveform.

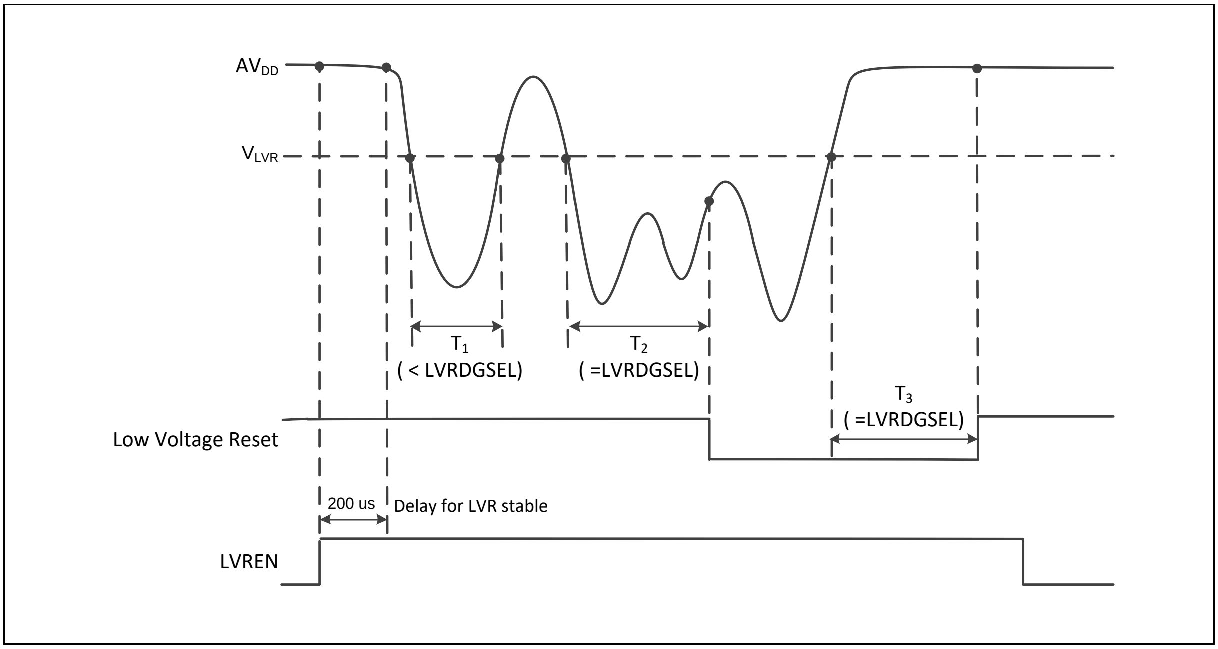


Figure 6-3 Low Voltage Reset (LVR) Waveform

6.4.2.3 *Pin nRESET Reset*

The nRESET reset means to generate a reset signal by pulling nRESET pin low, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 V_{DDIO0} and the state keeps longer than 100 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 V_{DDIO0} and the state keeps longer than 100 us (glitch filter). The PINRF (SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6-4 shows the nRESET reset waveform.

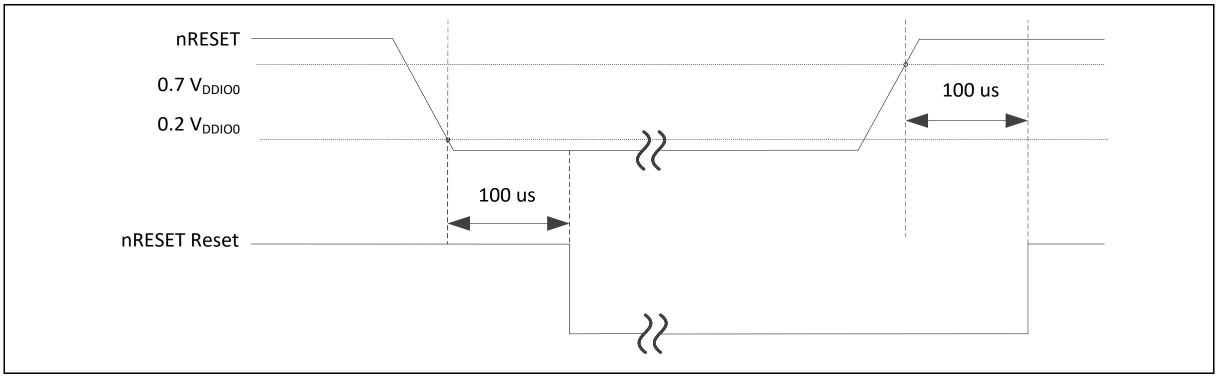


Figure 6-4 nRESET Reset Waveform

6.4.2.4 *Watchdog Timer Reset (WDT)*

In most industrial applications, system reliability is quite important. Recovering the system from failure status automatically is one way to improve system reliability. The watchdog timer (WDT) is widely used to check if the system works fine. If the system is crashed or out of control, it may cause the WDT time-out. User may decide to enable system reset during WDT time-out to recover the system and take action for the system crash/out-of-control after reset.

The MA35D1 series is equipped with three WDTs: WDT0, WDT1 and WDT2. The WDT0 is for TrustZone Secure (TZS), WDT1 is for TrustZone Secure/Non-Secure (TZS/TZNS) and WDT2 is for SubM.

The WDT0 time-out resets system automatically.

The WDT1 time-out resets Cortex-A35 core and controllers/peripherals configured in TZS/TZNS only when WDT1RSTAEN (SYS_MISCRFCR[16]) is 1. The WDT1 time-out resets Cortex-M4 core and peripherals configured in SubM only when WDT1RSTAEN (SYS_MISCRFCR[16]) and WDT1RSTMEN (SYS_MISCRFCR[18]) are both 1.

The WDT2 time-out resets Cortex-A35 core and controllers/peripherals configured in TZS/TZNS only when WDT2RSTAEN (SYS_MISCRFCR[17]) is 1. The WDT2 time-out resets Cortex-M4 core and peripherals configured in SubM automatically.

Software can check if the reset is caused by time-out of WDT0, WDT1 or WDT2 to indicate the previous reset is a WDT0, WDT1 or WDT2 reset and handle the failure of system after WDT0, WDT1 or WDT2 time-out reset by checking WDT0RF (SYS_RSTSTS[2]), WDT1RF (SYS_RSTSTS[10]), WDT2RFA (SYS_RSTSTS[11]), WDT1RFM (SYS_RSTSTS[18]) and WDT2RF (SYS_RSTSTS[19]).

6.4.2.5 *RTP Cortex-M4 CPU Lockup Reset*

The RTP Cortex-M4 CPU enters lockup state after RTP Cortex-M4 CPU produces HardFault at HardFault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the RTP Cortex-M4 CPU being locked because of an unrecoverable exception following the activation of the processor's built-in system state protection hardware. When chip enters debug mode, the RTP Cortex-M4 CPU lockup reset will be ignored.

Software can check if the reset is caused by RTP Cortex-M4 CPU entering lockup state to indicate the previous reset is a RTP Cortex-M4 CPU lockup reset by checking RTPM4LKRF (SYS_RSTSTS[20]).

6.4.2.6 *CHIP Reset*

The CHIP Reset is the same with Power-on Reset. The Cortex-A35 core, RTP Cortex-M4 core and controllers/peripherals are reset.

User sets CHIPRST (SYS_IPRST0[0]) to 1 to assert the CHIP Reset.

6.4.2.7 *Cortex-A35 processor CPU Reset and Warm Reset*

The Cortex-A35 processor CPU Reset means that only Cortex-A35 core is reset and all other controllers/peripherals remain the same status after CPU reset. User can set CA35CR0RST (SYS_IPRST0[1]) and CA35CR1RST (SYS_IPRST0[2]) to 1 to assert CPU Reset to Cortex-A35 core 0 and 1 respectively.

The Cortex-A35 processor Warm Reset requests a warm reset for Cortex-A35 core. User can set the bit RR (RMR[1]) of Cortex-A35 core 0 and 1 to assert Warm Reset to Cortex-A35 core 0 and 1 respectively.

6.4.2.8 *RTP Cortex-M4 processor CPU Reset*

The RTP Cortex-M4 processor CPU Reset means that only RTP Cortex-M4 core is reset and all other peripherals remain the same status after CPU reset. User can set the bit CM4RST (SYS_IPRST0[3]) or SYSRESETREQ (AIRCR[2]) to 1 to assert CPU Reset to RTP Cortex-M4 core.

6.4.3 System Power Distribution

In this chip, the power distribution is divided into several segments.

- Analog power from AV_{DD} provides 3.3V voltage to analog components operation. These analog components including POR33, LVR and Temperature Sensor.
- Analog power from AV_{DD_EADC0} provides 3.3V voltage to 12-bit 4.7 MSPS SAR-ADC.
- Analog power from AV_{DD_ADC0} provides 3.3V voltage to 12-bit 500k SPS SAR-ADC.
- Analog power from V_{DD_OTP} provides 2.5V voltage to POR25 and OTP memory.
- Power provides voltage to PLL and internal RC oscillator including:
  - AV_{DDL_PLL0} provides 1.1V voltage to CA-PLL and SYS-PLL.
  - AV_{DDL_PLL1} and AV_{DDH_PLL1} provide 1.1V and 3.3V voltage respectively to DDR-PLL.
  - V_{DD_PLL1} provides 1.1V voltage to DDR-PLL, EPLL, APLL and VPLL.
  - AV_{DDL_PLL2} and AV_{DDH_PLL2} provide 1.1V and 3.3V voltage respectively to EPLL, APLL and VPLL.
  - AV_{DDL_ROSC} provides 1.1V voltage to two 12 MHz RC oscillators (HIRC).
- Power provides voltage to a DDR32 PHY_AC macro, two DDR32 PHY_DATX8 macro and SSTL I/O including:
  - MV_{DD} provides 1.35V, 1.5V or 1.8V when SDRAM connected is DDR3L, DDR3 or DDR2 type.
  - $MV_{DD\_DPHYPLL}$ provides 2.5V voltage to PLL of DDR32 PHY_AC and PHY_DATX8 macros.
  - MV_{REF_CA} provides MV_{DD}/2 voltage to DDR32 PHY_AC macro and address, command SSTL I/O as a reference voltage.
  - MV_{REF_DQ} provides MV_{DD}/2 voltage to DDR32 PHY_DATX8 macros and data SSTL I/O as a reference voltage.
- Power from V_{DD_HSUSB0} and V_{DD_HSUSB1} provide 3.3V voltage to USB 2.0 PHY 0 and USB 2.0 PHY 1 respectively while V_{DD_CORE} provides 1.1V voltage to both USB 2.0 PHY 0 and USB 2.0 PHY 1.
- Power from V_{BAT} provides 3.3V voltage to 32.768 kHz Crystal Oscillator (LXT), 32 kHz RC oscillator (LIRC), LVR and RTC logic.
- Digital power from V_{DD_CPU} provides 1.1/1.2V voltage to dual Arm Cortex-A35 core, L1 Instruction/Data cache and L2 cache SRAM.
- Digital power from V_{DD_CORE} provides 1.1V voltage to POR11, ROM, SRAM and all digital logic.
- Power from V_{DDIO0}, V_{DDIO1}, V_{DDIO2}, V_{DDIO3}, V_{DDIO4}, V_{DDIO5}, V_{DDIO6}, V_{DDIO7}, V_{DDIO8}, V_{DDIO9} and V_{DDIO10} provides 1.8V or 3.3V voltage to 24 MHz Crystal Oscillator (HXT) and I/O pins (PA ~ PN).

Figure 6-5 shows the power distribution of the MA35D1 series.

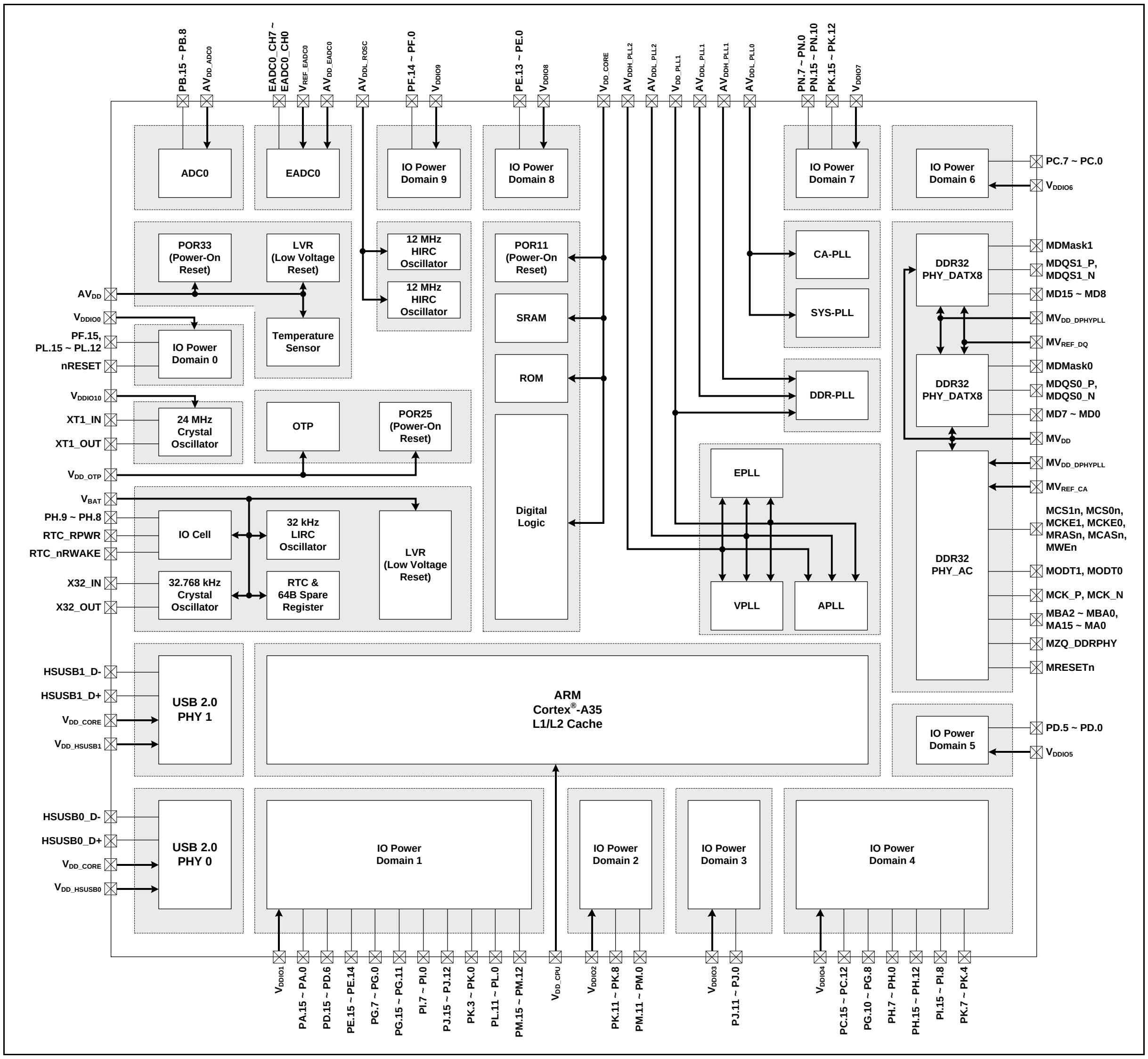


Figure 6-5 MA35D1 Series Power Distribution Diagram

6.4.4 Memory Organization

This chip supports only little-endian data format and provides 4G-byte addressing space. Some parts of memory space have different definitions for Cortex-A35 and RTP Cortex-M4 core. Figure 6-6 describes the detailed memory space definition.

The DDR SDRAM address space 0x8002_0000 ~ 0x803F_FFFF is aliased to 0x0002_0000 ~ 0x003F_FFFF in memory space view of RTP Cortex-M4 core. This address space aliasing also applies to PDMA 2 and PDMA 3.

The reserved memory space is un-accessible. Chip's behavior is undefined and unpredictable while accessing to reserved memory space.

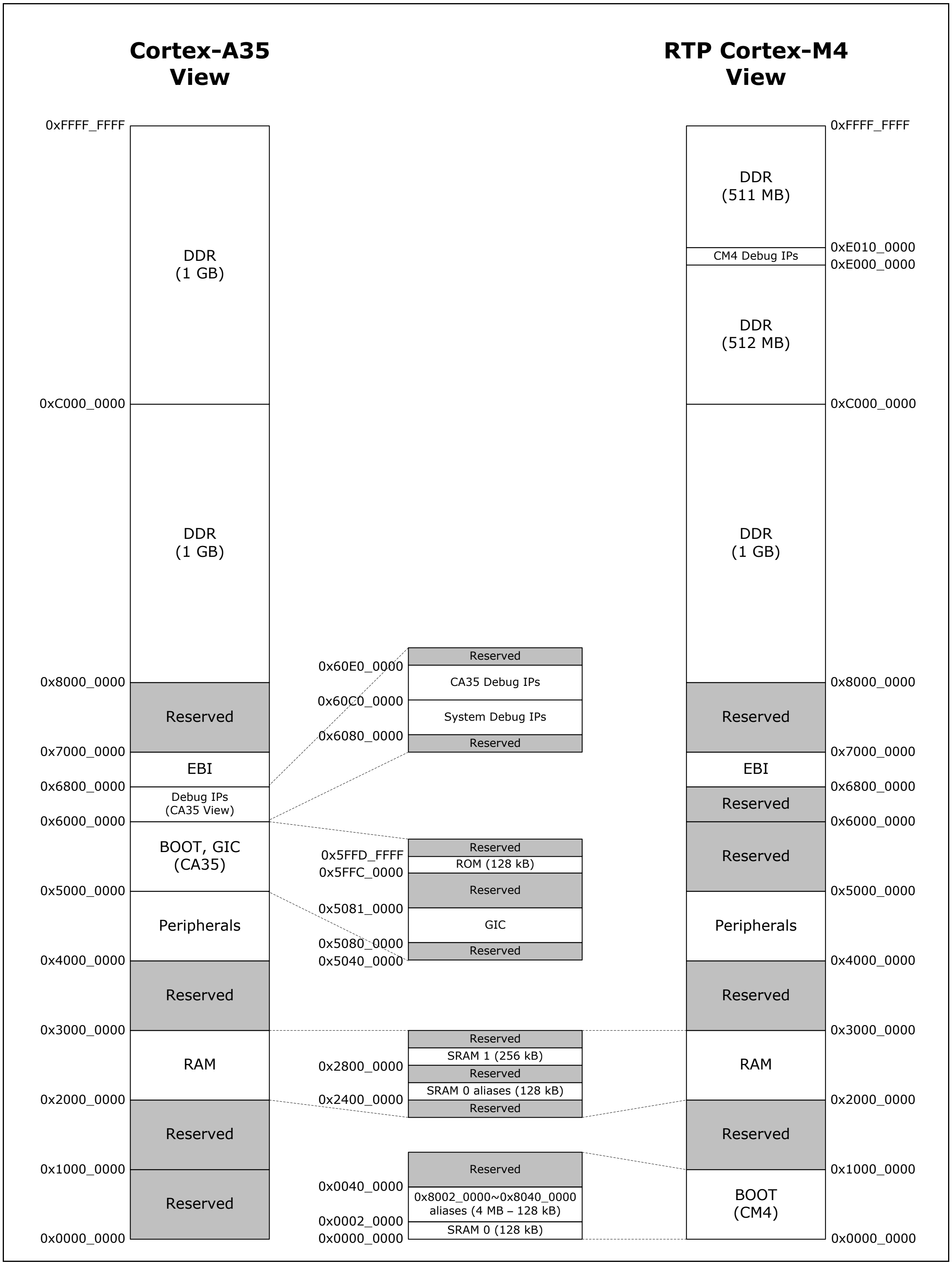

Cortex-A35 View
RTP Cortex-M4 View
0xFFFF_FFFF
DDR (1 GB)
0xC000_0000
DDR (1 GB)
0x8000_0000
Reserved
0x7000_0000
EBI
0x6800_0000
Debug IPs (CA35 View)
0x6000_0000
BOOT, GIC (CA35)
0x5000_0000
Peripherals
0x4000_0000
Reserved
0x3000_0000
RAM
0x2000_0000
Reserved
0x1000_0000
Reserved
0x0000_0000
Reserved
0x60E0_0000
CA35 Debug IPs
0x60C0_0000
System Debug IPs
0x6080_0000
Reserved
Reserved
0x5FFD_FFFF
ROM (128 kB)
0x5FFC_0000
Reserved
0x5081_0000
GIC
0x5080_0000
Reserved
0x5040_0000
Reserved
SRAM 1 (256 kB)
0x2800_0000
Reserved
SRAM 0 aliases (128 kB)
0x2400_0000
Reserved
Reserved
0x0040_0000
0x8002_0000~0x8040_0000 aliases (4 MB – 128 kB)
0x0002_0000
SRAM 0 (128 kB)
0x0000_0000
DDR (511 MB)
0xE010_0000
CM4 Debug IPs
0xE000_0000
DDR (512 MB)
0xC000_0000
DDR (1 GB)
0x8000_0000
Reserved
0x7000_0000
EBI
0x6800_0000
Reserved
0x6000_0000
Reserved
0x5000_0000
Peripherals
0x4000_0000
Reserved
0x3000_0000
RAM
0x2000_0000
Reserved
0x1000_0000
BOOT (CM4)
0x0000_0000

Figure 6-6 MA35D1 System Memory Map Diagram

The addressing space assigned to each on-chip controller or peripheral described in Table 6.4-1. The detailed register definition, addressing space, and programming details will be described in the following sections.

Address Space	Token	Controllers
SRAM, SDRAM, External Memory and IBR (Internal Boot ROM) Space		
0x0000_0000 - 0x0001_FFFF	SRAM0_BA	SRAM 0 Memory Space (128 KB)
0x0002_0000 - 0x003F_FFFF	SDRAM4M_BA	SDRAM Address 0x8002_0000~0x8040_0000 Alias Memory Space (4 MB-128 KB)
0x2400_0000 - 0x2403_FFFF	SRAM0A_BA	SRAM 0 Alias Memory Space (256 KB)
0x2800_0000 - 0x2803_FFFF	SRAM1_BA	SRAM 1 Memory Space (256 KB)
0x5FFC_0000 - 0x5FFF_FFFF	IBR_BA	Internal Boot ROM Space (128 KB)
0x6800_0000 - 0x6FFF_FFFF	EXTMEM_BA	External Memory Space (128 MB)
0x8000_0000 - 0xFFFF_FFFF	SDRAM_BA	SDRAM Memory Space (2GB)
AXI/AHB Peripheral Register Space		
0x4004_0000 – 0x4004_0FFF	GPIO_BA	GPIO Control Registers
0x4008_0000 – 0x4008_0FFF	PDMA0_BA	Peripheral DMA 0 Control Registers
0x4009_0000 – 0x4009_0FFF	PDMA1_BA	Peripheral DMA 1 Control Registers
0x400A_0000 – 0x400A_0FFF	PDMA2_BA	Peripheral DMA 2 Control Registers
0x400B_0000 – 0x400B_0FFF	PDMA3_BA	Peripheral DMA 3 Control Registers
0x4010_0000 – 0x4010_0FFF	EBI_BA	External Bus Interface Control Registers
0x4012_0000 – 0x4012_0FFF	GMAC0_BA	Gigabit Ethernet MAC 0 Control Registers
0x4013_0000 – 0x4013_0FFF	GMAC1_BA	Gigabit Ethernet MAC 1 Control Registers
0x4014_0000 – 0x4014_0FFF	HSUSBH0_BA	HSUSBH Host 0 Control Registers
0x4015_0000 – 0x4015_0FFF	USBH0_BA	USBH Host 0 Control Registers
0x4018_0000 – 0x4018_0FFF	SDH0_BA	SD 3.0 HOST 0 Control Registers
0x4019_0000 – 0x4019_0FFF	SDH1_BA	SD 3.0 HOST 1 Control Registers
0x401A_0000 – 0x401A_0FFF	NAND_BA	NAND Flash Memory Control Registers
0x401C_0000 – 0x401C_0FFF	HSUSBH1_BA	HSUSBH Host 1 Control Registers
0x401D_0000 – 0x401D_0FFF	USBH1_BA	USBH Host 1 Control Registers
0x4020_0000 – 0x4023_FFFF	HSUSBD_BA	HSUSBD Control Registers
0x4024_0000 – 0x4024_0FFF	CCAP0_BA	CCAP 0 Control Registers
0x4025_0000 – 0x4025_0FFF	CCAP1_BA	CCAP 1 Control Registers
0x4026_0000 – 0x4026_0FFF	DISP_BA	LCD Display Control Registers
0x4028_0000 – 0x4028_0FFF	GFX_BA	Graphic Control Registers

0x4029_0000 – 0x4029_0FFF	VDEC_BA	Video Decoder Control Registers
0x4038_0000 – 0x4038_0FFF	HWSEM0_BA	Hardware Semaphore 0 Control Registers
0x403A_0000 – 0x403A_0FFF	WRHO0_BA	Wormhole 0 Control Registers
0x403C_0000 – 0x403C_0FFF	CANFD0_BA	CANFD 0 Control Registers
0x403D_0000 – 0x403D_0FFF	CANFD1_BA	CANFD 1 Control Registers
0x403E_0000 – 0x403E_0FFF	CANFD2_BA	CANFD 2 Control Registers
0x403F_0000 – 0x403F_0FFF	CANFD3_BA	CANFD 3 Control Registers
0x503B_0000 – 0x503B_0FFF	WRHO1_BA	Wormhole 1 Control Registers
0x5080_0000 – 0x5080_7FFF	GIC_BA	Generic Interrupt Control Registers
APB Peripheral Register Space		
0x4040_0000 – 0x4040_0FFF	WDT0_BA	Watchdog Timer 0 Control Registers
0x4041_0000 – 0x4041_0FFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4042_0000 – 0x4042_0FFF	ADC0_BA	Analog-Digital-Converter 0 (ADC0) Control Registers
0x4043_0000 – 0x4043_0FFF	EADC0_BA	Enhanced Analog-Digital-Converter 0 (EADC0) Control Registers
0x4044_0000 – 0x4044_0FFF	WDT1_BA	Watchdog Timer 1 Control Registers
0x4046_0000 – 0x4046_01FF	SYS_BA	System Control Registers
0x4046_0200 – 0x4046_02FF	CLK_BA	Clock Control Registers
0x4046_0300 – 0x4046_03FF	NMI_BA	NMI Control Registers
0x4048_0000 – 0x4048_0FFF	I2S0_BA	I^2S 0 Interface Control Registers
0x4049_0000 – 0x4049_0FFF	I2S1_BA	I^2S 1 Interface Control Registers
0x404A_0000 – 0x404A_0FFF	KPI_BA	KeyPad Interface Control Registers
0x404C_0000 – 0x404C_0FFF	DDRPHY_BA	DDR PHY PUB Control Registers
0x404D_0000 – 0x404D_0FFF	UMCTL2_BA	DDR (MCTL2) Control Registers
0x404E_0000 – 0x404E_0FFF	SSMCC_BA	SSMCC Control Registers
0x404F_0000 – 0x404F_0FFF	SSPCC_BA	SSPCC Control Registers
0x4050_0000 – 0x4050_0FFF	TMR01_BA	Timer 0 and Timer 1 Control Registers
0x4051_0000 – 0x4051_0FFF	TMR23_BA	Timer 2 and Timer 3 Control Registers
0x4052_0000 – 0x4052_0FFF	TMR45_BA	Timer 4 and Timer 5 Control Registers
0x4053_0000 – 0x4053_0FFF	TMR67_BA	Timer 6 and Timer 7 Control Registers
0x4054_0000 – 0x4054_0FFF	TMR89_BA	Timer 8 and Timer 9 Control Registers
0x4055_0000 – 0x4055_0FFF	TMR1011_BA	Timer 10 and Timer 11 Control Registers
0x4058_0000 – 0x4058_0FFF	EPWM0_BA	EPWM 0 Control Registers
0x4059_0000 – 0x4059_0FFF	EPWM1_BA	EPWM 1 Control Registers
0x405A_0000 – 0x405A_0FFF	EPWM2_BA	EPWM 2 Control Registers

0x4060_0000 – 0x4060_0FFF	SPI0_BA	SPI 0 Control Registers
0x4061_0000 – 0x4061_0FFF	SPI1_BA	SPI 1 Control Registers
0x4062_0000 – 0x4062_0FFF	SPI2_BA	SPI 2 Control Registers
0x4063_0000 – 0x4063_0FFF	SPI3_BA	SPI 3 Control Registers
0x4068_0000 – 0x4068_0FFF	QSPI0_BA	QSPI 0 Control Registers
0x4069_0000 – 0x4069_0FFF	QSPI1_BA	QSPI 1 Control Registers
0x4070_0000 – 0x4070_0FFF	UART0_BA	UART 0 Control Registers
0x4071_0000 – 0x4071_0FFF	UART1_BA	UART 1 Control Registers
0x4072_0000 – 0x4072_0FFF	UART2_BA	UART 2 Control Registers
0x4073_0000 – 0x4073_0FFF	UART3_BA	UART 3 Control Registers
0x4074_0000 – 0x4074_0FFF	UART4_BA	UART 4 Control Registers
0x4075_0000 – 0x4075_0FFF	UART5_BA	UART 5 Control Registers
0x4076_0000 – 0x4076_0FFF	UART6_BA	UART 6 Control Registers
0x4077_0000 – 0x4077_0FFF	UART7_BA	UART 7 Control Registers
0x4078_0000 – 0x4078_0FFF	UART8_BA	UART 8 Control Registers
0x4079_0000 – 0x4079_0FFF	UART9_BA	UART 9 Control Registers
0x407A_0000 – 0x407A_0FFF	UART10_BA	UART 10 Control Registers
0x407B_0000 – 0x407B_0FFF	UART11_BA	UART 11 Control Registers
0x407C_0000 – 0x407C_0FFF	UART12_BA	UART 12 Control Registers
0x407D_0000 – 0x407D_0FFF	UART13_BA	UART 13 Control Registers
0x407E_0000 – 0x407E_0FFF	UART14_BA	UART 14 Control Registers
0x407F_0000 – 0x407F_0FFF	UART15_BA	UART 15 Control Registers
0x4080_0000 – 0x4080_0FFF	I2C0_BA	I^2C 0 Control Registers
0x4081_0000 – 0x4081_0FFF	I2C1_BA	I^2C 1 Control Registers
0x4082_0000 – 0x4082_0FFF	I2C2_BA	I^2C 2 Control Registers
0x4083_0000 – 0x4083_0FFF	I2C3_BA	I^2C 3 Control Registers
0x4084_0000 – 0x4084_0FFF	I2C4_BA	I^2C 4 Control Registers
0x4085_0000 – 0x4085_0FFF	I2C5_BA	I^2C 5 Control Registers
0x4088_0000 – 0x4088_0FFF	UART16_BA	UART 16 Control Registers
0x4090_0000 – 0x4090_0FFF	SC0_BA	Smartcard Host 0 Control Registers
0x4091_0000 – 0x4091_0FFF	SC1_BA	Smartcard Host 1 Control Registers
0x4098_0000 – 0x4098_0FFF	WDT2_BA	Watchdog Timer 2 Control Registers
0x40B0_0000 – 0x40B0_0FFF	QEI0_BA	QEI 0 Control Registers
0x40B1_0000 – 0x40B1_0FFF	QEI1_BA	QEI 1 Control Registers

0x40B2_0000 – 0x40B2_0FFF	QEI2_BA	QEI 2 Control Registers
0x40B4_0000 – 0x40B4_0FFF	ECAP0_BA	ECAP 0 Control Registers
0x40B5_0000 – 0x40B5_0FFF	ECAP1_BA	ECAP 1 Control Registers
0x40B6_0000 – 0x40B6_0FFF	ECAP2_BA	ECAP 2 Control Registers
0x40B9_0000 – 0x40B9_0FFF	TRNG_BA	TRNG Control Registers
Debug IP Register Space		
0x6080_0000 - 0x608F_FFFF	SYSDBG_BA	System Debug IP Control Registers
0x60C0_0000 - 0x60DF_FFFF	A35DBG_BA	Cortex-A35 Debug IP Control Registers
0xE000_0000 - 0xE00F_FFFF	RPTDBG_BA	RTP Cortex-M4 Debug IP Control Registers

Table 6.4-1 Address Space Assignments for On-Chip Controllers

6.4.5 Power-On Setting

After power on reset, Power-On setting registers are latched to configure this chip. The Table 6.4-2 describes the definition of each power-on setting bit.

PWRONSRC (SYS_PWRONOTP[0])		**Description**	
1	0		
SYS_PWRONOTP	SYS_PWRONPIN		
[16]	-	USBP0ID	USB Port 0 ID Pin Status 0 = USB Port 0 act as a USB host. 1 = USB Port 0 act as a USB device. **Note:** The value of USBP0ID always comes from pin HSUSB0_ID.

[15:14]	[7:6]	MISCCFG	Miscellaneous Configuration If BTSRCSEL = 01, Boot from SD/eMMC. MISCCFG[0]: 0 = SD0/eMMC0 booting. (Default) 1 = SD1/eMMC1 booting. MISCCFG[1]: 0 = eMMC 4-bit booting. (Default) 1 = eMMC 8-bit booting. If BTSRCSEL = 10, the Boot from NAND Flash. 00 = Ignore. 01 = ECC is BCH T12. 10 = ECC is BCH T24. 11 = No ECC. If BTSRCSEL = 00, the Boot from SPI Flash. 00 = SPI-NAND Flash with 1-bit mode booting (Default). 10 = SPI-NOR Flash with 1-bit mode booting. If BTSRCSEL = 11, the Boot from USB. X0 = over-current low active detect. X1 = over-current high active detect. **Note:** If PWRONSRC = 0, the value of pin PG[7:6] latched to MISCCFG when pin nRESET transited from low to high. If PWRONSRC = 1, the value of MISCCFG latched from OTP's BTOPTION.
[13:12]	[5:4]	NPAGESEL	If BTSRCSEL = 10, the Boot from NAND Flash, these two bits indicates NAND Flash Page Size Selection. 00 = ignore. 01 = NAND Flash page size is 2 KB. 10 = NAND Flash page size is 4 KB. 11 = NAND Flash page size is 8 KB. If BTSRCSEL = 11, the Boot from USB, these two bits indicates USB Role and Port Selection. 00 = USBD booting. 01 = USBH port 0 boot. 10 = USBD booting. 11 = USBH port 1 boot. **Note:** If PWRONSRC = 0, the value of pin PG[5:4] latched to NPAGSEL when pin nRESET transited from low to high. If PWRONSRC = 1, the value of NPAGSEL latched from OTP's BTNANDPS.

[11:10]	[3:2]	BTSRCSEL	Boot Source Selection 00 = Boot from SPI Flash (Default). 01 = Boot from SD/eMMC. 10 = Boot from NAND Flash. 11 = Boot from USB. **Note:** If PWRONSRC = 0, the value of pin PG[3:2] latched to BTSRCSEL when pin nRESET transited from low to high. If PWRONSRC = 1, the value of BTSRCSEL latched from OTP's BTSRCSEL.
[9]	[1]	BTSRCVOL	Boot Source Interface IO Voltage 0 = Boot source interface IO voltage is 3.3V. 1 = Boot source interface IO voltage is 1.8V. **Note:** If PWRONSRC = 0, the value of pin PG[1] latched to BTSRCVOL when pin nRESET transited from low to high. If PWRONSRC = 1, the value of BTSRCVOL latched from OTP's BTSRCVOL.
[8]	[0]	SECBTDIS	Secure Boot Disable Bit 0 = Secure Boot Enabled (Default). 1 = Secure Boot Disabled. **Note:** If PWRONSRC = 0, the value of pin PG[0] latched to SECBTDIS when pin nRESET transited from low to high. If PWRONSRC = 1, the secure boot disable controlled by OTP's SECBTPSWD.
[5]	-	SD0BKEN	SD0 Back Up Boot Enable Bit 0 = SD0 back up boot Disabled (Default). 1 = SD0 back up boot Enabled. **Note:** The value of SD0BKEN always defined by OTP's SD0BKEN.
[4]	-	UR0DBGDIS	UART 0 Debug Message Output Disable Bit 0= UART 0 debug message output Enabled. 1= UART 0 debug message output Disabled. **Note:** The value of UR0DBGDIS always defined by OTP's UR0MSGODIS.
[2]	-	WDT1ON	Watchdog Timer 1 ON/OFF Selection 0 = After power-on, WDT 1 Disabled. 1 = after power-on WDT 1 Enabled. **Note:** The value of WDT1ON always defined by OTP's WDT1EN.
[1]	-	QSPI0CKSEL	QSPI0_CLK Frequency Selection 0 = QSPI0_CLK frequency is 30 MHz. 1 = QSPI0_CLK frequency is 50 MHz. **Note:** The value of QSPI0CKSEL always defined by OTP's QSPI0CKF.

Table 6.4-2 Power-On Setting Bit Description

6.4.6 Control Registers Access Attribute

The system manager control registers access attribute are shown in Table 6.4-3.

Register	SYSSIAEN (SSPCC_SINFAEN[1]) =0			SYSSIAEN (SSPCC_SINFAEN[1]) =1		
	TZS	TZNS	SUBM	TZS	TZNS	SUBM
SYS_PDID	R			R		
SYS_PWRONOTP	R			R		
SYS_PWRONPIN	R			R		
SYS_RSTSTS	R/W			R/W		
SYS_MISCRFCR	R/W	R		R/W	R	
SYS_RSTDEBCTL	R/W	R		R/W	R	
SYS_LVRDCR	R/W	R		R/W	R	
SYS_IPRST0	R/W			R/W		
SYS_IPRST1	R/W			R/W		
SYS_IPRST2	R/W			R/W		
SYS_IPRST3	R/W			R/W		
SYS_PMUCR	R/W	R		R/W	R	
SYS_DDRCQCSR	R/W	R		R/W	R	
SYS_PMUIEN	R/W	R		R/W	R	
SYS_PMUSTS	R/W	R		R/W	R	
SYS_CA35WRBADR1	R/W	R		R/W	R	
SYS_CA35WRBPAR1	R/W	R		R/W	R	
SYS_CA35WRBADR2	R/W	R		R/W	R	
SYS_CA35WRBPAR2	R/W	R		R/W	R	
SYS_USBPMISCR	R/W		R	R/W		R
SYS_USBP0PCR	R/W	R		R/W		R
SYS_USBP1PCR	R/W		R	R/W		R
SYS_MISCFCR0	R/W		R	R/W		R
SYS_MISCFCR1	R/W			R/W		
SYS_MISCIER	R/W		R	R/W		R
SYS_MISCISR	R/W		R	R/W		R
SYS_GPA_MFPL	R/W	R		R/W		
SYS_GPA_MFPH	R/W	R		R/W		
SYS_GPB_MFPL	R/W	R		R/W		
SYS_GPB_MFPH	R/W	R		R/W		

SYS_GPC_MFPL	R/W	R		R/W	
SYS_GPC_MFPH	R/W	R		R/W	
SYS_GPD_MFPL	R/W	R		R/W	
SYS_GPD_MFPH	R/W	R		R/W	
SYS_GPE_MFPL	R/W	R		R/W	
SYS_GPE_MFPH	R/W	R		R/W	
SYS_GPF_MFPL	R/W	R		R/W	
SYS_GPF_MFPH	R/W	R		R/W	
SYS_GPG_MFPL	R/W	R		R/W	
SYS_GPG_MFPH	R/W	R		R/W	
SYS_GPH_MFPL	R/W	R		R/W	
SYS_GPH_MFPH	R/W	R		R/W	
SYS_GPI_MFPL	R/W	R		R/W	
SYS_GPI_MFPH	R/W	R		R/W	
SYS_GPJ_MFPL	R/W	R		R/W	
SYS_GPJ_MFPH	R/W	R		R/W	
SYS_GPK_MFPL	R/W	R		R/W	
SYS_GPK_MFPH	R/W	R		R/W	
SYS_GPL_MFPL	R/W	R		R/W	
SYS_GPL_MFPH	R/W	R		R/W	
SYS_GPM_MFPL	R/W	R		R/W	
SYS_GPM_MFPH	R/W	R		R/W	
SYS_GPN_MFPL	R/W	R		R/W	
SYS_GPN_MFPH	R/W	R		R/W	
SYS_TSENSRFCR	R/W	R		R/W	
SYS_GMAC0MISCR	R/W		R	R/W	R
SYS_GMAC1MISCR	R/W		R	R/W	R
SYS_MACAD0LSR	R			R	
SYS_MACAD0HSR	R			R	
SYS_MACAD1LSR	R			R	
SYS_MACAD1HSR	R			R	
SYS_CSDBGCTL	R/W	R		R/W	R
SYS_GPAB_MFOS	R/W	R		R/W	
SYS_GPCD_MFOS	R/W	R		R/W	

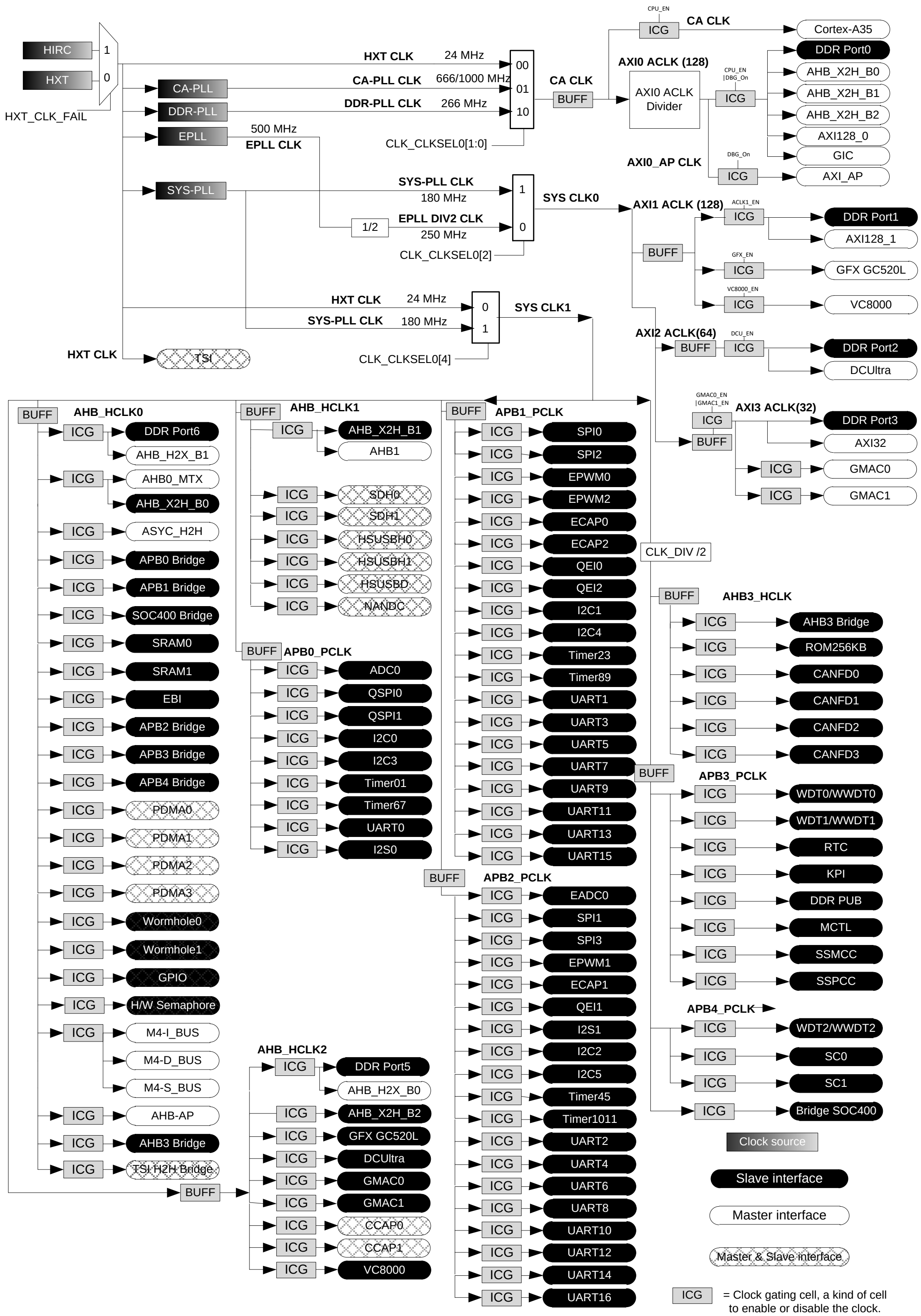
SYS_GPEF_MFOS	R/W	R		R/W		
SYS_GPGH_MFOS	R/W	R		R/W		
SYS_GPIJ_MFOS	R/W	R		R/W		
SYS_GPKL_MFOS	R/W	R		R/W		
SYS_GPMN_MFOS	R/W	R		R/W		
SYS_UID0	R			R		
SYS_UID1	R			R		
SYS_UID2	R			R		
SYS_UCID0	R			R		
SYS_UCID1	R			R		
SYS_UCID2	R			R		
SYS_RLKTZS	R/W	RAZ/WI		R/W	RAZ/WI	
SYS_RLKTZNS	R/W		R	R/W		R
SYS_RLKSUBM	R	R	R/W	R	R	R/W
SYS_NMIIEN	R		R/W	R		R/W
SYS_NMISTS	R			R		

Table 6.4-3 System Manager Control Registers Access Attribute

6.5 Clock Controller

6.5.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individual clock ON/OFF control, clock source selection and a clock divider. The chip will not enter RTP-M4 Power-down mode until RTP-M4 or CA35 sets the Power-down enable bit RTPPDEN (SYS_PMUCR [24]) and the core executes the WFI instruction. The chip will not enter CA35 Power-down mode until CA35 sets the Power-down enable bit CA35PDEN (SYS_PMUCR [16]) and the core executes the WFI instruction. After that, the chip enters CA35 Power-down mode or RTP-M4 Power-down mode and waits for wake-up interrupt source triggered to leave Power-down mode. In CA35 or RTP-M4 Power-down mode, the clock controller can turn off some clock sources or PLL automatically by setting the control bit in CLK_PWRCTL. Figure 6-7, Figure 6-8 and Figure 6-9 show the clock generator and the overview of the clock source control.



Note: Before clock switching, both the pre-selected and newly selected clock source must be turned on and stable.

Figure 6-7 Clock Generator Global View Diagram (1/3)

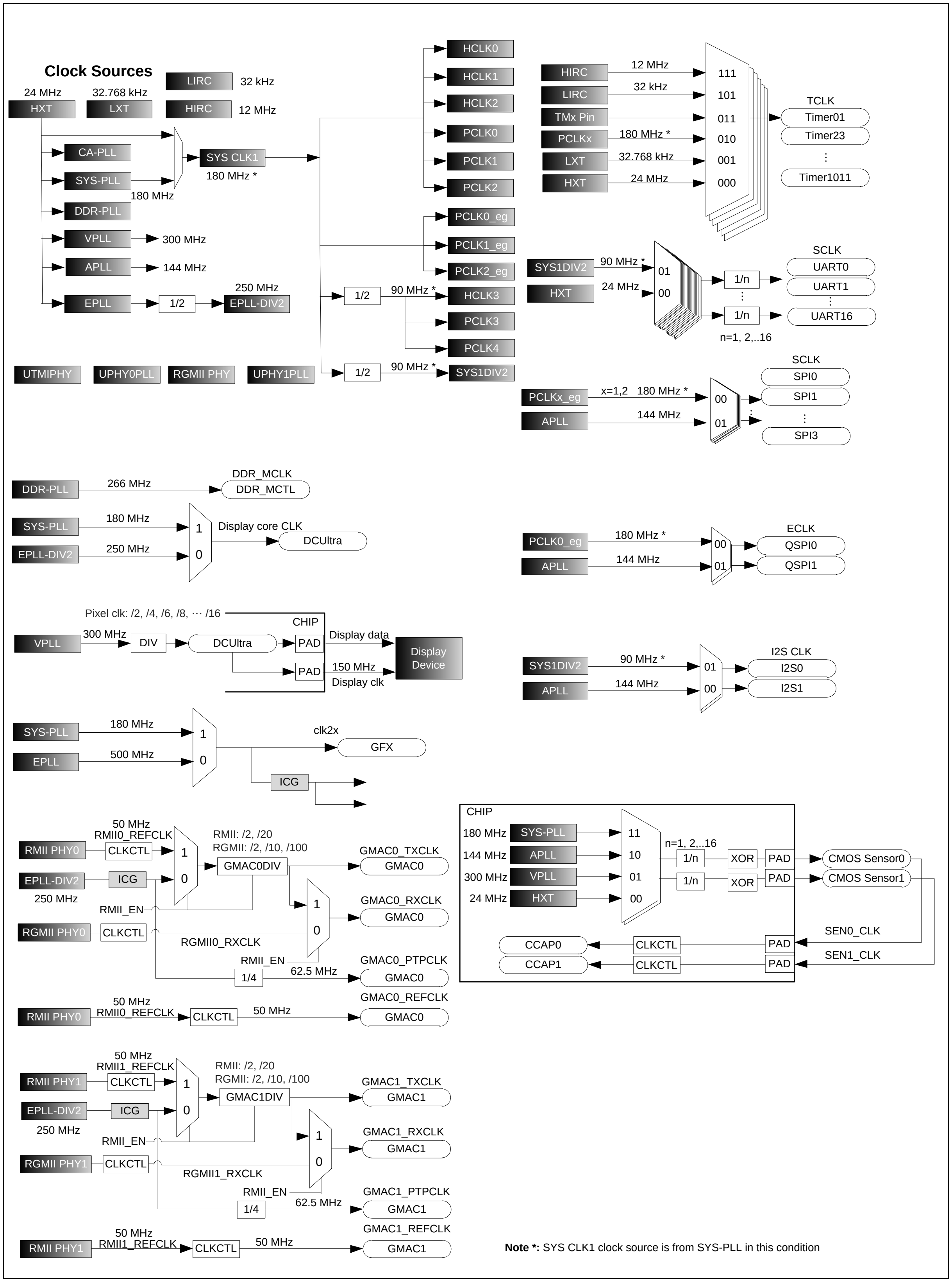


Figure 6-8 Clock Generator Global View Diagram (2/3)

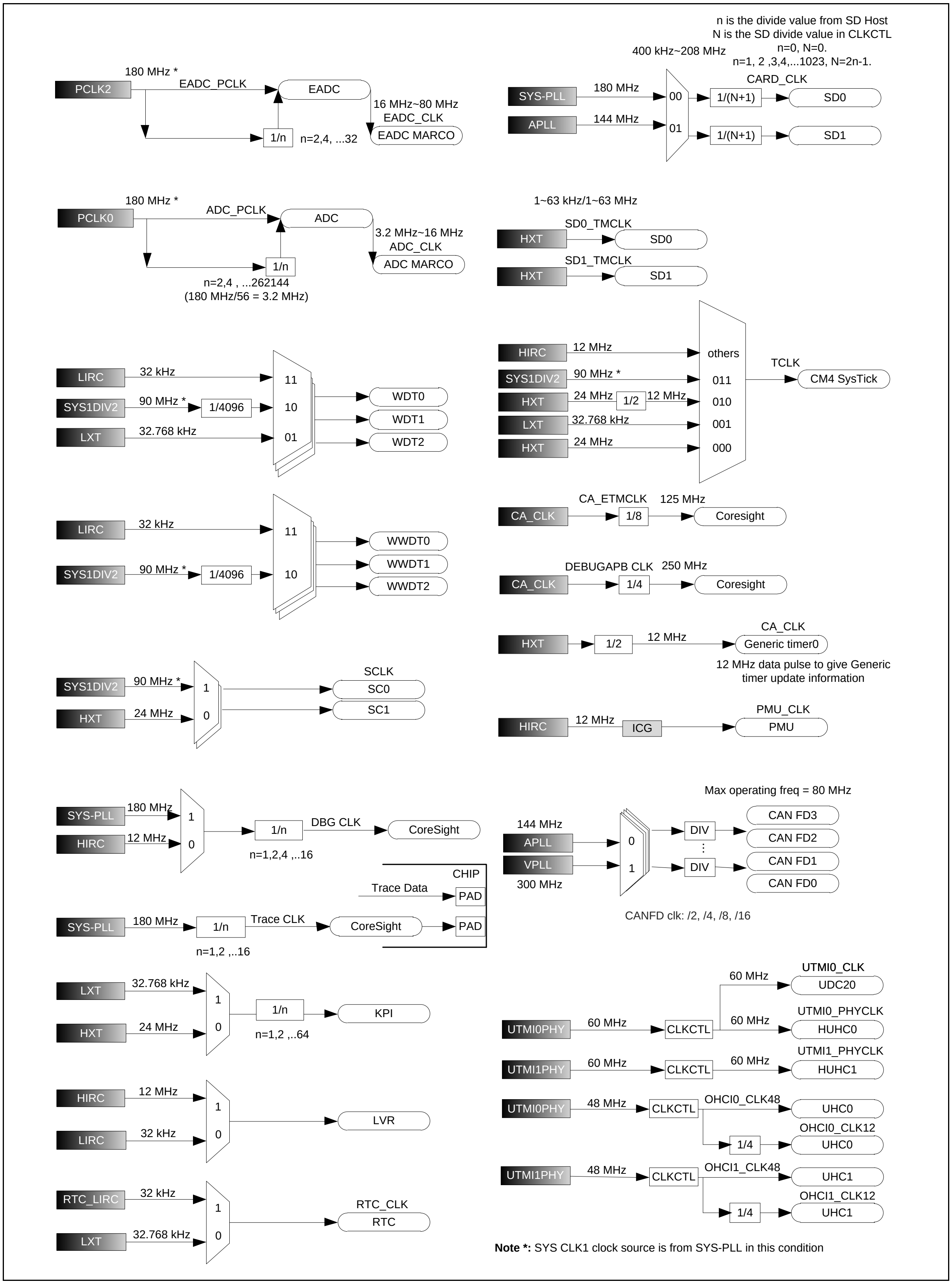


Figure 6-9 Clock Generator Global View Diagram (3/3)

6.5.2 Clock Generator

The clock generator consists of 10 clock sources, which are listed below:

- Programmable PLL for Cortex-CA35 output clock frequency (CA-PLL), PLL source can be selected from external 24 MHz external high speed crystal (HXT).
- Programmable PLL for system output clock frequency (SYS-PLL), PLL source can be selected from external 24 MHz external high speed crystal (HXT).
- Programmable PLL for DDR output clock frequency (DDR-PLL), PLL source can be selected from external 24 MHz external high speed crystal (HXT).
- Programmable PLL for Audio output clock frequency (APLL), PLL source can be selected from external 24 MHz external high speed crystal (HXT).
- Programmable PLL for Ethernet output clock frequency (EPLL), PLL source can be selected from external 24 MHz external high speed crystal (HXT).
- Programmable PLL for video output clock frequency (VPLL), PLL source can be selected from external 24 MHz external high speed crystal (HXT).
- 24 MHz external high speed crystal oscillator (HXT)
- 32.768 kHz external low speed crystal oscillator (LXT)
- 12 MHz internal high speed RC oscillator (HIRC)
- 32 kHz internal low speed RC oscillator (LIRC)

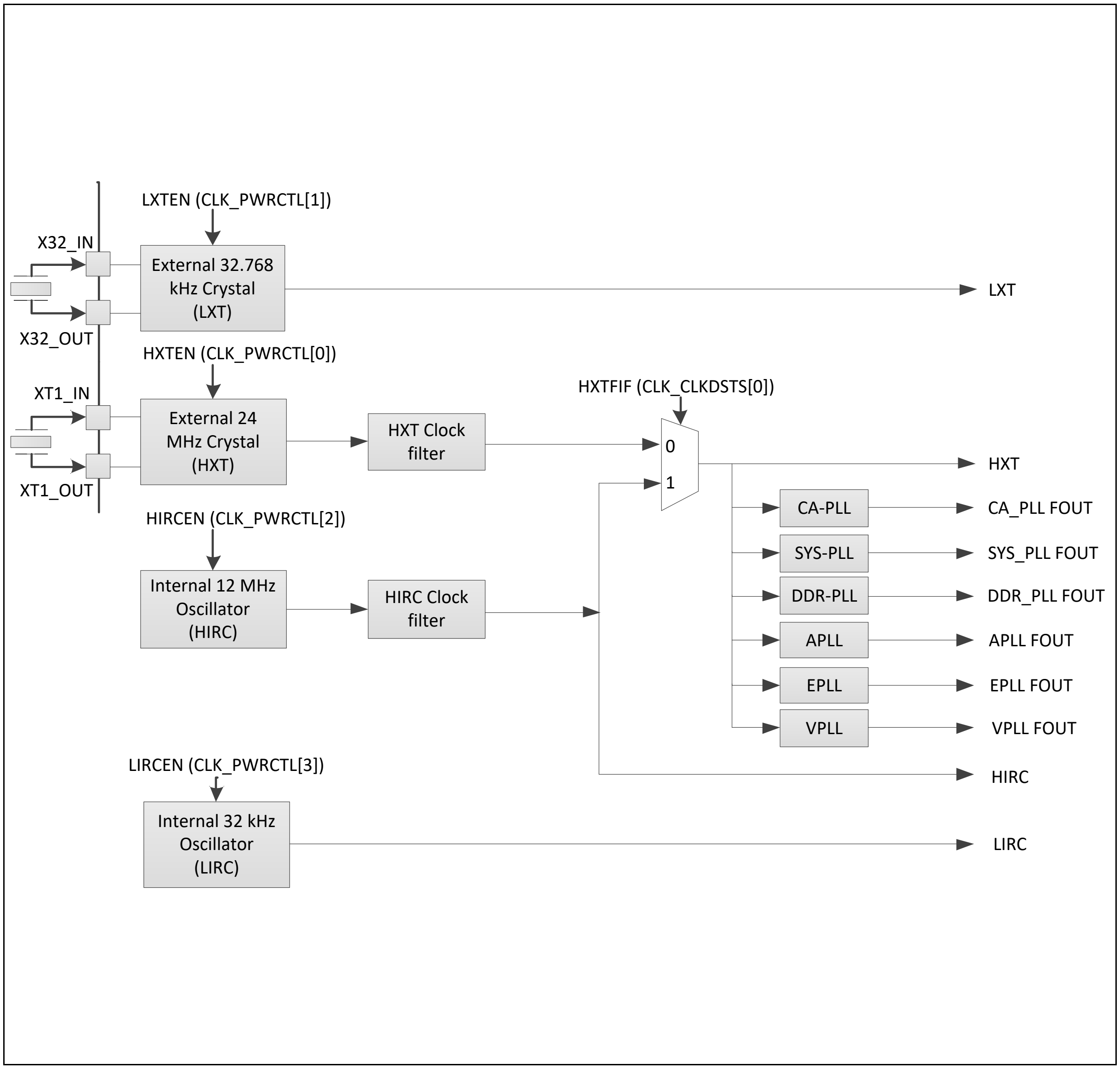


Figure 6-10 Clock Generator Block Diagram

Each of these clock sources has certain stable time to wait for clock operating at stable frequency. When clock source is enabled, a stable counter start counting and correlated clock stable index.

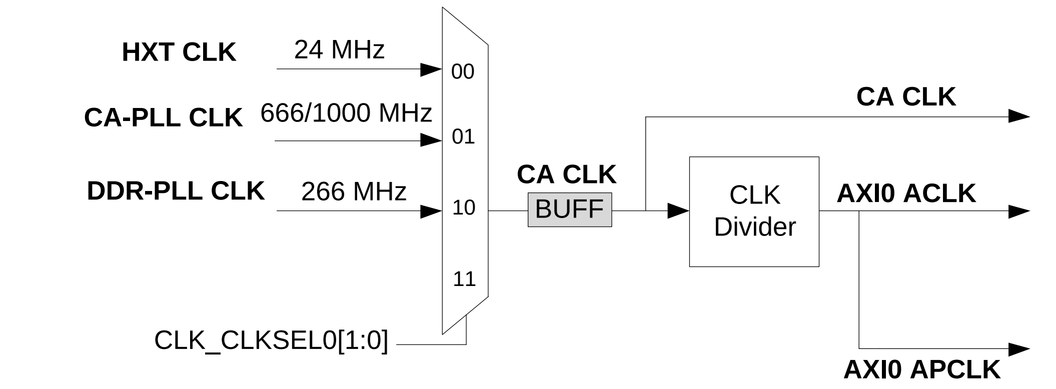
That is, HXTSTB (CLK_STATUS[0]), LXTSTB (CLK_STATUS[1]), SYSPLLSTB (CLK_STATUS[2]), LIRCSTB (CLK_STATUS[3]), HIRCSTB (CLK_STATUS[4]), CAPLLSTB (CLK_STATUS[6]), DDRPLLSTB (CLK_STATUS[8]), EPLLSTB (CLK_STATUS[9]), APLLSTB (CLK_STATUS[10]) and VPLLSTB (CLK_STATUS[11]) these bits are set to 1 after stable counter value reach a define value.

System and peripheral can use the clock as its operating clock only when correlate clock stable index is set to 1. The clock stable index will be automatically cleared when user disables the clock source (HXTEN (CLK_PWRCTL[0]), LXTEN (CLK_PWRCTL[1]), HIRCEN (CLK_PWRCTL[2]), LIRCEN (CLK_PWRCTL[3]), and PD (CLK_PLL0CTL1[0], CLK_PLL2CTL1[0], CLK_PLL3CTL1[0], CLK_PLL4CTL1[0], and CLK_PLL5CTL1[0])).

Besides, the clock stable index of HXT, HIRC, and PLL will be automatically cleared when chip enters power-down and clock stable counter will re-count after chip wake-up if correlate clock is enabled.

6.5.3 CA35 CPU Clock, System Clock and SysTick Clock

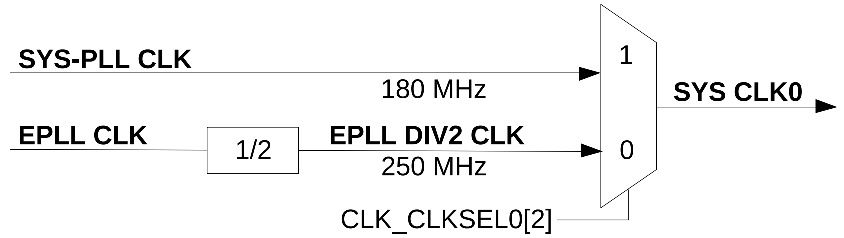
The CA35 CPU clock has 3 clock sources, which are generated from clock generator block. The clock source switch depends on the register CA35CKSEL (CLK_CLKSEL0 [1:0]). There is a clock divider before AXI0 ACLK and AXI0 APCLK. The clock of AXI0 ACLK and AXI0 APCLK can divide 4 or divide 2 by setting ACLK0DIV (CLK_CLKDIV0 [26]). The block diagram is shown in Figure 6-11.



Note: Before clock switching, both the pre-selected and newly selected clock source must be turned on and stable.

Figure 6-11 CA35 CPU Clock Block Diagram

This chip has 2 system clocks, SYSCLK0, and SYSCLK1. The SYSCLK0 has 2 clock sources, which are generated from SYS-PLL and EPLL. There is a frequency divider fixed at 2 before the MUX of SYSCLK0 EPLL source. The SYSCLK0 is the bus clock source of the GFX, VC8000, DCUltra and GMAC. The block diagram is shown in Figure 6-12.



Note: Before clock switching, both the pre-selected and newly selected clock source must be turned on and stable.

Figure 6-12 SYSCLK0 Block Diagram

The SYSCLK1 has 2 clock sources, which are generated from SYS-PLL, and HXT. The SYSCLK1 is the bus clock source of Real time processor and most of all the peripherals. The block diagram is shown in Figure 6-13.

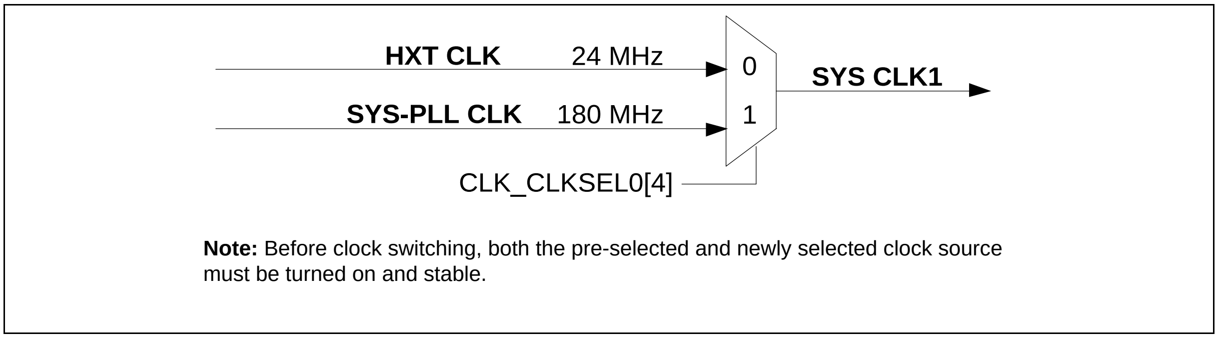


Figure 6-13 SYSCLK1 Block Diagram

There are two clock fail detectors to observe HXT and LXT clock source and they have individual enable and interrupt control. When HXT detector is enabled, the HIRC clock is enabled automatically. When LXT detector is enabled, the LIRC clock is enabled automatically.

When HXT clock detector is enabled, the HXT clock source will automatically switch to HIRC if HXT clock stop is detected. If HXT clock stop condition is detected, the HXTFIF (CLK_CLKDSTS[0]) is set to 1 and chip will enter interrupt if HXTFIE (CLK_CLKDCTL[5]) is set to 1. HXT clock source stable flag, HXTSTB (CLK_STATUS[0]), will be cleared if HXT stops when using HXT fail detector function. User can try to recover HXT by disabling HXT, and enable HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recovered to oscillate after re-enable action and user can switch system clock to HXT again.

The HXT clock stop detect and system clock switch to HIRC procedure is shown in Figure 6-14.

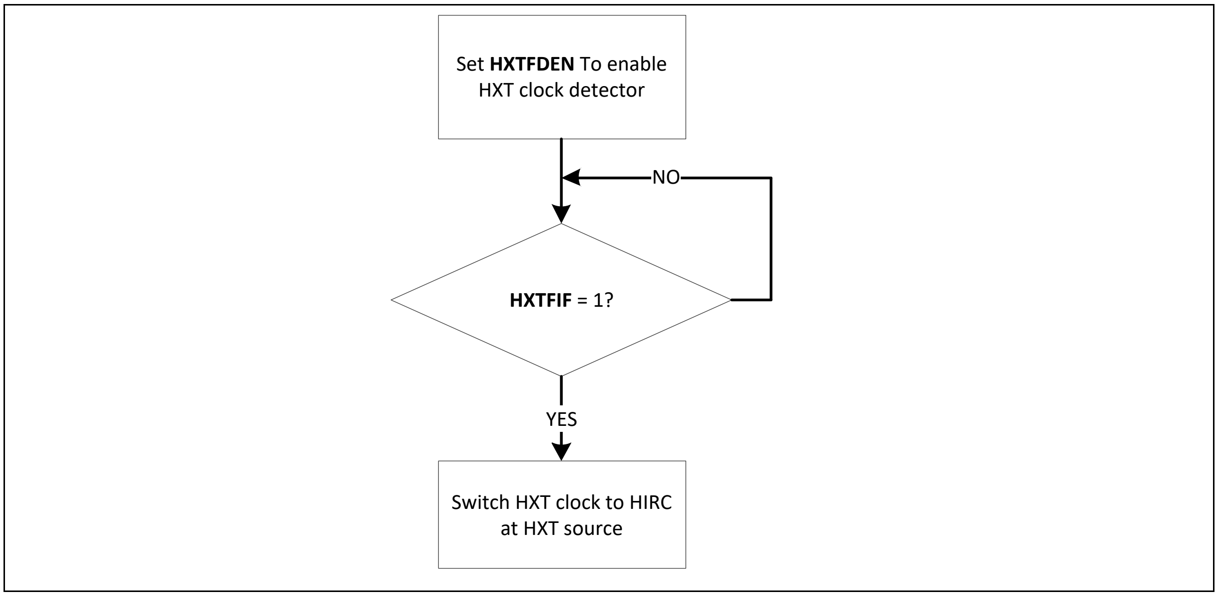


Figure 6-14 HXT Stop Protect Procedure

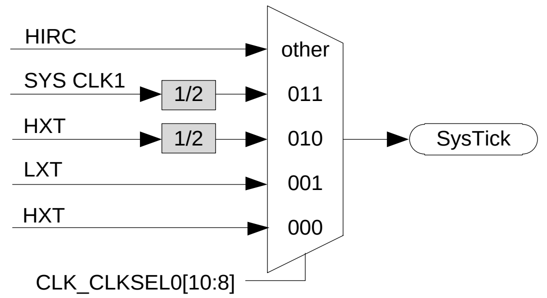


Figure 6-15 SysTick Clock Control Block Diagram

The clock source of SysTick in processor can use CPU clock or external clock (SYST_CTRL[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register RTPSTSEL (CLK_CLKSEL0 [10:8]). The block diagram is shown in Figure 6-15.

6.5.4 Peripherals Clock

Each peripheral clock has its own clock source selection. Refer to the CLK_CLKSEL0, CLK_CLKSEL1, CLK_CLKSEL2, CLK_CLKSEL3 and CLK_CLKSEL4 register.

6.5.5 PLL Settings and Operation Modes

This chip is embedded with 2 PLLs and 4 Advanced PLLs. The PLL has only 1 operation mode. The Advanced PLL has 3 operation modes for use, including integer mode, fraction mode and spread spectrum mode. The integer mode is used for normal PLL operations. The fraction mode is used for the specific clock output frequency, such like 147.456 MHz. The spread spectrum mode is used for the application with EMI concern.

Output Clock Frequency Formula in different modes is shown below.

6.5.5.1 *PLL Control Mode*

$$\frac{F_{CLK}}{N} = \frac{F_{REF}}{M}$$

$$F_{CLKO} = \frac{F_{CLK}}{P}$$

Equation 6.5-1 PLL Control Mode Equation

Feedback divider factor, N = FBDIV[7:0] = PLL0CTL0[7:0]

Input divider, M = INDIV[5:0] = PLL0CTL0[11:8]

Output divider, P = 2^ OUTDIV[1:0] = PLL0CTL0[13:12],

EX: If OUTDIV = 00, P=1. If OUTDIV = 01, P=2. If OUTDIV = 10, P=4. If OUTDIV = 11, P=8.

For proper operation in normal mode, the following constraints must be satisfied:

1 MHz ≤ F_{REF} ≤ 50 MHz

500 MHz ≤ F_{CLK} ≤ 1500 MHz

$62.5\ MHz \le F_{CLKO} \le 1500\ MHz$

M >=2; N >=1

6.5.5.2 *Advanced PLL Integer Mode*

$$\frac{F_{CLK}}{N} = \frac{F_{REF}}{M}$$

$$F_{CLKO} = \frac{F_{CLK}}{P}$$

Equation 6.5-2 Advanced PLL Integer Mode Equation

Feedback divider factor, N = FBDIV[10:0] = PLLxCTL0[10:0]

Input divider, M = INDIV[5:0] = PLLxCTL0[17:12]

Output divider, P = OUTDIV[2:0] = PLLxCTL1[6:4]

Wherein F_{REF} is the input frequency, F_{CLK} is the output frequency of VCO, F_{CLKO} is the output frequency after output divider.

For proper operation in integer mode, the following constraints must be satisfied:

$1\ MHz \le F_{REF} \le 200\ MHz$

$1\ MHz \le F_{REF}/M \le 40\ MHz$

$600\ MHz \le F_{CLK} \le 2400\ MHz$

$85.7\ MHz \le F_{CLKO} \le 2400\ MHz$

6.5.5.3 *Advanced PLL Fractional Mode*

$$\frac{F_{CLK}}{N.X} = \frac{F_{REF}}{M}$$

$$F_{CLKO} = \frac{F_{CLK}}{P}$$

Equation 6.5-3 Advanced PLL Fractional Mode Equation

Feedback divider factor, N = FBDIV[10:0] = PLLxCTL0[10:0]

Input divider, M = INDIV[5:0] = PLLxCTL0[17:12]

Output divider, P = OUTDIV[2:0] = PLLxCTL1[6:4]

Fractional number, X=FRAC[23:0]/2^{24}, FRAC[23:0] = PLLxCTL1[31:8]

Fractional divider, N.X = N+X

For proper operation in Fraction mode, the following constraints must be satisfied:

1 MHz ≤ F_{REF} ≤ 200 MHz

10 MHz ≤ F_{REF} /M ≤ 40 MHz

600 MHz ≤ F_{CLK} ≤ 2400 MHz

85.7 MHz ≤ F_{CLKO} ≤ 2400 MHz

147.456 MHz, FCLKO= 18432/125,

let P = 5, FCLK= 18432/25,

18432/(25*N.X)=(24/M), 18432/(25*24) = (N.X)/M, 30.72 = (N.X)/M

For 24/M > 10, M = 1,

30.72 = N.X, N= 30, X = 0.72, FRAC = 12079595.52 ~= 12079596

FBDIV[10:0] = N = 30 = 0x1E

INDIV[4:0] = M = 1

OUTDIV[2:0] = P = 5

FRAC[23:0] = FRAC= 12079596 = 0xB851EC

6.5.5.4 *Advanced PLL Spread Spectrum Mode*

The Advanced PLL Spread Spectrum mode only supports down spreading.

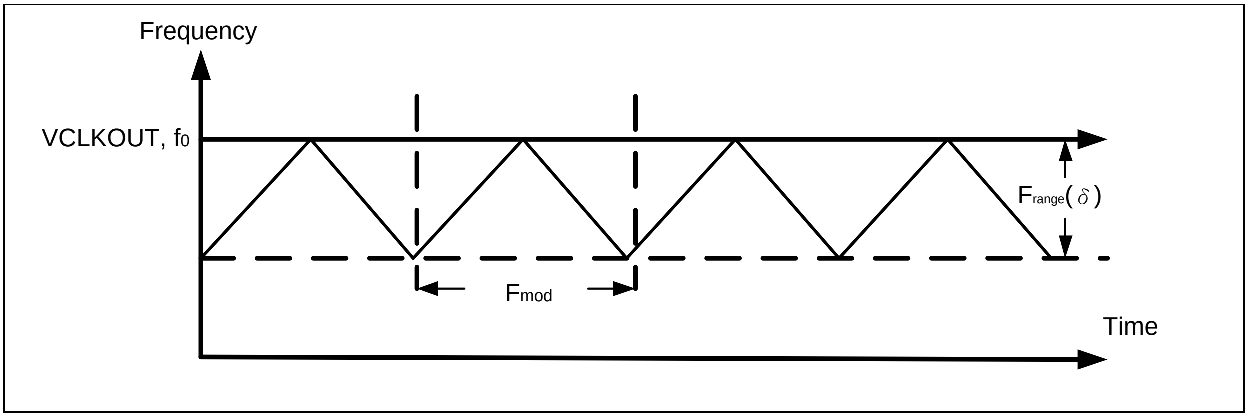


Figure 6-16 Advanced PLL Down Spreading in Spectrum Mode

$$\frac{F_{CLK}}{N.X} = \frac{F_{REF}}{M}$$

$$F_{CLKO} = \frac{F_{CLK}}{P}$$

$$F_{MOD} = \frac{F_{REF}}{M * SS * 2}$$

$$SS = \frac{\frac{F_{REF}}{M}}{F_{MOD} * 2}$$

$$SSRATE = SS - 1$$

$$SLOPE = \frac{N.X * \delta}{SS} * 2^{24}$$

Equation 6.5-4 Advanced PLL Spread Spectrum Mode Equation

SSRATE = PLLxCTL0 [30:20]
SLOPE = PLLxCTL2 [23:0]

For proper operation in Spread Spectrum mode, the following constraints must be satisfied:

1 MHz ≤ F_{REF} ≤ 200 MHz

10 MHz ≤ F_{REF} /M ≤ 40 MHz

600 MHz ≤ F_{CLK} ≤ 2400 MHz

85.7 MHz ≤ F_{CLKO} ≤ 2400 MHz

-3% ≤ δ (spread range) ≤ 0%

15 kHz ≤ F_{MOD} (modulation frequency) ≤ 50 kHz

1. Spread Spectrum Mode Example 1

   266 MHz, FCLKO= 266 MHz, (P*266)/(N.X)=(24/M), δ (spread range) = 1.94%, modulation frequency = 50 kHz

   For 24/M > 10, M <= 2, choose M = 2.

   For 16 ≤ N ≤ 2047

   266/12 = 133/6 = 22.167= (N.X)/P, N= 133, X = 0, FRAC = 0, P= 6.

   FCLK = 2400 MHz ≤ 1596 MHz ≤ 600 MHz

   SSRATE = ((24 MHz/2)/(50 kHz*2)) – 1 = 119 (SPEC max is 50 kHz)

   SLOPE = ((133.0*1.94%) / 119) *2^{24}=363769.5187 ~= 363770

   FBDIV [10:0] = N = 133 = 0x85

   INDIV [4:0] = M = 2

   OUTDIV [2:0] = P = 6, OUTDIV = 6

   FRAC [23:0] = FRAC= 0 = 0x0

   SSRATE [10:0] = SSRATE = 119 = 0x77

   SLOPE [23:0] = SLOPE = 363770 = 0x58CFA

2. Spread Spectrum Mode Example 2

533 MHz, FCLKO= 533 MHz, (P*533)/(N.X)=(24/M), δ (spread range) = 3%, modulation frequency = 40 kHz

For 24/M > 10, M = 1, 1066/24 =44.4167= P*(N.X), P=2, N= 44, X = 0.4167, FRAC = 6990506.667~= 6990507

SSRATE = ((24 MHz/1)/(40 kHz*2)) -1 = 300-1 =299

SLOPE = ((44.4167)*3%/300)*2^{24}=74518.85699 ~= 74519

FBDIV [10:0] = N = 44 =0x2C

INDIV [4:0] = M = 1

OUTDIV [2:0] = P = 2

FRAC [23:0] = FRAC= 6990507 = 0x6AAAAB

SSRATE [10:0] = SSRATE = 299 = 0x12B

SLOPE [23:0] = SLOPE = 74519 = 0x12317

Table 6.5-1 Advanced PLL Settings Example

Mode	F_{Out}	F_{REF}	Spread Range (Δ)	Modulation Frequency (F_{MOD})	PLLxCTL0[31:0]	PLLxCTL1[31:0]	PLLxCTL2[31:0]
Fractional mode	147.456 MHz	24 MHz	N/A	N/A	0x0004_101E	0x B851_EC50	0x0000_0000
Spread Spectrum Mode	266 MHz	24 MHz	1.94%	50 kHz	0x0778_2085	0x0000_0060	0x0005_8CFA
Spread Spectrum Mode	533 MHz	24 MHz	3%	40 kHz	0x12B8_102C	0x6AAA_AB20	0x0001_2317

6.5.6 Power-down Mode Clock

When entering Power-down mode, some PLL and clock sources can be configured to turn off automatically by setting control bit in CLK_PWRCTL for the better power consumption.

Besides these PLLs and clock sources, other clock sources can be enabled or disabled by different applications.

The clock sources and PLLs, which can be configured to turn off automatically, are listed below:

- When CA35 is power down:
  - Turn off 12 MHz internal high speed RC oscillator (HIRC) automatically by setting HIRCAPD (CLK_PWRCTL [23]).
  - Turn off 24 MHz external high speed crystal oscillator (HXT) automatically by setting HXTAPD (CLK_PWRCTL [22]).
- When CA35 is in power gating mode:
  - Turn off General Interrupt Controller (GIC) clock automatically by setting GICAOFF (CLK_PWRCTL [21]).
  - Turn off 12 MHz internal high speed RC oscillator (HIRC) automatically by setting HIRCAOFF (CLK_PWRCTL [15]).
  - Turn off 24 MHz external high speed crystal oscillator (HXT) automatically by setting HXTAOFF (CLK_PWRCTL [14]).
  - Turn off DDR-PLL automatically by setting DDRPLLAPD (CLK_PWRCTL [13]).
  - Turn off CA-PLL automatically by setting CAPLLAPD (CLK_PWRCTL [12]).
- When CA35 and RTP-M4 are power down:
  - Turn off SYS-PLL automatically by setting SYSPLLAPD (CLK_PWRCTL [11]).

6.5.7 Clock Output

This device is equipped with a power-of-2 frequency divider that is composed by 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore, there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]). When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stays in low state.

If DIV1EN(CLK_CLKOCTL[5]) set to 1, the clock output clock (CLKO_CLK) will bypass power-of-2 frequency divider. The output divider clock will be output to CLKO pin directly.

When entering Power-down mode, clock output does not output clock even if the CLKO clock source is LXT.

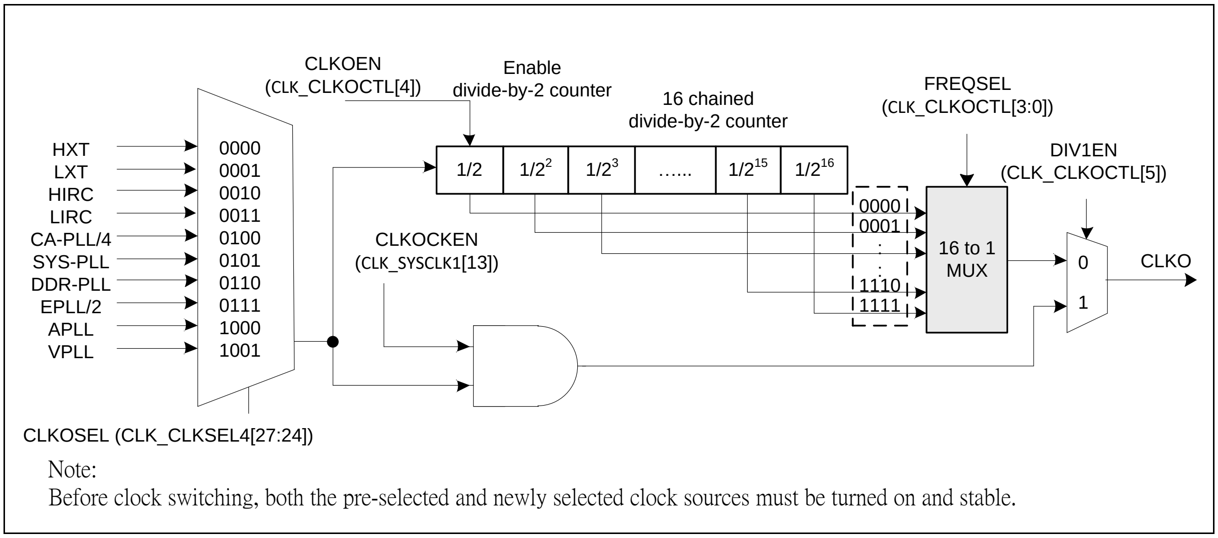


Figure 6-17 Clock Output Block Diagram

6.5.8 Control Registers Access Attribute

The clock controller shares part of register information to non-secure world with enable bits in SYSSINFAEN (SCU_SINFAEN[1]) register. Shared registers are enabled by default.

The clock control registers access attributes are shown in Table 6.5-2.

R: read only, **W:** write only, **R/W:** both read and write, **RAZ/WI**: read as zero, write ignore, **Wip**: write authority is set by SSPCC.

Register	**SYSSIAEN (SSPCC_SINFAEN[1]) =0**			**SYSSIAEN (SSPCC_SINFAEN[1]) =1**		
	TZS	TZNS	SubM	TZS	TZNS	SubM
CLK_PWRCTL	R/W	R		R/W	R	
CLK_SYSCLK0	R/ Wip			R/ Wip		
CLK_SYSCLK1	R/ Wip			R/ Wip		
CLK_APBCLK0	R/ Wip			R/ Wip		
CLK_APBCLK1	R/ Wip			R/ Wip		
CLK_APBCLK2	R/ Wip			R/ Wip		
CLK_CLKSEL0	R/ Wip			R/ Wip		
CLK_CLKSEL1	R/ Wip			R/ Wip		
CLK_CLKSEL2	R/ Wip			R/ Wip		
CLK_CLKSEL3	R/ Wip			R/ Wip		
CLK_CLKSEL4	R/ Wip			R/ Wip		

CLK_CLKDIV0	R/ Wip			R/ Wip		
CLK_CLKDIV1	R/ Wip			R/ Wip		
CLK_CLKDIV2	R/ Wip			R/ Wip		
CLK_CLKDIV3	R/ Wip			R/ Wip		
CLK_CLKDIV4	R/ Wip			R/ Wip		
CLK_CLKOCTL	R/W			R/ W		
CLK_STATUS	R			R		
CLK_PLL0CTL0	R/W	R		R/W	R	
CLK_PLL2CTL0	R/W	R		R/W	R	
CLK_PLL2CTL1	R/W	R		R/W	R	
CLK_PLL2CTL2	R/W	R		R/W	R	
CLK_PLL3CTL0	R/W	R		R/W		R
CLK_PLL3CTL1	R/W	R		R/W		R
CLK_PLL3CTL2	R/W	R		R/W		R
CLK_PLL4CTL0	R/W	R		R/W		R
CLK_PLL4CTL1	R/W	R		R/W		R
CLK_PLL4CTL2	R/W	R		R/W		R
CLK_PLL5CTL0	R/W	R		R/W		R
CLK_PLL5CTL1	R/W	R		R/W		R
CLK_PLL5CTL2	R/W	R		R/W		R
CLK_CLKDCTL	R/W	R		R/W	R	
CLK_CLKDSTS	R/W	R		R/W		
CLK_CDUPB	R/W	R		R/W	R	
CLK_CDLOWB	R/W	R		R/W	R	
CLK_HXTFSEL	R/W	R		R/W	R	

Table 6.5-2 Clock Controller Registers Access Attribute

6.6 SSPCC

6.6.1 Overview

System security peripheral configuration controller, SSPCC, is used to configure the security attribution of SRAM, GPIO and all other peripherals for Cortex-A35 and Cortex-M4. SSPCC also collects peripherals' security violation response and generates interrupt when violation event occurs.

In addition, SSPCC contains DPM, a module controlling debug access of this chip, and PLM, which uses pre-defined life-cycle stages to provide hardware-based controls controlling the ability of some functions.

6.6.2 Features

- Configures SRAM's security attribution by boundary
- Configures GPIO security attribution pin by pin
- Configures peripherals' security attribution
- Write protect mechanism to security attribution configuration
- Generates secure violation interrupt
- Debug protection mechanism (DPM)
- Product life-cycle management (PLM)

6.7 SSMCC

6.7.1 Overview

System Security Memory Configuration Controller, SSMCC, is the module to manage the access authority of external DRAM. SSMCC provides the access authority, including TrustZone authority and SubM region authority, which follows the pre-defined memory access policy but has more flexibility.

6.7.2 Features

- Configure security attribution of DRAM based on address range
- Two Arm TZC400 controllers controlling seven AXI channels in total
- Security violation report and interrupt
- Programmable DRAM region for SubM system
- Write Protect of security configuration to prevent accidental change.

6.8 True Random Number Generator (TRNG)

6.8.1 Overview

The TRNG NIST SP800-90C is NIST SP800-90A/B/c and BSI AIS 20/31 compliant True Random Number Generator (TRNG). It generates random numbers that are intended to be statistically equivalent to a uniformly distributed random data stream. The circuit includes a NIST SP800-90B compliant noise source, a NIST SP800-90B vetted conditioning component, and a NIST SP800-90A approved Deterministic Random Bit Generator (DRBG). The noise source sends Independent and Identically Distributed (IID) noise stream to the conditioning component to produce full-entropy seed which is then fed into the DRBG to generate random numbers. A health test block is included to perform Known Answer Tests (KAT) and seven different statistical tests required by NIST SP800-90A/B/c and BSI AIS 20/31. The health test block is capable of performing start-up, on-demand, and continuous tests.

The TRNG NIST can generate random seeds from the internal ring-oscillator based noise source or can be manually seeded through a host-provided nonce. Host-provided nonce are fed into the conditioning component to increase the entropy rate using a NIST SP800-90B vetted conditioning function. If the host's nonce has enough entropy, the nonce can also be directly loaded into the DRBG to be used as a seed

6.8.2 Features

- Background noise collection to speed reseeding operations
- Internal random seeding operation
- 128-bit random number generation
- Start-up, continuous and on-demand health tests
- Compliant with NIST SP800-90A/B/c and BSI AIS 20/31
- 128-bit or 256-bit of security strength
- Ring oscillator-based Bit Generator blocks with wide system clock rate dynamic range
- Independent ring oscillator-based Bit Generator blocks

6.9 Hardware Semaphore (HWSEM)

6.9.1 Overview

The Hardware Semaphore block provides 8 hardware semaphores, which can be used to synchronize between different processors with different semaphore keys.

6.9.2 Features

- Supports 8 hardware semaphores for synchronization control between processors
- Interrupt notification for semaphore unlock
- Semaphore is locked by an 8-bit key
- Only the core locking a semaphore can unlock the semaphore with the correct key

6.10 Wormhole Controller (WHC)

6.10.1 Overview

This chip is equipped with two Wormhole Controllers (WHC) that facilitates inter-processor communication between Cortex-A35 and Cortex-M4, and between Cortex-A35 and TSI.

The WHC utilizes an interactive mechanism for each processor to deliver and receive data with eight unidirectional message channels. Each side can send messages and inform counterpart to read these messages. After the receiver has read these messages, the sender will be acknowledged and then be able to send next messages. Moreover, a recall function is implemented for sender to call back the sent messages.

6.10.2 Features

- One interrupt notifies reset event or power state change event to other side
- One register indicates the status of counterpart, including:
  - Power state (power down, power off)
  - Reset source
- Four general event interrupts on each side
- Eight unidirectional message channels, four for each direction. Each channel transfer 16-byte data.
- Supports message recall by Tx side.

6.11 DDR Memory Controller (UMCTL2)

6.11.1 Overview

The uMCTL2 is a DDR memory controller and specific hardware configuration of Synopsys uMCTL2 DDR controller v3.80a.

In our chip, the uMCTL2 only supports the following three SDRAM types, and other SDRAM types are not supported:

- DDR2
- DDR3
- DDR3L

On the host side, the uMCTL2 can accept memory access requests from up to 7 application-side host ports. The configuration registers are programmed through the AMBA 3.0 APB software interface.

6.11.2 Features

- Complete, integrated, single-vendor DDR2, DDR3, DDR3L solution when combined with the Synopsys DWC DDR PHY
- Supports a range of DDR3/DDR3L SDRAM speeds, from DDR3-667/DDR3L-667 through DDR3-1066/DDR3L-1066
- Supports a range of DDR2 SDRAM speeds, from DDR2-667 through DDR2-1066
- For DDR3 configurations, direct software request control or programmable internal control for ZQ short calibration cycles
- For DDR3 configurations, support for ZQ long calibration after self-refresh exit
- Dynamic scheduling to optimize bandwidth and latency
- Read and write buffers in fully associative CAMs, configurable in powers of two
- Delayed writes for optimum performance on SDRAM data bus
- For maximum SDRAM efficiency, commands are executed out-of-order
- Programmable SDRAM parameters
- 16 bits SDRAM data-bus width
- Supported SDRAM Burst Length of 8
- Supports maximum 2 memory ranks
- Not support all DIMM modes
- Control options to avoid starvation of lower priorities
- Guaranteed coherency for write-after-read (WAR) and read-after-write (RAW) hazards
- Write combine to allow multiple writes to the same address to be combined into a single write to SDRAM; supported for same starting address
- Paging policy selectable by configuration registers as any of the following:
  - Leave pages open after accesses, or
  - Close page when there are no further accesses available in the controller for that

  page, or
  - Auto-precharge with each access, with an optimization for page-close mode which leaves the page open after a flush for read-write and write-read collision cases
- Supports automatic SDRAM power-down entry and exit caused by lack of transaction arrival for a programmable time
- Supports automatic uMCTL2 low power mode operation caused by lack of transaction arrival for a programmable time through the Hardware Low Power Interface
- Supports self-refresh entry and exit as follows:
  - Support for automatic self-refresh entry and exit caused by lack of transaction arrival for a programmable time
  - Support for self-refresh entry and exit under software control
  - Support for self-refresh entry and exit using dedicated DDRC hardware low power interface control (similar to the AMBA 3 AXI protocol low power control interface)
- Support for explicit SDRAM mode register updates under software control
- Flexible address mapper logic to allow application specific mapping of row, column, bank, and rank bits
- Programmable support for 1T or 2T timing
- Selectable refresh control options:
  - Controller-generated auto-refreshes at programmable average intervals
  - In multi-rank designs, an offset can be applied to each rank's refresh timer to allow rank refreshes to expire at different times
  - Ability to group up to 8 controller-generated refreshes together to be issued consecutively
  - When controller-generated refreshes are grouped, some refreshes can be issued speculatively when the controller is idle for a programmable period of time
  - Ability to disable controller-generated auto-refreshes
  - Ability to issue a refresh through direct software request
  - When controller-generated refreshes are grouped, some refreshes can be issued speculatively when the controller is idle does not have any HIF transactions to the SDRAM rank/bank address for a programmable period of time
- Advanced power-saving design includes no unnecessary toggling of command, address, and data pins (RAS/CAS/WE/BA/A hold last state after each command; DQ does not transition on writes when bytes are disabled)
- Leverages out of order requests with CAM to maximize throughput
- APB interface for the uMCTL2 software accessible registers
- 7 host ports using AMBA AXI

6.12 DDR 3/2 PHY Controller (DDR32PHY)

6.12.1 Overview

The DDR3/2 PHY is a DDR PHY controller and specific hardware configuration of Synopsys DDR3/2 PHY v1.50a.

The DDR3/2 PHY Utility Block (PUB) is a specific hardware configuration of Synopsys DDR3/2 PHY Utility Block (PUB) v3.18.

The DWC DDR3/2 PHY core, Synopsys' Double Data Rate 3 (DDR3) physical layer, provides an interface between the DDR3/DDR2 memory controller and external DDR3/DDR2 SDRAM devices.

The DWC DDR3/2 PHY is a complete mixed-signal IP solution designed to provide DDR 3/2 SDRAM connectivity. The DWC DDR3/2 PHY supports a range of DDR3 SDRAM speeds, from DDR3-667 through DDR3-1066, with backward compatibility provided for DDR2-667 through DDR2-1066 devices. Targeted toward supporting x16 DDR3 SDRAM components, DWC DDR3/2 PHY supports interfaces widths of 16 bits wide.

The DWC PHY Utility Block (PUB) provides control features to ease the customer implementation of digitally controlled features of the PHY such as initialization, DQS gate training, delay line calibration and VT compensation, write leveling, and programmable configuration controls. The PUB has built-in self-test features to provide support for production testing of the DWC PHY. It also provides a DFI interface to the PHY.

The PUB includes configuration registers that are accessible via a configuration port. The configuration port is an APB interface. A complete memory interface and control solution is achieved when the PUB is combined with Synopsys DWC DDR3/2 PHY and with either the Synopsys DesignWare Cores SDRAM Enhanced Universal DDR Memory Controller (uMCTL2).

6.12.2 Features

- Supports DDR3, DDR3L, and DDR2 operation
- Compatible with JEDEC standard DDR2/DDR3/DDR3L SDRAMs
- Supports a range of DDR3/DDR3L SDRAM speeds, from DDR3-667/DDR3L-667 through DDR3-1066/DDR3L-1066
- Supports a range of DDR2 SDRAM speeds, from DDR2-667 through DDR2-1066
- Maximum controller clock frequency of 266 MHz resulting in maximum SDRAM data rate of 1066Mbps
- Includes embedded PLL and DDLs necessary to meet timing specifications
- DDR3 PHY-Controller interface runs at 1/4 the memory baud rate, simplifying core logic timing constraints
- Write leveling delay line (WLDL) to compensate address and control versus data delays of up to 1 clock cycle or 2500ps
- Write and read bit delay lines (BDLs) compensate per-bit delay skew of up to 600ps at fast PVT; delay resolution approximately 15ps under typical conditions
- PHY Utility Block (PUB), a design that includes PHY control features, such as write leveling and data eye training, and provides support for production testing of the DWC DDR3/2 PHY
- SDRAM DLL off mode is not supported

- Data path width in 16-bits
- Support up to 2 memory ranks
- Support HDR mode only
- Single data channel configurations
- Complete PHY initialization, training and control
- Automatic DQS gate training
- Delay line calibrations and VT compensation
- Automatic write leveling
- Automatic read and write data bit de-skew
- Automatic DQ/DQS eye training
- PHY control and configuration registers
- APB interfaces to configuration registers
- DFI interface 2.1

6.12.2.1 *Compatible Standards*

Table 6.12-1 is compatible standards with the DWC DDR3/2 PHY design.

JESD79-2E	JEDEC DDR2 SDRAM Specification
JESD79-3C	JEDEC DDR3 SDRAM Specification
DFI v2.1	DDR PHY Interface (DFI) Specification

Table 6.12-1 Compatible Standards

6.13 One Time Programming Memory Controller (OTP)

6.13.1 Overview

The One Time Programming Memory Controller (OTP) has an embedded Synopsys® Extra Permanent Memory (XPM). Data stored in XPM is Total Secure. The OTP controller realizes all functions of XPM memory including reading and programming function by 32 bits data format. The OTP controller provides fault tolerant mechanism to revise configuration or data, and provides the read only lock bit to protect configuration or data from being destroyed.

6.13.2 Features

- Supports 32 bits programming function and reading function
- Supports 8kbits Secure OTP memory
- Supports data retention more than 10 years
- Supports fault tolerant mechanism
- Supports read only lock bit
- Supports side-band handshaking signals with Key Store

6.14 External Bus Interface (EBI)

6.14.1 Overview

This chip is equipped with an external bus interface (EBI) for external device use. To save the connections between an external device and a chip, EBI is operating at address bus and data bus multiplex mode. The EBI supports three chip selects that can connect three external devices with different timing setting requirements.

6.14.2 Features

- Supports up to three memory banks
- Supports dedicated external chip select pin with polarity control for each bank
- Supports accessible space up to 1 Mbytes for each bank, actually external addressable space is dependent on package pin out
- Supports 8-/16-bit data width
- Supports byte write in 16-bit data width mode
- Supports address bus and data bus multiplexed mode
- Supports address bus and data bus separate mode
- Supports Timing parameters individual adjustment for each memory block
- Supports LCD interface i80 mode
- Supports PDMA mode
- Supports variable external bus base clock (MCLK) which based on HCLK
- Supports configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R)

6.15 General Purpose I/O (GPIO)

6.15.1 Overview

This chip has up to 208 General-Purpose I/O (GPIO) pins and can be shared with other function pins depending on the chip configuration. These 208 pins are arranged in 16 ports named as PA, PB, PC, PD, PE, PF, PG, PH, PI, PJ, PK, PL, PM, PN. Each port has 16 pins on port, except PB, PC, PH and PN. PB has 8 pins on port. PC has 12 pins on port. PH and PN has 14 pins on port. All of the 208 I/O pins is independent and can be easily configured by user to meet various system configurations and design requirements.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output or Open-drain output. After reset, all 208 I/O pins are configured in General-Purpose I/O Input mode. Each I/O pin has a very weakly individual pull-up resistor. Please refer to the MA35D1 Series Datasheet for detailed pin operation voltage information about V_{DD} electrical characteristics

6.15.2 Features

- Three I/O modes:
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Drive and High Slew Rate I/O mode
- Support independent pull-up and pull-down control
- Enabling the pin interrupt function will also enable the wake-up function

6.16 PDMA Controller (PDMA)

6.16.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. There are four PDMA controller, PDMA0 ~ PDMA3. Both PDMA0 and PDMA1 can be set as secure or non-secure. On the other side, both PDMA2 and PDMA3 can be configured as non-secure or SubM domain. Each PDMA controller has a total of 10 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

6.16.2 Features

- Supports 10 independently configurable channels
- Supports 2 selectable levels of priority
  - Fixed priority
  - Round-robin priority
- Supports 4 PDMA controllers:
  - PDMA0 and PDMA1 can be configured as secure or non-secure PDMA
  - PDMA2 and PDMA3 can be configured as non-secure or SubM PDMA
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and UART, QSPI, SPI, EPWM, I^2C, I^2S, Timer and EADC request
- Supports Scatter-gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports time-out function
- Supports stride function from channel 0 to channel 5
- Supports enhanced stride function on channel 0 and channel1

6.17 Timer Controller (TMR)

6.17.1 Overview

The timer controller includes 12 sets of 32-bit timers, Timer0 ~ Timer11, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

The timer controller also provides twelve PWM generators. Each PWM generator supports two PWM output channels in independent mode and complementary mode. The output state of PWM output pin can be control by pin mask, polarity and break control, and dead-time generator.

6.17.2 Features

6.17.2.1 *Timer Function Features*

- 12 sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Supports Timer0 ~ Timer11 time-out interrupt signal or capture interrupt signal to trigger EPWM, EADC and PDMA function
- Supports internal capture triggered from internal clock (HIRC, LIRC) or external clock (HXT, LXT)
- Supports Inter-Timer trigger mode

6.17.2.2 *PWM Function Features*

- Supports maximum clock frequency up to maximum PCLK
- Supports independent mode for PWM generator with two output channels
- Supports complementary mode for PWM generator with paired PWM output channel
  - 12-bit dead-time insertion with 12-bit prescale
- Supports 12-bit prescale from 1 to 4096
- Supports 16-bit PWM counter
  - Up, down and up-down count operation type
  - One-shot or auto-reload counter operation mode
- Supports mask function and tri-state enable for each PWM output pin
- Supports brake function

- Brake source from pin, analog comparator and system safety events (clock failed, LVD interrupt flag detection and CPU lockup)
- Brake pin noise filter control for brake source
- Edge detect brake source to control brake state until brake status cleared
- Level detect brake source to auto recover function after brake condition removed

- Supports interrupt on the following events:
  - PWM zero point, period point, up-count compared or down-count compared point events
  - Brake condition happened
- Supports trigger EADC on the following events:
  - PWM zero point, period, zero or period point, up-count compared or down-count compared point events

6.18 EPWM Generator and Capture Timer (EPWM)

6.18.1 Overview

The chip provides three EPWM generators — EPWM0, EPWM1 and EPWM2. Each EPWM supports 6 channels of EPWM output or input capture. There is a 12-bit prescaler to supports flexible clock to the 16-bit EPWM counter with 16-bit comparator. The EPWM counter supports up, down and up-down counter types. EPWM uses comparator compared with counter to generate events. These events use to generate EPWM pulse, interrupt and trigger signal for EADC to start conversion.

The EPWM generator supports two standard EPWM output modes: Independent mode and Complementary mode, they have difference architecture. There are two output functions based on standard output modes: Group function and Synchronous function. Group function can be enabled under Independent mode or complementary mode. Synchronous function only enabled under complementary mode. Complementary mode has two comparators to generate various EPWM pulse with 12-bit dead-time generator and another free trigger comparator to generate trigger signal for EADC. For EPWM output control unit, it supports polarity output, independent pin mask and brake functions.

The EPWM generator also supports input capture function. It supports latch EPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition happened. Capture function also supports PDMA to transfer captured data to memory.

6.18.2 Features

6.18.2.1 *EPWM Function Features*

- Supports maximum clock frequency up to maximum PLL frequency
- Supports up to three EPWM modules, each module provides 6 output channels
- Supports independent mode for EPWM output/Capture input channel
- Supports complementary mode for 3 complementary paired EPWM output channel
  - Dead-time insertion with 12-bit resolution
  - Synchronous function for phase control
  - Two compared values during one period
- Supports 12-bit prescaler from 1 to 4096
- Supports 16-bit resolution EPWM counter
  - Up, down and up/down counter operation type
- Supports one-shot or auto-reload counter operation mode
- Supports group function
- Supports mask function and tri-state enable for each EPWM pin
- Supports trigger EADC on the following events:
  - EPWM counter matches 0, period value or compared value
  - EPWM counter matches free trigger comparator compared value (only for EADC)
  - Supports EPWM trigger EADC event prescaler feature
- Supports EPWM output accumulator stop counter mode
- Supports Fault Detect Function.
- Supports brake function

  - Brake source from pin, analog comparator and system safety events (clock failed, LVDIF detection and CPU lockup).
  - Noise filter for brake source from pin
  - Leading edge blanking (LEB) function for brake source from analog comparator
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed
- Supports synchronous function
- Supports interrupt on the following events:
  - EPWM counter matches 0, period value or compared value
  - Brake condition happened

6.18.2.2 *Capture Function Features*

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option
- Supports PDMA transfer function for all EPWM channels

6.19 Enhanced Input Capture Timer (ECAP)

6.19.1 Overview

This device provides up to three units of Input Capture Timer/Counter whose capture function can detect the digital edge-changed signal at channel inputs. Each unit has three input capture channels. The timer/counter is equipped with up counting, reload and compare-match capabilities.

6.19.2 Features

- Up to three Input Capture Timer/Counter units, CAP0, CAP1 and CAP2.
- Each unit has 3 input channels.
- Each unit has its own interrupt vector.
- Each input channel has its own capture counter hold register.
- 24-bit Input Capture up-counting timer/counter.
- With noise filter in front end of input ports.
- Edge detector with three options:
  - Rising edge detection
  - Falling edge detection
  - Both edge detection
- Captured events reset and/or reload capture counter.
- Supports compare-match function.

6.20 Quadrature Encoder Interface (QEI)

6.20.1 Overview

There are three Quadrature Encoder Interfaces (QEI) QEI controllers in this device. The QEI decodes speed of rotation and motion sensor information and can be used in any application that uses a quadrature encoder for feedback.

6.20.2 Features

6.20.2.1 *Quadrature Encoder Interface (QEI) Features*

- Up to three QEI controllers, QEI0, QEI1 and QEI2.
- Two QEI phase inputs, QEA and QEB; One Index input.
- A 32-bit up/down Quadrature Encoder Pulse Counter (QEI_CNT)
- A 32-bit software-latch Quadrature Encoder Pulse Counter Hold Register (QEI_CNTHOLD)
- A 32-bit Quadrature Encoder Pulse Counter Index Latch Register (QEI_CNTLATCH)
- A 32-bit Quadrature Encoder Pulse Counter Compare Register (QEI_CNTCMP) with a Pre-set Maximum Count Register (QEI_CNTMAX)
- One QEI control register (QEI_CTL) and one QEI Status Register (QEI_STATUS)
- Four Quadrature encoder pulse counter operation modes
  - Supports x4 free-counting mode
  - Supports x2 free-counting mode
  - Supports x4 compare-counting mode
  - Supports x2 compare-counting mode
- Encoder Pulse Width measurement mode
- Input frequency of QEA/QEB/IDX without noise filter must lower than PCLK/4
- Input frequency of QEA/QEB/IDX with noise filter must lower than Noise Filter Clk/8

6.21 Watchdog Timer (WDT)

6.21.1 Overview

The Watchdog Timer (WDT) is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake up system from Idle/Power-down mode.

6.21.2 Features

- Three Watchdogs, one for TrustZone Secure (TZS), one for TrustZone Secure/Non-Secure (TZS/TZNS) and the other for SubM
- 20-bit free running up counter for WDT time-out interval.
- Selectable time-out interval (2^4 ~ 2^{20}) and the time-out interval is 0.5 ms ~ 32.768 s if WDT_CLK = 32 kHz.
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026, 130, 18 or 3 WDT_CLK reset delay period.
- Supports to force WDT1 enabled after chip powered on or reset by setting Power-on Setting [2]
- Supports WDT time-out wake-up function.
- WDT0 can reset both real time Cortex-A35 and real time Cortex-M4 sub-systems.
- WDT1 can reset real time Cortex-A35 sub-system when WDT1RSTAEN (SYS_MISCRFCR[16]) is set.
- WDT1 can reset real time Cortex-M4 sub-system when WDT1RSTMEN (SYS_MISCRFCR[18]) is set.
- WDT2 can reset Cortex-M4 sub-system.
- WDT2 can reset Cortex-A35 sub-system when WDT2RSTAEN(SYS_MISCRFCR[17]) is set.

6.22 Window Watchdog Timer (WWDT)

6.22.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software running to uncontrollable status by any unpredictable condition.

6.22.2 Features

- Three Window Watchdogs, one for TrustZone Secure (TZS), one for TrustZone Secure/Non-Secure (TZS/TZNS) and the other for SubM
- 6-bit down counter value (CNTDAT, WWDT_CNT[5:0]) and 6-bit compare value (CMPDAT, WWDT_CTL[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value (PSCSEL, WWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode
- WWDT0 can reset both real time Cortex-A35 and real time Cortex-M4 sub-systems
- WWDT1 can reset real time Cortex-A35 sub-system when WDT1RSTAEN (SYS_MISCRFCR[16]) is set
- WWDT1 can reset real time Cortex-M4 sub-system when WDT1RSTMEN (SYS_MISCRFCR[18]) is set
- WWDT2 can reset Cortex-M4 sub-system
- WWDT2 can reset Cortex-A35 sub-system when WDT2RSTAEN(SYS_MISCRFCR[17]) is set

6.23 Real Time Clock (RTC)

6.23.1 Overview

The Real Time Clock (RTC) controller provides the real time and calendar message. The RTC offers programmable time tick and alarm match interrupts. The data format of time and calendar messages are expressed in BCD format. A digital frequency compensation feature is available to compensate external crystal oscillator frequency accuracy.

6.23.2 Features

- Supports external power pin V_{BAT}.
- Supports real time counter in RTC_TIME (hour, minute, second) and calendar counter in RTC_CAL (year, month, day) for RTC time and calendar check.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in RTC_TALM and RTC_CALM.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) mask enable in RTC_TAMSK and RTC_CAMSK.
- Selectable 12-hour or 24-hour time scale in RTC_CLKFMT register.
-
- Supports Leap Year indication in RTC_LEAPYEAR register.
- Supports Day of the Week counter in RTC_WEEKDAY register.
- Frequency of RTC clock source compensate by RTC_FREQADJ register.
- All time and calendar message expressed in BCD format.
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second.
- Supports RTC Time Tick and Alarm Match interrupt.
- Supports 32 kHz clock output.
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated.
- Supports 1 pairs dynamic loop tamper pin or 2 individual tamper pins.
- Built-in LXT frequency monitor.
- Supports 64 bytes spare registers and tamper pins detection to clear the content of these spare registers.

6.24 UART Interface Controller (UART)

6.24.1 Overview

The chip provides seventeen channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs serial-to-parallel conversion on data received from the peripheral and parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports ten types of interrupts. The UART controller supports flow control function. The UART controller also supports IrDA SIR, RS-485, and Single-wire function modes and auto-baud rate measuring function.

6.24.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 32/32 bytes entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART_TOUT [15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
  - Support 9600 bps for UART_CLK is selected LXT.
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - Supports for 3/16 bit duration for normal mode
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports PDMA transfer function
- Support Single-wire function mode.

UART Feature	UART0		UART1 ~ UART16	
FIFO	32 Bytes		32 Bytes	

Processor	A35		M4	
Auto Flow Control (CTS/RTS)	√		√	
IrDA	√		√	
RS-485 Function Mode	√		√	
nCTS Wake-up	√		√	
Incoming Data Wake-up	√		√	
Received Data FIFO reached threshold Wake-up	√		√	
RS-485 Address Match (AAD mode) Wake-up	√		√	
Received Data FIFO reached threshold Time-out Wake-up	√		√	
Baud Rate Compensation	√		√	
Auto-Baud Rate Measurement	√		√	
STOP Bit Length	1, 1.5, 2 bits		1, 1.5, 2 bits	
Word Length	5, 6, 7, 8 bits		5, 6, 7, 8 bits	
Even / Odd Parity	√		√	
Stick Bit	√		√	

Table 6.24-1 NuMicro MA35D1 Series UART Features

6.25 Smart Card Host Interface (SC)

6.25.1 Overview

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal. It can also be set as UART mode to communicate with other devices.

6.25.2 Features

- ISO 7816-3 T = 0, T = 1 compliant
- EMV2000 compliant
- Two ISO 7816-3 ports
- Separates receive/transmit 4-byte entry FIFO for data payloads
- Programmable transmission clock frequency
- Programmable receiver buffer trigger level
- Programmable guard time selection (11 ETU ~ 267 ETU)
- One 24-bit timer and two 8-bit timers for Answer to Request (ATR) and waiting times processing
- Supports auto direct / inverse convention function
- Supports transmitter and receiver error retry and error number limiting function
- Supports hardware activation sequence process, and the time between PWR on and CLK start is configurable
- Supports hardware warm reset sequence process
- Supports hardware deactivation sequence process
- Supports hardware auto deactivation sequence when detected the card removal
- Supports UART mode
  - Full duplex, asynchronous communications
  - Separates receiving / transmitting 4-byte entry FIFO for data payloads
  - Supports programmable baud rate generator
  - Supports programmable receiver buffer trigger level
  - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting EGT (SCn_EGT[7:0])
  - Programmable even, odd or no parity bit generation and detection
  - Programmable stop bit, 1- or 2- stop bit generation

6.26 I^2C Serial Interface Controller (I^2C)

6.26.1 Overview

I^2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I^2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are six sets of I^2C controllers that support Power-down wake-up function.

6.26.2 Features

The I^2C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I^2C bus include:

- Supports up to six I^2C ports
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflow
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing and 10-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports PDMA with one buffer capability
- Supports setup/hold time programmable

6.27 Serial Peripheral Interface (SPI)

6.27.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains up to four sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each SPI controller can be configured as a master or a slave device and supports the PDMA function to access the data buffer. Each SPI controller also supports I²S mode to connect external audio CODEC.

6.27.2 Features

- SPI Mode
  - Up to four sets of SPI controllers
  - Supports Master or Slave mode operation
  - Configurable bit length of a transaction word from 8 to 32-bit
  - For SPI PDMA function disable, provides separate 8-level of 32-bit (or 16-level of 16-bit) transmit and receive FIFO buffers which depended on SPI setting of data width
  - For SPI PDMA function enable, provides separate 8-level of 32-bit (or 16-level of 16-bit or 32-level of 8-bit) transmit and receive FIFO buffers which depended on SPI setting of data width
  - Supports MSB first or LSB first transfer sequence
  - Supports Byte Reorder function
  - Supports Byte or Word Suspend mode
  - Supports PDMA transfer
  - Supports 3-Wire, no slave selection signal, bi-direction interface
  - Supports one data channel half-duplex transfer
  - Supports receive-only mode
- I²S Mode
  - Supports Master or Slave
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Each provides two 8-level FIFO data buffers, one for transmitting and the other for receiving
  - Supports monaural and stereo audio data
  - Supports PCM mode A, PCM mode B, I²S and MSB justified data format
  - Supports two PDMA requests, one for transmitting and the other for receiving

6.28 Quad Serial Peripheral Interface (QSPI)

6.28.1 Overview

The Quad Serial Peripheral Interface (QSPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains two QSPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device.

The QSPI controller supports 2-bit transfer mode to perform full-duplex 2-bit data transfer and also supports Dual and Quad I/O transfer mode and the controller supports the PDMA function to access the data buffer.

6.28.2 Features

- Up to two sets of QSPI controllers
- Supports Master or Slave mode operation
- Supports 2-bit transfer mode
- Supports Dual and Quad I/O transfer mode
- Configurable bit length of a transaction word from 8 to 32-bit
- For SPI PDMA function disable, provides separate 8-level of 32-bit transmit and receive FIFO buffers
- For SPI PDMA function enable, provides separate 8-level of 32-bit (or 16-level of 16-bit or 32-level of 8-bit) transmit and receive FIFO buffers which depended on SPI setting of data width
- Supports MSB first or LSB first transfer sequence
- Supports Byte Reorder function
- Supports Byte or Word Suspend mode
- Supports PDMA transfer
- Supports 3-Wire, no slave selection signal, bi-direction interface
- Supports one data channel half-duplex transfer
- Supports Double Transfer Rate Mode (DTR mode) for SPI master mode
- Supports receive-only mode

6.29 I²S Controller (I²S)

6.29.1 Overview

The I²S controller consists of I²S protocol to interface with external audio CODEC. Two 16-level depth FIFO for reading path and writing path respectively are capable of handling 8/16/24/32 bits audio data sizes. A PDMA controller handles the data movement between FIFO and memory.

6.29.2 Features

- Supports Master mode and Slave mode
- Capable of handling 8, 16, 24 and 32 bits data sizes in each audio channel
- Supports monaural and stereo audio data
- Supports I²S protocols: Philips standard, MSB-justified, and LSB-justified data format
- Supports PCM protocols: PCM standard, MSB-justified, and LSB-justified data format
- PCM protocol supports TDM multi-channel transmission in one audio sample, and the number of data channel can be set as 2, 4, 6, or 8
- Provides two 16-level FIFO data buffers, one for transmitting and the other for receiving
- Generates interrupt requests when buffer levels cross a programmable boundary
- Supports two PDMA requests, one for transmitting and the other for receiving

6.30 High Speed USB 2.0 Device Controller (HSUSBD)

6.30.1 Overview

This chip is equipped with a USB 2.0 HS/FS Device Controller. The USB Device Controller interfaces the AHB bus and the UTMI bus. The USB Device Controller contains both the AHB master interface and AHB slave interface. CPU programs the USB Device Controller control and status registers through the AHB slave interface. The USB Device Controller is complaint with USB 2.0 specification and it contains 8 bidirectional endpoints in addition to control endpoint. These endpoints could be configured to BULK, INTERRUPT or ISOCHRONOUS. The USB Device Controller has a built-in DMA to relieve the load of CPU.

6.30.2 Features

- Compliant with Universal Serial Bus (USB) Specification Revision 2.0.
- Supports up to eight bidirectional endpoints, in addition to control endpoint 0.
- Supports Control, Bulk, Interrupt, Isochronous transfers.
- Supports Descriptor (Scatter gather) DMA operation.
- Supports LPM feature.
- Supports V_{BUS}/Resume wake-up from system power-down mode.

6.31 USB 2.0 Host Controller (HSUSBH)

6.31.1 Overview

This chip is equipped with two individual USB 2.0 HS Host Controllers (HSUSBH0, HSUSBH1) that support Enhanced Host Controller Interface (EHCI) Specification, a register-level description of a host controller, to manage the devices and data transfer of Universal Serial Bus (USB).

Each HSUSBH supports an integrated Root Hub with a USB port, a DMA for real-time data transfer between system memory and USB bus, port power control and port overcurrent detection.

Each HSUSBH is responsible for detecting the connect and disconnect of USB devices, managing data transfer, collecting status and activity of USB bus, providing power control and detecting overcurrent of attached USB devices.

6.31.2 Features

- Compliant with Universal Serial Bus (USB) Specification Revision 2.0.
- Supports Enhanced Host Controller Interface (EHCI) Specification Revision 1.0.
- Supports high-speed (480Mbps) USB devices.
- Supports Control, Bulk, Interrupt, Isochronous and Split transfers.
- Supports an integrated Root Hub.
- Supports a port routing logic to route full/low speed device to OHCI controller.
- Supports port power control and port overcurrent detection.
- Supports DMA for real-time data transfer.
- Supports dual-role switching with the USB 2.0 Device Controller (for HSUSBH0 only).

6.32 USB 1.1 Host Controller (USBH)

6.32.1 Overview

This chip is equipped with two USB 1.1 FS Host Controller (USBH) that supports Open Host Controller Interface (OpenHCI, OHCI) Specification, a register-level description of a host controller, to manage the devices and data transfer of Universal Serial Bus (USB). USBH0 and USBH1 are the companion host controller of HSUSBH0 and HSUSBH1 respectively.

Each USBH supports an integrated Root Hub with a USB port, a DMA for real-time data transfer between system memory and USB bus, port power control and port overcurrent detection.

The USBH is responsible for detecting the connect and disconnect of USB devices, managing data transfer, collecting status and activity of USB bus, providing power control and detecting overcurrent of attached USB devices.

6.32.2 Features

- Compliant with Universal Serial Bus (USB) Specification Revision 2.0.
- Supports Open Host Controller Interface (OpenHCI) Specification Revision 1.0.
- Supports full-speed (12Mbps) and low-speed (1.5Mbps) USB devices.
- Supports Control, Bulk, Interrupt, Isochronous and Split transfers.
- Supports an integrated Root Hub.
- Supports port power control and port overcurrent detection.
- Supports DMA for real-time data transfer.

6.33 Controller Area Network with Feasibility Data Rate (CAN FD)

6.33.1 Overview

The CAN FD controller performs communication according to ISO 11898-1:2015 and need be connected to additional transceiver hardware for the physical layer.

The CAN FD controller consists of one CAN Core, Memory access control and arbiter, Tx Handler, Rx Handler, a shared Message RAM memory and a 32-bit AHB interface for control and configuration registers.

The message storage is intended to be a single-ported Message RAM outside of the CAN Core module. It is connected to the CAN Core via the memory control interface. The Message RAM implements filters, receive FIFOs, transmit event FIFOs and transmit FIFOs.

All functions concerning the handling of messages are implemented by the Rx Handler and the Tx Handler. The Rx Handler manages message acceptance filtering, the transfer of received messages from the CAN Core to the Message RAM as well as providing received message status information. The Tx Handler is responsible for the transfer of transmit messages from the Message RAM to the CAN Core as well as providing transmitted status information.

The controller's clock domain concept allows the separation among CAN Core clock and the AHB clock.

6.33.2 Features

- Conform with CAN protocol version 2.0 part A, B and ISO 11898-1: 2015
- CAN FD with up to 64 data bytes supported
- CAN Error Logging
- AUTOSAR support
- SAE J1939 support
- Improved acceptance filtering
- Two configurable Receive FIFOs
- Separate signaling on reception of High Priority Messages
- Configurable Transmit FIFO, Transmit Queue, Transmit Event FIFO
- Direct Message RAM access for CPU
- Programmable loop-back test mode
- Maskable module interrupts
- Two clock domains (CAN Core clock and AHB clock)
- Power-down support

6.34 Gigabit Media Access Controller (GMAC)

6.34.1 Overview

The GMAC enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2008 standard. This chip only supports Reduced Gigabit Media Independent Interface (RGMII) and Reduced Media Independent Interface (RMII) interfaces.

The GMAC is compliant with the following standards:

- IEEE 802.3-2008 for Ethernet MAC
- IEEE 1588-2008 standard for precision networked clock synchronization
- IEEE 802.3az-2010, for Energy Efficient Ethernet (EEE)
- AMBA 2.0 for AHB slave port
- AMBA 3.0 for AXI master port
- RGMII specification version 2.6 from HP/Marvell
- RMII specification version 1.2 from RMII consortium

6.34.2 Features

- 10, 100, and 1000 Mbps data transfer rates with the following PHY interfaces:
  - RGMII interface to communicate with an external gigabit PHY
  - RMII interface to communicate with an external Fast Ethernet PHY
- Full-duplex operation:
  - IEEE 802.3x flow control automatic transmission of zero-quanta Pause frame on flow control input de-assertion
  - Forwarding of received Pause frames to the user application
- Half-duplex operation:
  - CSMA/CD Protocol support
  - Flow control using backpressure support
  - Frame bursting and frame extension in 1000 Mbps half-duplex operation
- Preamble and start of frame data (SFD) insertion in Transmit path
- Preamble and SFD deletion in the Receive path
- Automatic CRC and pad generation controllable on a per-frame basis
- Automatic Pad and CRC Stripping options for receive frames
- Programmable frame length to support Standard or Jumbo Ethernet frames with up to 16 Kbytes of size
- Programmable Interframe Gap (IFG) (40-96 bit times in steps of 8)
- Option to transmit frames with reduced preamble size
- Separate 32-bit status for transmit and receive packets
- IEEE 802.1Q VLAN tag detection for reception frames
- Separate transmission, reception, and control interfaces to the application

- Receive module for checksum off-load for received IPv4 and TCP packets encapsulated by the Ethernet frame (Type 1)
- Enhanced Receive module for checking IPv4 header checksum and TCP, UDP, or ICMP checksum encapsulated in IPv4 or IPv6 datagrams (Type 2)
- Support Ethernet frame timestamping as described in IEEE 1588-2002 and IEEE 1588-2008

  The 64-bit timestamps are given in the transmit or receive status of each frame
- MDIO master interface for PHY device configuration and management
- Standard IEEE 802.3az-2010 for Energy Efficient Ethernet
- Flexibility to control the Pulse-Per-Second (PPS) output signal (ptp_pps_o)
- CRC replacement, Source Address field insertion or replacement, and VLAN insertion, replacement, and deletion in transmitted frames with per-frame control
- Programmable watchdog timeout limit in the receive path

6.35 Secure Digital Host Controller (SDH)

6.35.1 Overview

The Secure Digital Host Controller (SD Host) has DMA engine, host controller registers, FIFO controller and SD/UHS-I/eMMC unit. The DMA engine provides a DMA (Direct Memory Access) function for SD to exchange data between system memory and shared buffer, and DMA options such as SDMA(Single operation DMA), ADMA2 (Advanced DMA) as specified in the SD host controller standard. The SD host controller can support SD or eMMC specification and cooperate with the DMA engine to provide a fast data transfer between system memory and cards.

6.35.2 Features

- AMBA AHB master/slave interface compatible, for data transfer and register read/write.
- Supports data transfer types such as CPU, SDMA, ADMA2 for SD, eMMC mode.
- Supports 1-bit and 4-bit data bus widths for the SD memory card specification version 3.0. (SDR104 speed limited to maximum allowed I/O speed. SPI mode, DDR50 and UHS-II mode not supported).
- Supports 1-bit, 4-bit and 8-bit data bus widths for the eMMC interface. (HS200 speed limited to maximum allowed I/O speed and HS400 is not supported).
- Supports SD/SDHC/SDXC/SDIO, eMMC card.
- Supports gating of controller base clock if host controller is inactive.
- Supports two set of SD host controllers, only one can support UHS-I mode.
- Supports SD/eMMC tuning, CMD19(SD) or CMD21(eMMC).
- Supports 50 MHz to achieve SD 25 Mbyte/s for 4-bit mode.
- Supports 200 MHz to achieve eMMC HS200 at 1.8V I/O operation.

6.36 NAND Flash Interface (NFI)

6.36.1 Overview

The NAND Flash Interface of this chip has DMA unit and NAND Flash unit. The DMA unit provides a DMA (Direct Memory Access) function for NFI to exchange data between system memory (e.g. SDRAM) and shared buffer (128 bytes), and the NAND Flash unit control the interface of NAND Flash. The interface controller can support NAND-type Flash and the NFI is cooperated with DMAC to provide a fast data transfer between system memory and cards.

6.36.2 Features

- Supports single DMA channel and address in non-word boundary
- Supports hardware Scatter-Gather function
- Supports 128 bytes shared buffer for data exchange between system memory and Flash device (Separated into two 64 bytes ping-pong FIFO)
- Supports SLC and MLC NAND type Flash
- Adjustable NAND page sizes. (2048B+spare area, 4096B+spare area and 8192B+spare area)
- Supports up to 8-bit/12-bit /24-bit hardware ECC calculation circuit to protect data communication
- Supports programmable NAND timing cycle
- Supports EDO mode

6.37 Cryptographic Accelerator (CRYPTO)

6.37.1 Overview

The Crypto (Cryptographic Accelerator) includes a secure pseudo random number generator (PRNG) core and supports AES, SHA/HMAC, RSA, and ECC algorithms.

The PRNG core supports 128, 163, 192, 224, 233, 255, 256, 283, 384, 409, 512, 521 and 571 bits random number generation. (283~571 bits are only generated for Key Store).

The AES accelerator is an implementation fully compliant with the AES (Advance Encryption Standard) encryption and decryption algorithm. The AES accelerator supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2, CBC-CS3, CCM and GCM mode.

The SHA accelerator is an implementation fully compliant with the MD5, SM3, SHA-160, SHA-224, SHA-256, SHA-384, SHA-512, SHA-512/t, SHA3 and corresponding HMAC (Keyed-Hash Message Authentication Code) algorithms, except for SHAKE128 and SHAKE256.

The ECC accelerator is an implementation fully compliant with elliptic curve cryptography by using polynomial basis in binary field and prime filed.

The RSA accelerator is an implementation fully compliant with RSA cryptography, CRT decryption algorithm, side-channel attack countermeasures and CRT fault injection attack countermeasure algorithm.

The Crypto can get key from Key Store and/or put the key to Key Store determined by the function of each accelerator.

The Crypto supports one technique to improve power analysis protection ability.

6.37.2 Features

- PRNG
  - Supports 128, 163, 192, 224, 233, 255, 256, 283, 384, 409, 512, 521 and 571 bits random number generation (283~571 bits are only generated for Key Store).
  - Can take the true random number seed from TRNG
  - Can take the true random number from TRNG (only for Key Store)
- AES
  - Supports FIPS NIST 197
  - Supports SP800-38A and addendum
  - Supports 128, 192, and 256 bits key
  - Supports both encryption and decryption
  - Supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2 and CBC-CS3 modes
  - Supports CCM mode, GCM mode and GMAC function
  - Supports SM4 block cipher algorithm
  - Supports key expander for key expansion in FIPS NIST 197
  - Supports three techniques to improve side-channel attack protection ability
  - Supports five techniques to improve advance side-channel attack protection ability for differential fault analysis (DFA), collision-correlation attack (CCA), and template based attack (TA)
- SHA

- Supports FIPS NIST 180, 180-2, 180-4
- Supports MD5
- Supports SHA-160, SHA-224, SHA-256, SHA-384, SHA-512 and SHA-512/t
- Supports SHA3-224, SHA3-256, SHA3-384, SHA3-512, SHAKE128 and SHAKE256
- Supports SM3 Cryptographic Hash Algorithm

- HMAC
  - Supports FIPS NIST 180, 180-2, 180-4
  - Supports HMAC-MD5
  - Supports HMAC-SHA-160, HMAC-SHA-224, HMAC-SHA-256, HMAC-SHA-384, and HMAC-SHA-512
  - Supports HMAC-SHA3-224, HMAC-SHA3-256, HMAC-SHA3-384, and HMAC-SHA3-512
- ECC
  - Supports both prime field GF(p) and binary filed GF(2^m)
  - Supports NIST P-192, P-224, P-256, P-384, and P-521
  - Supports NIST B-163, B-233, B-283, B-409, and B-571
  - Supports NIST K-163, K-233, K-283, K-409, and K-571
  - Supports Curve25519
  - Supports Public Key Cryptographic Algorithm SM2 Based on Elliptic Curves
  - Supports point multiplication, addition and doubling operations in GF(p) and GF(2^m)
  - Supports modulus division, multiplication, addition and subtraction operations in GF(p)
  - Supports three techniques to improve side-channel attack protection ability
  - Supports three techniques to improve advance side-channel attack protection ability for differential fault attack (DFA), differential power analysis (DPA) and correlation power analysis (CPA)
- RSA
  - Supports both encryption and decryption with 1024, 2048, 3072 and 4096 bits
  - Supports CRT decryption with 2048, 3072 and 4096 bits
  - Supports three techniques to improve side-channel attack protection ability
  - Supports one technique to improve CRT fault injection attack protection ability

6.38 Key Store (KS)

6.38.1 Overview

The Key Store (KS) is a key management device with 4 Kbytes SRAM and OTP for key storage. The Key Store is capable of providing a crypto engine to access or store the key while encryption, decryption and generation. The Key Store supports revoke key operation if key is unused. The Key Store is able to protect the key by data scrambling, data remanence prevention and silent access.

6.38.2 Features

- Supports programming interface for key management
- Supports key size required for Cryptography from 128 bits to 4096 bits
- Supports 32 SRAM keys by 4 Kbytes SRAM
- Supports 9 OTP keys of which key 0~2 are 128-bits and key 3~8 are 256-bits
- Supports crypto engine access or store key in Key Store directly
- Supports ECDH operation with ECC and PRNG engine
- Supports to store middle data for RSA CRT and SCAP mode
- Supports revoke operation
- Supports erase key in SRAM and revoke key in OTP while tamper detected
- Supports integrity checking
- Supports data scrambling
- Supports data remanence prevention at SRAM
- Supports silent access for side-channel protection at SRAM

6.39 Camera Capture Interface Controller (CCAP)

6.39.1 Overview

The camera capture interface controller (CCAP) is designed to capture image data from a sensor. After capturing or fetching image data, it will process the image data, and then the embedded DMA controller will move the data from the internal FIFO to system memory with AHB bus.

6.39.2 Features

- CCIR601 and CCIR656 and 4-bit interfaces supported for connection to CMOS image sensor
- 8-bit YUV422 and 8-bit RGB565 color format supported for data-in from CMOS sensor
- 8-bit/4-bit monochrome format supported for data-in from CMOS sensor
- 8-bit/10-bit raw Bayer format supported for data-in from CMOS sensor
- YUV422, RGB565, RGB555 and Y-only color supported for packet data output.
- Single interrupt source to interrupt controller from maskable interrupt source: Address Match, Bus Master Transfer Error, Video Frame End
- Embedded DMA controller supported to transfer data from internal FIFO to system memory through AHB bus
- Supports YUV422 and YUV420 planar data output
- CROP function supported to crop input image to the required size for digital application.
- Frame rate scaling-down supported
- Image scaling-down supported
- Bit luma output with 8-bit threshold setting supported.

6.40 LCD Display Controller (DISP)

6.40.1 Overview

The Vivante DCUltraLite (DCUltraL) display controller (DISP) IP defines a high-performance optimized-area display core that can be used for reading rendered images from the frame buffer to the display. In addition to providing hardware cursor patterns, the display controller performs format conversions, dithering and gamma corrections. This controller includes support for parallel pixel output and is easily adapted to external serialization logic, for example HDMI. This document contains copyright confidential and proprietary material disclosed with permission of Vivante Corporation. Vivante has authorized re-distribution of this material restricted to those NDA partners and licensees of Nuvoton who are engineering MPU product which includes the discussed Vivante IP. All rights reserved.

6.40.2 Features

- Video Timing Generation
  - HSYNC, VSYNC, DE signals
  - Programmable timers
- Sync Interface
  - Parallel Pixel Output with 24-bit Data, HSync, VSync, Data enable
  - DPI 24-bit, 18-bit (2 configs) and 16-bit support (3 configs)
  - Easily adaptable to external serialization logic, e.g. HDMI
- MPU Interface
  - Support i80/m68 with 8, 9, 16, 18-bit system interface
  - Support VSYNC interface (output)
  - Support TE signal (input)
  - Support LCD chip register configuration by MPU interface
- Display
  - Single display
  - Maximum display size: 1080p
  - Sync and blank signals
  - Gamma and dither tables
- Input Formats
  - ARGB2101010,A/XRGB8888,A/XRGB1555,RGB565,A/XRGB4444
  - Index1/2/4/8
  - YUV422 packed and semi planar (YUY2, UYVY, NV16)
  - YUV420 semi-planar (YUY2(P010), NV12 and YUV420 semi-planar 10-bit)
- Format Conversion
  - Pixel inputs accepted from multiple RGB and YUV formats
  - Color Space Conversion BT.2020 and BT.709
  - Pixel output is 24 bit RGB in multiple formats
- Output Formats

- DPI_D16CFG1/DPI_D16CFG2/DPI_D16CFG3/DPI_D18CFG1/DPI_D18CFG2/ DPI_D24

- Hardware Cursor
  - Supports ARGB888 and Mask cursor formats
- Supports OSD function
- Color
  - A separate Look Up Table for Dither
  - A separate Look Up Table for Gamma Correction
  - Overlay with coordinate generator
  - Alpha Blending: 8 Porter Duff Blending modes

6.41 2D Graphic Engine (GFX)

6.41.1 Overview

Vivante GC520L composition processing core (CPC) IP defines a high-performance multi-pipe 2D raster graphics core that accelerates the 2D graphics display on a variety of consumer devices and provides advanced compression capabilities. Addressable screen sizes range from the smallest cell phones up to 1080p displays.

6.41.2 Features

- 2D
  - Bit Blit.
  - Stretch Blit.
  - Rectangle fill and clear.
  - Line drawing.
  - Filter Blit.
  - Mono expansion for text rendering.
  - ROP2, ROP3 and ROP4.
  - Alpha blending, including Java 2 Porter-Duff compositing blending rules.
  - 32K x 32K coordinate system.
  - 90 / 180 / 270 degree rotation.
  - Transparency by monochrome mask, chroma key, or pattern mask.
  - Supports 2x2 in 4x4 tile format.
  - Supports XMajor and YMajor Super Tile 64x64 format.
  - Supports Fast Clear when reading Super Tiled source.
  - A8 output with rotation in filter blit and bit blit.
  - Supports Src/Dest color key full bypass.
- Multi Source Blending
  - Supports Multi source blending with variable block size to improve BW and reduce SW overhead.
  - Supports up to 8 sources.
  - Programmable block size guarantees cache efficiency so each source is read once and each destination is written once.
  - Supports 90, 180, 270 degree rotation with different block size for higher cache efficiency.
- YUV Support
  - Supports Full Multi destination for converting non-planar YUV formats to planar YUV. Used in extracting various components from the input color into different destination

planes.

  - Supports YUV422 output with alpha blending.

- Clock Disabling
  - The core clock enters the frequency scaling block, and a clock with missing pulses is output, buffered, and sent to clock gating logic. The clock gate output will be used by the 2D GFX blocks. The core clock can be shut down through software by setting the proper register bits.
- AXI Bus
  - AXI 4-bit ID, such that all Read and Write transactions have a unique AXI ID.
  - Supports AXI out of order read return.
- Additional Enhancements
  - Supports Full functional MMU with variable page size.

6.42 H.264/JPEG Decoder (VC8000NanoD)

6.42.1 Overview

The Hantro VC8000NanoD Multi-format Decoder is a single-core solution providing HD decoding for H.264 and JPE.G. It is one of the smallest multi-format video decoder IP solutions and offers low power consumption and negligible load on the host CPU. Dynamic power consumption is minimized by extensive use of multi-level hierarchical clock gating.

An optimized software stack and a comprehensive set of software development tools are supported by a robust pipeline designed for industry-standard codecs and Hantro APIs, and with full support for Linux embedded development platforms. Software for VC8000NanoD IP supports Hantro APIs for the following industry standard codecs: AVC (H.264), MVC, SVC, and JPE.G.

6.42.2 Features

- Video decoding
  - H.264 Decoder (Baseline/mainstream/High profile supported)
  - Single decoding pipeline: 1080p@30fps
  - Support picture size from 48x48 to 1920x1080
  - Support step size 16 pixels
  - Stream error detection
  - Support reference buffer
- JPEG decoding
  - JFIF file format: 1.02
  - Multiple input formats
  - YCbCr420 semi-planar raster scan output format
  - Support picture size from 48x48 to 16368x16368
  - Support step size 8 pixels
  - Stream error detection
  - JPEG compressed thumbnails supported
- Post Processing
  - Support image down-scaling
  - Support image up-scaling
  - Support YCbCr to RGB color conversion
  - Support dithering
  - Programmable alpha channel
  - Support alpha blending
  - Support deinterlacing

- Support contrast, brightness, and color saturation adjustment for RGB image
- Support image cropping and digital zoom
- Support picture in picture
- Support output image masking
- Support image rotation

6.43 Keypad Interface (KPI)

6.43.1 Overview

The Keypad Interface (**KPI**) is an APB slave with configurable minimum 2-row up to 8-row scan output and minimum 1-column up to 8-column scan input. Any keys in the array pressed or released are de-bounced and generate an interrupt.

The KPI supports release multiple keys, press multiple keys scan interrupt and specified INT3KEYs interrupt for chip reset. If the 3 pressed keys matches with the 3 keys defined in **KPI3KCONF**, it will generate an interrupt for chip reset depending on the **EN3KYRST (KPI3KCONF[24])** setting. The period of three key reset is 64 * KPI engine clock. The interrupt is generated whenever it detects any key in the keypad pressing or releasing or waking up from IDLE or three-key reset. User can know the interrupt source by querying KPISTATUS register.

6.43.2 Features

- Matrix keypad interface (maximum 8x8 array, and minimum 2x1array)
- Programmable de-bounce time
- Low-power wakeup mode
- Programmable three-key reset
- Generates interrupt and updates all the keys(maximum 64 keys, minimum 2 keys) information (press/release) every time the user pressing or releasing

6.44 Analog to Digital Converter (ADC)

6.44.1 Overview

The chip contains one 12-bit Successive Approximation Register analog-to-digital converter (SAR A/D converter) with 8 input channels. The A/D converter supports two operation modes: 4-wire or 5-wire mode. The ADC is especially suitable to act as touch screen controller.

6.44.2 Features

- Resolution: 12-bit resolution.
- DNL: +/-1.5 LSB, INL: +/-3 LSB.
- Maximum ADC clock frequency is 16 MHz
- Up to 727.2 KSPS conversion rate when ADC clock frequency is 16 MHz in high speed mode
- Up to 145.4 KSPS conversion rate when ADC clock frequency is 3.2 MHz in low speed mode
- Analog Input Range: V_{REF} to AGND, can be rail-to-rail.
- Analog Supply: 2.7~3.6V.
- Digital Supply: 0.99~1.21V.
- 8 Single-Ended analog inputs.
- Compatible with 4-wire or 5-wire Touch Screen Interface.
- Touch Pressure Measurement for 4-wire touch screen application.
- Low Power Consumption: 600uA (727.2 KSPS) / 300uA (145.4 KSPS)

6.45 Enhanced 12-bit Analog-to-Digital Converter (EADC)

6.45.1 Overview

The chip contains one 12-bit successive approximation analog-to-digital converter (SAR EADC converter) with 8 external input channels and 1 internal channel. The EADC converter can be started by software trigger, EPWM0/1/2 triggers, Timer0~11 overflow pulse triggers, ADINT0, ADINT1 interrupt EOC (End of conversion) pulse trigger and external pin (EADC0_ST) input signal.

6.45.2 Features

- Analog input voltage range: 0~V_{REF} (Max to 3.6V)
- Reference voltage from V_{REF} pin
- 12-bit resolution
- Up to 8 single-end analog external input channels and 4 pair differential analog input channels
- Up to 1 internal channel for Battery power (V_{BAT})
- Four EADC interrupts (ADINT0~3) with individual interrupt vector addresses
- Maximum EADC clock frequency of 80 MHz
- Up to 4.7 MSPS conversion rate when EADC clock frequency is 80 MHz in high speed mode
- Up to 941.1 KSPS conversion rate when EADC clock frequency is 16 MHz in low speed mode
- Configurable EADC internal sampling time
- Supports calibration function
- Supports internal reference voltage V_{REF}: 1.6V, 2.0V, 2.5V, and 3.0V
- Supports three power saving modes:
  - Deep Power-down mode
  - Power-down mode
  - Standby mode
- Up to 9 sample modules:
  - Each of sample modules which is configurable for EADC converter channel EADC_CH0~7 and trigger source
  - Sample module 8 is fixed for EADC channel 8 input source as battery power (V_{BAT})
  - Double buffer for sample control logic module 0~3
  - Configurable sampling time for each sample module
  - Conversion results are held in 9 data registers with valid and overrun indicators
- An EADC conversion can be started by:
  - Write 1 to SWTRG (EADC_SWTRG[n], n = 0~8)
  - External pin EADC0_ST
  - Timer0~11 overflow pulse triggers
  - ADINT0 and ADINT1 interrupt EOC (End of conversion) pulse triggers

  - EPWM triggers
- Supports PDMA transfer
- Conversion Result Monitor by Compare Mode

6.46 System Debug (CoreSight™ SoC-400)

6.46.1 Overview

The system debug component is based on the Arm CoreSight™ SoC-400 and provides the function to debug Cortex-A35 and Cortex-M4 at the same time.

6.46.2 Features

- Access to debug features and AHB matrix through a JTAG or Serial Wire Debug (SWD) interface.
- Merging of multiple trace sources (Cortex-A35 Core0 ETM, Cortex-A35 Core1 ETM, and Cortex-M4 ETM) into a single trace stream
- Capture of trace streams on-chip (4 Kbytes ETB) or off-chip (TPIU)
- Cross-triggering between different debug and trace components
- Timestamp generation and system-wide compressed timestamp distribution
- Supports debug authentication for TrustZone and resource isolation

7 APPLICATION CIRCUIT

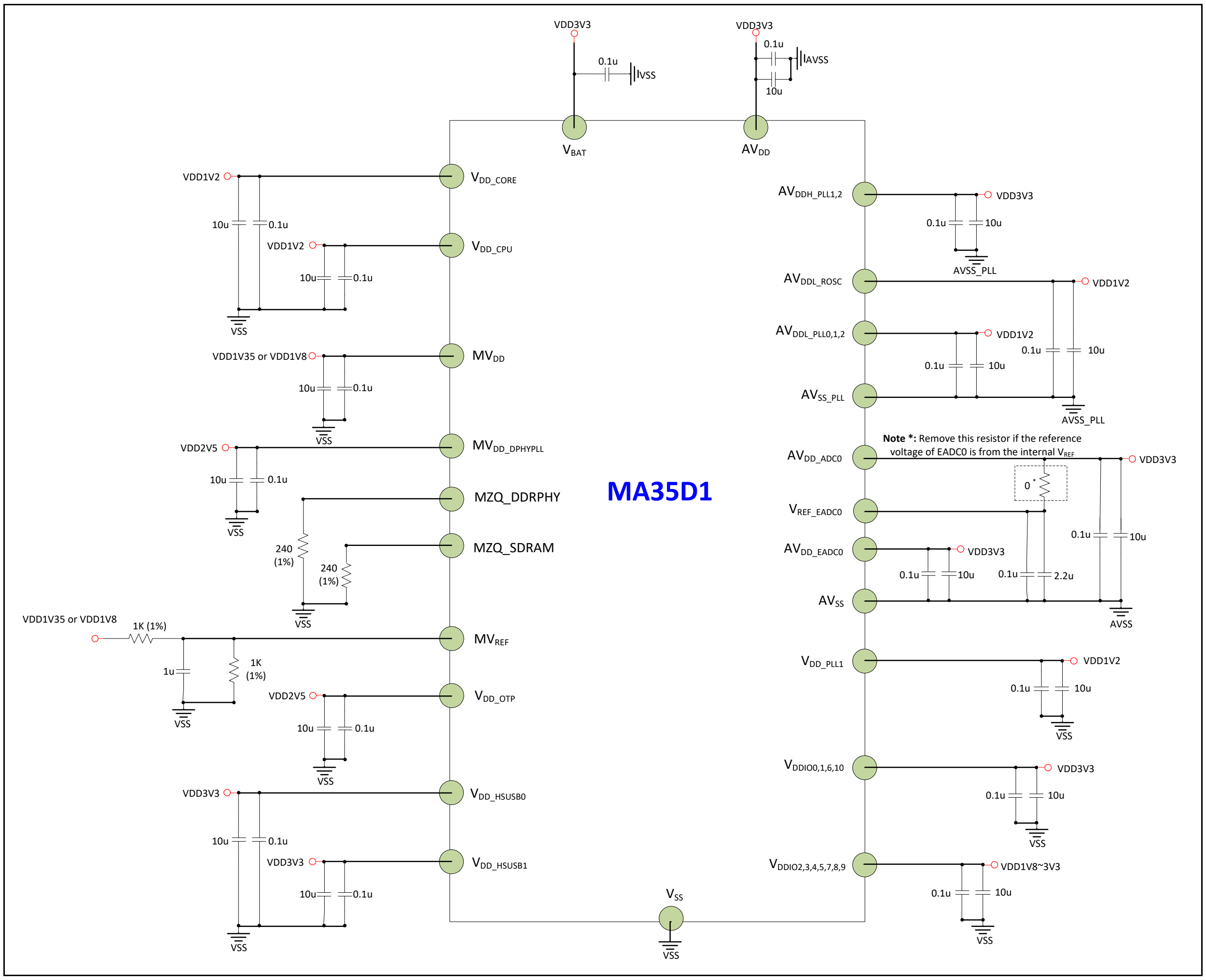


Figure 7-1 Application Circuit

Note: MV_{DD} is the power supply for internal DDR2/DDR3L-type SDRAM. Please refer to the part number from MA35D1 selection guide to supply the correct voltage on these pins. It is 1.8V for internal DDR2-type SDRAM or 1.35V for internal DDR3L-type SDRAM. $MV_{REF} = 1/2MV_{DD}$.

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

8.1.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD_CPU}-V_{SS} [*1]	CPU DC Power Supply Voltage	-0.3	1.50	V
V_{DD_LOW}-V_{SS} [*1]	Low Level DC Power Supply Voltage (V_{DD_LOW} including V_{DD_CPU}, V_{DD_CORE}, AV_{DDL_ROSC}, AV_{DDL_PLL0}, AV_{DDL_PLL1}, V_{DD_PLL1}, AV_{DDL_PLL2})	-0.3	1.36	V
V_{DD_MEDIUM}-V_{SS} [*1]	Medium Level DC Power Supply Voltage (V_{DD_MEDIUM} including $MV_{DD\_DPHYPLL}$, V_{DD_OTP})	-0.3	2.75	V
V_{DD_HIGH}-V_{SS} [*1]	High Level DC Power Supply Voltage (V_{DD_HIGH} including AV_{DD}, AV_{DD_ADC0}, AV_{DD_EADC0}, AV_{DDH_PLL1}, AV_{DDH_PLL2}, V_{DD_HSUSB0}, V_{DD_HSUSB1})	-0.3	4.0	V
V_{DDIOX}-V_{SS} [*1]	IO Power Supply Voltage (V_{DDIOX} inclduing V_{DDIO0}, V_{DDIO1}, V_{DDIO2}, V_{DDIO3}, V_{DDIO4}, V_{DDIO5}, V_{DDIO6}, V_{DDIO7}, V_{DDIO8}, V_{DDIO9}, V_{DDIO10})	-0.3	4.0	V
MV_{DD}-V_{SS} [*1]	DDR IO Power Supply Voltage	-0.3	1.975	V
V_{BAT}-V_{SS} [*1]	RTC Domain Power Supply Voltage	-0.3	4.0	V
ΔV_{DD}	Variations Between Different Power Pins	-	50	mV
$\|V_{DD} - AV_{DD}\|$	Allowed Voltage Difference For V_{DD} And AV_{DD}	-	50	mV
ΔV_{SS}	Variations Between Different Ground Pins	-	50	mV
$\|V_{SS} - AV_{SS}\|$	Allowed Voltage Difference For V_{SS} And AV_{SS}	-	50	mV

Note:

1. All main power (V_{DD_CPU}, V_{DD_CORE}, AV_{DD}, AV_{DD_ADC0}, AV_{DD_EADC0}, AV_{DDL_ROSC}, AV_{DDL_PLL0}, AV_{DDL_PLL1}, AV_{DDH_PLL1}, V_{DD_PLL1}, AV_{DDL_PLL2}, AV_{DDH_PLL2}, V_{DD_HSUSB0}, V_{DD_HSUSB1}, MV_{DD}, $MV_{DD\_DPHYPLL}$, V_{DD_OTP}, V_{BAT}, V_{DDIOX}) and ground (V_{SS}, AV_{SS}) pins must always be connected to the external power supply, in the permitted range.

Table 8.1-1 Voltage Characteristics

MA35D1 SERIES DATASHEET

8.1.2 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA})$

- T_A = ambient temperature (^{O}C)
- θ_{JA} = thermal resistance junction-ambient (^{O}C/Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_J	Junction Temperature (Absolute)	-40	-	125	^{o}C
T_{ST}	Storage Temperature	-65	-	150	
θ_{JA} [*1]	Thermal Resistance Junction-Ambient LQFP-EP 216-Pin (24x24 mm)	-	17.6	-	^{O}C/Watt
	Thermal Resistance Junction-Ambient LFBGA 312-Ball (15x15 mm)	-	21.7	-	^{O}C/Watt
	Thermal Resistance Junction-Ambient TFBGA 364-Ball (14x14 mm)	-	25.1	-	^{O}C/Watt

Note:

1. Determined according to JESD51 Integrated Circuits Thermal Test Method Environment Conditions,
   - FR4 PCB thickness is 1.6mm
   - Copper thickness is 2-OZ for Microstrip (Top/Bottom) layer
   - Copper thickness is 1-OZ for stripline (Inner) layer
   - LQFP216 follows JESD 51-7, 2S2P PCB is size 3" x 4.5"
   - BGA follows JESD 51-9, 2S2P PCB size is 4" x 4.5"

Table 8.1-2 Thermal Characteristics

8.1.3 EMC Characteristics

8.1.3.1 *Electrostatic discharge (ESD)*

For the Nuvoton MPU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

For the ESD test (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination.

8.1.3.2 *Static latch-up*

Two complementary static tests are required on **13** parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

Symbol	Description	Test Conditions	Maximum Value	Unit
V_{HBM}[*1]	Electrostatic Discharge, Human Body Mode	All GPIO except USB Port	±2	KV
		USB Ports	±4	KV
V_{CDM}[*2]	Electrostatic Discharge, Charge Device Model		500	V
LU[*3]	Static Latch-Up Class	T_A + 25 °C	100	mA

Note:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard

Table 8.1-3 EMC Characteristics

8.2 Operating Conditions

8.2.1 General Operating Conditions

(V_{BAT} = 3.0V, T_A = 25°C, f_{SYS_CLK1} = 180 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
f_{CA_CLK}	Cortex-A35 CPU clock frequency	-	-	800	MHz	V_{DD_CPU}=1.25V
f_{AXI_ACLK0}	Internal AXI0 clock frequency	-	-	1/2 f_{CA_CLK}	MHz	
f_{AXI_ACLK1} f_{AXI_ACLK2} f_{AXI_ACLK3} f_{AXI_ACLK4}	Internal AXI1, AXI2, AXI3 and AXI4 clock frequency	-	-	250	MHz	
f_{SYS_CLK1}	Internal system clock frequency	-	-	180	MHz	
f_{AHB_HCLK0} f_{AHB_HCLK1} f_{AHB_HCLK2}	Internal AHB0, AHB1 and AHB2 clock frequency	-	-	180	MHz	
f_{APB_PCLK0} f_{APB_PCLK1} f_{APB_PCLK2}	Internal APB0, APB1 and APB2 clock frequency	-	-	180	MHz	
f_{AHB_HCLK3} f_{APB_PCLK3} f_{APB_PCLK4}	Internal AHB3, APB3 and APB4 clock frequency	-	-	1/2 f_{SYS_CLK1}	MHz	
f_{MCK_P} f_{MCK_N}	External DDR SDRAM Positive and Negative Clock Output Frequency	-	-	533	MHz	
V_{DD_CPU}	Cortex-A35 CPU operation voltage	1.25	-	1.31	V	f_{CA_CLK} @ 800 MHz for BGA
V_{DD_CORE}	Internal digital circuit operation voltage	1.20		1.31	V	For BGA
		-	1.20	-		f_{CA_CLK} @ 800 MHz for LQFP216
AV_{DD}	Analog operation voltage for POR33, LVD, LVR and temperature snesor	3.0	-	3.6	V	
AV_{DD_ADC0}	Analog operation voltage for ADC0	3.0	-	3.6	V	
AV_{DD_EADC0}	Analog operation voltage for EADC0	3.0	-	3.6	V	
V_{REF_EADC0}	Analog reference voltage for EADC0	0	-	AV_{DD_EADC0}	V	Need to connect this pin with 0.1uF and 2.2uF capacitors
AV_{DDL_ROSC}	Low analog operation voltage for internal 12 MHz High Speed RC Oscillator (HIRC)	1.25		1.31	V	
AV_{DDL_PLL0}	Low analog operation voltage	1.25		1.31	V	CA-PLL and SYS-PLL

	for PLL group 0					
AV_{DDL_PLL1}	Low analog operaton voltage for PLL group 1	1.25		1.31	V	DDR-PLL
AV_{DDH_PLL1}	High analog operation voltage for PLL group 1	3.0	3.3	3.6	V	DDR-PLL
V_{DD_PLL1}	Digital operation voltage for PLL group 1	1.25	-	1.31	V	DDR-PLL
AV_{DDL_PLL2}	Low analog operaton voltage for PLL group 2	1.25		1.31	V	EPLL, APLL and VPLL
AV_{DDH_PLL2}	High analog operation voltage for PLL group 2	3.0	3.3	3.6	V	EPLL, APLL and VPLL
V_{DD_HSUSB0}	USB 2.0 Port 0 PHY operation voltage	3.3	3.3	3.6	V	
V_{DD_HSUSB1}	USB 2.0 Port 1 PHY operation voltage	3.3	3.3	3.6	V	
MV_{DD}	DDR PHY, DDR IO and DDR SDRAM operation voltage	1.7	1.8	1.9	V	LQFP with 128MB DDR2, such as P/N, MA35D16F787C
		1.29	1.35	1.45		BGA312 with 256MB DDR3L, LQFP216 with 512MB DDR3L, such as P/N, MA35D16A887C or MA35D16F987C
		1.29	-	1.9		BGA364, depended on external DDR DC spec., such as P/N, MA35D16A087C
$MV_{DD\_DPHYPLL}$	DDR PHY PLL operation voltage	2.25	2.5	2.75	V	
MV_{VREF_CA}	DDR SDRAM reference voltage for control, command and address pin	-	1/2 MV_{DD}	-	V	
MV_{VREF_DQ}	DDR SDRAM reference voltage for DQ data pin	-	1/2 MV_{DD}	-	V	
V_{DD_OTP}	OTP operation voltage	2.25	2.5	2.75	V	
V_{BAT}	RTC operation voltage by batteries	2.0	3.0	3.6	V	
V_{DDIO0}	IO group 0 operation voltage	3.0	-	3.6	V	
V_{DDIO1}	IO group 1 operation voltage	3.0	-	3.6	V	
V_{DDIO2}	IO group 2 operation voltage	1.65	-	3.6	V	
V_{DDIO3}	IO group 3 operation voltage	1.65	-	3.6	V	
V_{DDIO4}	IO group 4 operation voltage	1.65	-	3.6	V	
V_{DDIO5}	IO group 5 operation voltage	1.65	-	3.6	V	
V_{DDIO6}	IO group 6 operation voltage	3.0	-	3.6	V	
V_{DDIO7}	IO group 7 operation voltage	1.65	-	3.6	V	

V_{DDIO8}	IO group 8 operation voltage	1.65	-	3.6	V	
V_{DDIO9}	IO group 9 operation voltage	1.65	-	3.6	V	
V_{DDIO10}	IO group 10 operation voltage	3.0	-	3.6	V	
Note:						

Table 8.2-1 General Operating Conditions

8.2.2 Recommended Thermal Operation Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
T_J	Junction Temperature		-	105	^{o}C
PD	Allowable Power Dissipation	LQFP-EP 216-Pin (24x24 mm) at T_A = 85^{O}C	-	1.1	Watt
		LQFP-EP 216-Pin (24x24 mm) at T_A = 70^{O}C	-	1.9	Watt
		LFBGA 312-Ball (15x15 mm) at T_A = 70^{O}C	-	1.6	Watt
		TFBGA 364-Ball (14x14 mm) at T_A = 70^{O}C	-	1.3	Watt
Note:					

Table 8.2-2 Recommended Thermal Operation Conditions

8.3 DC Electrical Characteristics

8.3.1 Power Supply Scheme

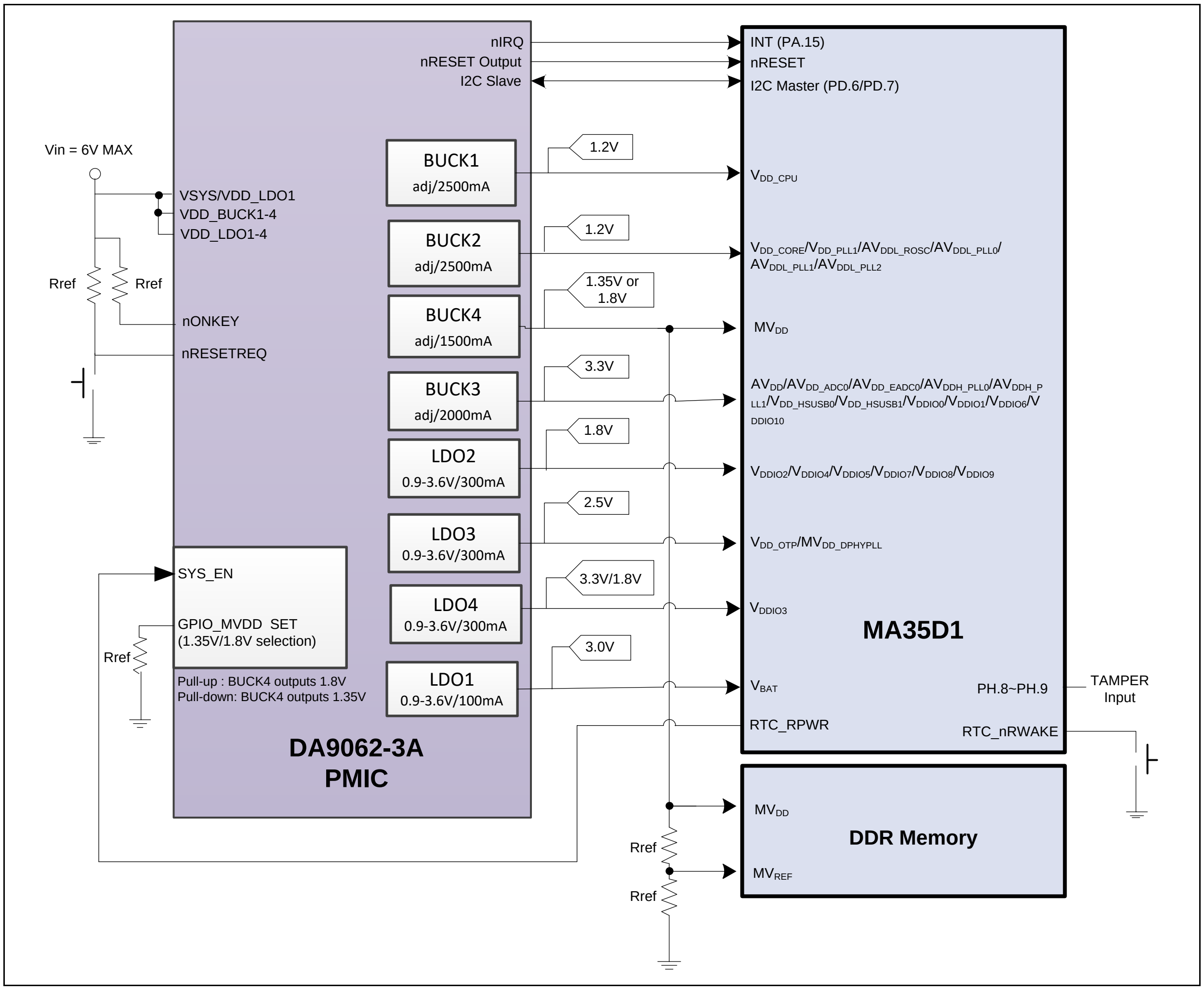


Figure 8-1 System Power Scheme Diagram

8.3.2 Power Mode Configurations

Mode	OFF/ RTC	Low Power Mode			Normal
Powered		DPD (Deep Power Down)	PD (Power Down)	IDLE	
CA35	X	X	PD	WFI	On
CA35x2	X	X	PD	WFI	On
SOC	X	PD	PD	On	On
DDR	X	Self-refresh	Self-refresh	On	On
M4	X	PD	On/PD	On/PD	On/PD
TSI	X	PD	PD	On/PD	On/PD
VBAT	On	On	On	On	On

Table 8.3-1 Power Mode Configurations

8.3.3 System Power Management Architecture

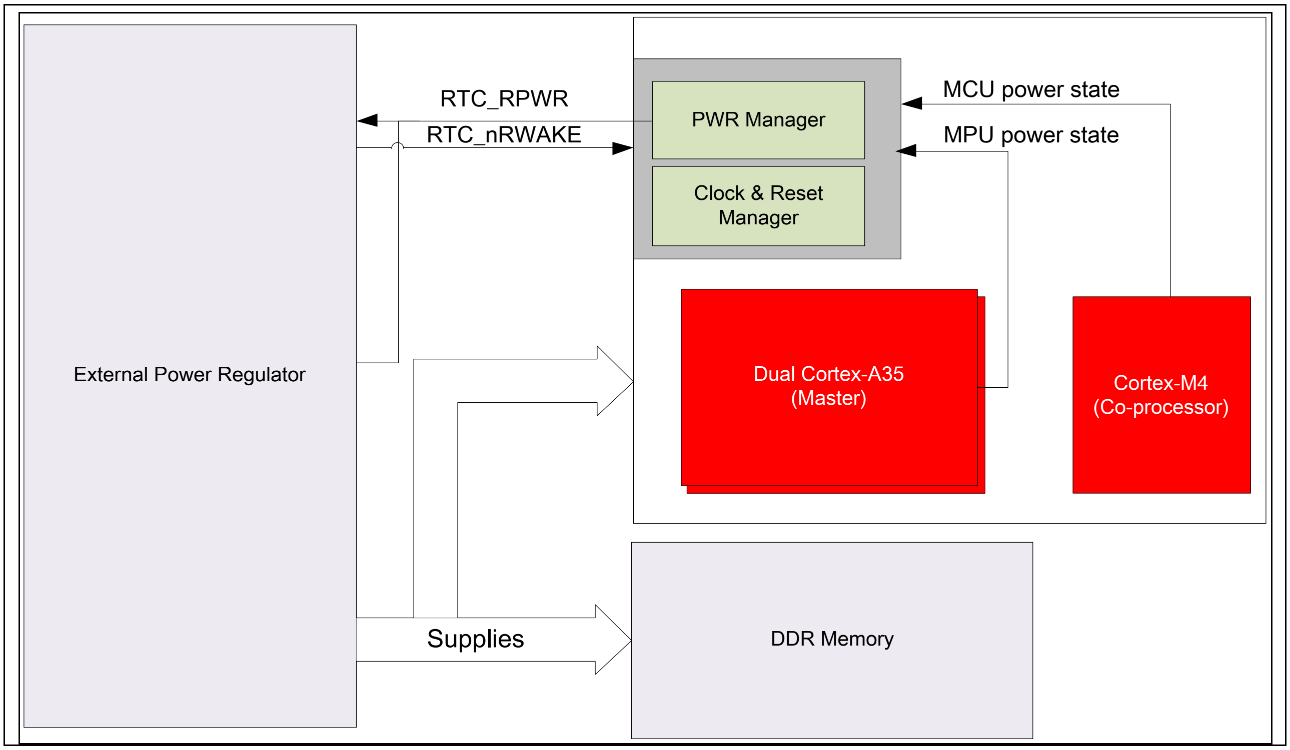


Figure 8-2 System Power Management Architecture

8.3.4 Supply Current Characteristics

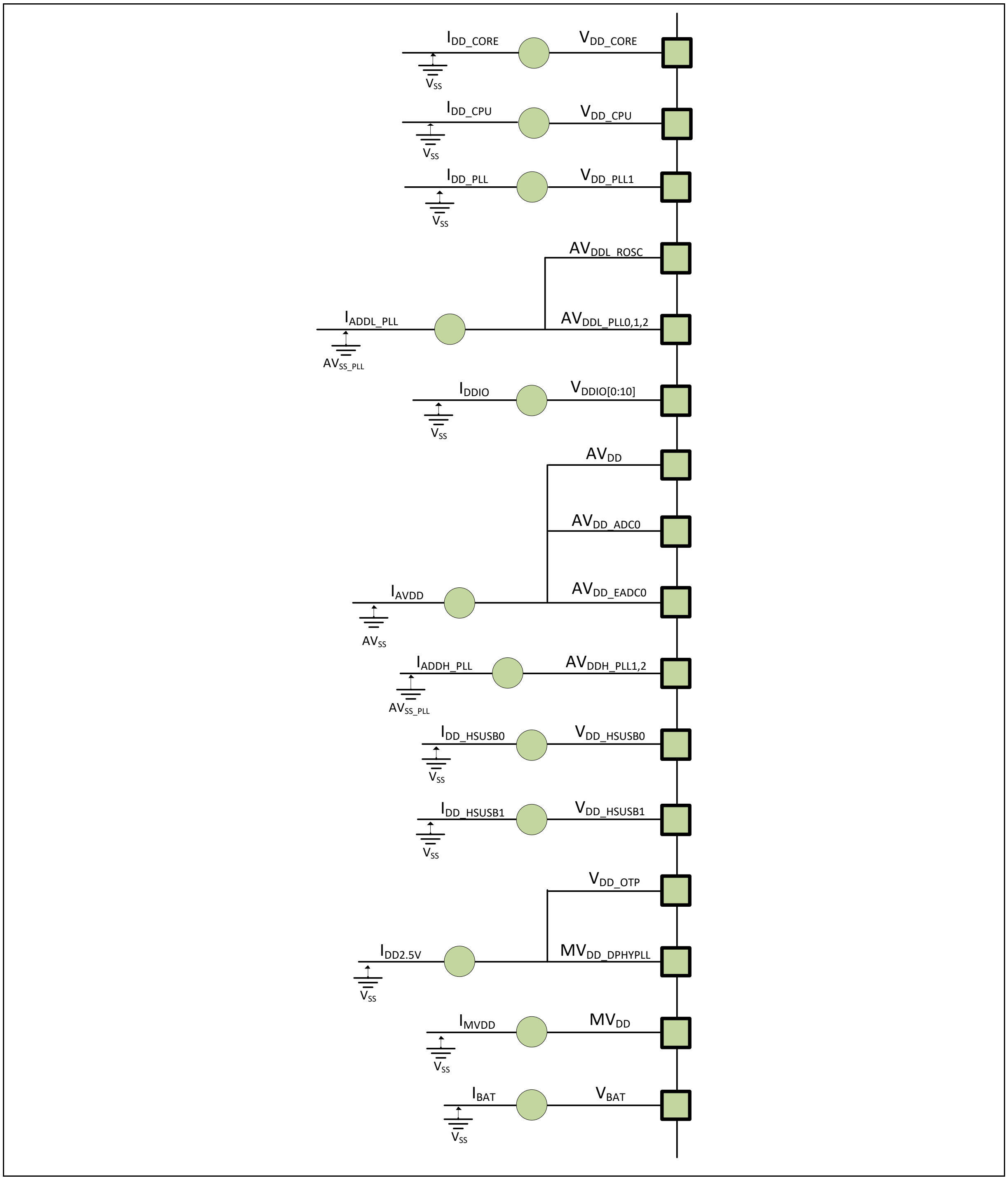


Figure 8-3 Current Measurement Scheme

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code. The current consumption measured as described in Figure 8-3 Current Measurement Scheme.

8.3.5 Typical Current Consumption

8.3.5.1 *MA35D16A887C Typical Current Consumption (BGA312 MCP with DDR3L/256MB)*

Parameter	Symbol	Specification				Test Conditions
		TA = -40°C (Max)	TA = 25°C (Typ)	TA = 85°C (Max)	Unit	
Current Consumption of Normal Operating Mode-2 T_A = 25°C, FOSC = 24 MHz Frequency of CPUCLK/DDR_CLK is 800/533 MHz. All IPs on HCLK = 180 MHz MCLK = 533 MHz M4 CLK = 180 MHz TSI CLK = 180 MHz Core_1 @WFE(); M4 @while(1);	Group1 (I_{VDD_CORE}, I_{VDD_PLL1}, $I_{AVDDL\_PLL[2:0]}$, I_{AVDDL_ROSC})	172.1	178.0	329.9	mA	1.2V
	Group2 (I_{VDD_CPU})	92.3	107.8	405.7	mA	1.25V
	Group3 ($I_{VDDIO[10:0]}$)	1.8	1.6	1.7	mA	3.3V
	Group4 (I_{VDD_OTP}, $I_{MVDD\_DPHYPLL}$)	27.4	25.3	26.8	mA	2.5V
	Group5 ($I_{AVDDH\_PLL[2:1]}$)	636.1	592.2	623.8	uA	3.3V
	Group6 (I_{AVDD}, I_{AVDD_ADC0}, I_{AVDD_EADC0}, $I_{VDD\_HSUSB[1:0]}$)	326.2	307.6	370.7	uA	3.3V
	Group7 (I_{MVDD})	22.1	18.6	45.7	mA	1.35V
	Group8 (I_{VBAT})	35.5	29.8	27.0	uA	3.0V
Current Consumption of Idle Mode-2 T_A = 25°C, FOSC = 24 MHz Frequency of CPUCLK/DDR_CLK is 800/533 MHz. All IPs on HCLK = 180 MHz MCLK = 533 MHz M4 CLK = 180 MHz TSI CLK = 180 MHz Core_1 @WFE(); M4 @PWD	Group1 (I_{VDD_CORE}, I_{VDD_PLL1}, $I_{AVDDL\_PLL[2:0]}$, I_{AVDDL_ROSC})	161.7	167.5	315.4	mA	1.2V
	Group2 (I_{VDD_CPU})	11.2	25.8	315.9	mA	1.25V
	Group3 ($I_{VDDIO[10:0]}$)	1.8	1.6	1.7	mA	3.3V
	Group4 (I_{VDD_OTP}, $I_{MVDD\_DPHYPLL}$)	27.4	25.4	26.8	mA	2.5V
	Group5 ($I_{AVDDH\_PLL[2:1]}$)	636.2	592.3	623.9	uA	3.3V

	Group6 (I_{AVDD}, I_{AVDD_ADC0}, I_{AVDD_EADC0}, $I_{VDD\_HSUSB[1:0]}$)	329.1	307.8	366.4	uA	3.3V
	Group7 (I_{MVDD})	22.1	18.6	46.3	mA	1.35V
	Group8 (I_{VBAT})	35.5	29.8	26.9	uA	3.0V
Current Consumption of NPD Mode T_A = 25°C, FOSC = 24 MHz Frequency of CPUCLK/DDR_CLK is 800/533 MHz. All IPs off, all GPIO are input with pull-up. HCLK = STOP MCLK = STOP and DRAM enter Slef-Refresh M4 CLK = STOP TSI CLK = STOP Core_1 @WFE(); M4 @PWD	Group1 (I_{VDD_CORE}, I_{VDD_PLL1}, $I_{AVDDL\_PLL[2:0]}$, I_{AVDDL_ROSC})	1.5	6.4	138.8	mA	1.2V
	Group2 (I_{VDD_CPU})	3.7	16.7	285.1	mA	1.25V
	Group3 ($I_{VDDIO[10:0]}$)	220.8	231.2	335.1	uA	3.3V
	Group4 (I_{VDD_OTP}, $I_{MVDD\_DPHYPLL}$)	9.3	10.6	124.8	uA	2.5V
	Group5 ($I_{AVDDH\_PLL[2:1]}$)	0.0	42.1	4025.8	nA	3.3V
	Group6 (I_{AVDD}, I_{AVDD_ADC0}, I_{AVDD_EADC0}, $I_{VDD\_HSUSB[1:0]}$)	167.0	154.5	215.3	uA	3.3V
	Group7 (I_{MVDD})	7.1	6.7	28.4	mA	1.35V
	Group8 (I_{VBAT})	35.5	29.8	26.8	uA	3.0V
Current Consumption of DPD Mode T_A = 25°C, FOSC = 24 MHz Frequency of CPUCLK/DDR_CLK is 800/533 MHz. All IPs off, all GPIO are input with pull-up. HCLK = STOP MCLK = STOP and DRAM enter Slef-Refresh M4 CLK = STOP TSI CLK = STOP Core_1 @WFE();	Group1 (I_{VDD_CORE}, I_{VDD_PLL1}, $I_{AVDDL\_PLL[2:0]}$, I_{AVDDL_ROSC})	758.9	6.1	117.8	mA	1.2V
	Group2 (I_{VDD_CPU})	31.9	207.4	634.3	uA	1.25V
	Group3 ($I_{VDDIO[10:0]}$)	220.8	230.6	318.0	uA	3.3V
	Group4 (I_{VDD_OTP}, $I_{MVDD\_DPHYPLL}$)	9.3	51833.3	106.8	uA	2.5V

M4 @PWD	Group5 ($I_{AVDDH\_PLL[2:1]}$)	0.0	39.1	3347.0	nA	3.3V
	Group6 (I_{AVDD}, I_{AVDD_ADC0}, I_{AVDD_EADC0}, $I_{VDD\_HSUSB[1:0]}$)	168.2	154.4	202.3	uA	3.3V
	Group7 (I_{MVDD})	7.1	6.6	26.1	mA	1.35V
	Group8 (I_{VBAT})	35.5	29.8	26.7	uA	3.0V

8.3.5.2 *MA35D16F987C Typical Current Consumption (LQFP216 MCP with DDR3L/512MB)*

Parameter	Symbol	Specification				Test Conditions
		TA = -40°C (Typ)	TA = 25°C (Typ)	TA = 85°C (Typ)	Unit	
Current Consumption of Normal Operating Mode-1 T_A = 25°C, FOSC = 24 MHz Frequency of CPUCLK/DDR_CLK is 800/533 MHz. All IPs on HCLK = 180 MHz MCLK = 533 MHz M4 CLK = 180 MHz TSI CLK = 180 MHz Core_1 @WFE(); M4 @while(1);	Group1 (I_{VDD_CORE}, I_{VDD_PLL1}, $I_{AVDDL\_PLL[2:0]}$, I_{AVDDL_ROSC})	248.5	276.4	407.6	mA	1.25V
	Group3 ($I_{VDDIO[10:0]}$)	2.4	2.3	2.3	mA	3.3V
	Group4 (I_{VDD_OTP}, $I_{MVDD\_DPHYPLL}$)	24.9	25.1	25.1	mA	2.5V
	Group5 ($I_{AVDDH\_PLL[2:1]}$)	0.0	24.2	541.7	nA	3.3V
	Group6 (I_{AVDD}, I_{AVDD_ADC0}, I_{AVDD_EADC0}, $I_{VDD\_HSUSB[1:0]}$)	178.8	181.6	194.3	uA	3.3V
	Group7 (I_{MVDD})	15.9	18.2	37.6	mA	1.35V
	Group8 (I_{VBAT})	33.9	29.5	26.2	uA	3.0V
Current Consumption of Idle Mode-1 T_A = 25°C, FOSC = 24 MHz Frequency of CPUCLK/DDR_CLK is 800/533 MHz. All IPs on HCLK = 180 MHz MCLK = 533 MHz M4 CLK = 180 MHz TSI CLK = 180 MHz Core_1 @WFE(); M4 @PWD	Group1 (I_{VDD_CORE}, I_{VDD_PLL1}, $I_{AVDDL\_PLL[2:0]}$, I_{AVDDL_ROSC})	165.3	189.6	330.6	mA	1.25V
	Group3 ($I_{VDDIO[10:0]}$)	2.5	2.4	2.3	mA	3.3V
	Group4 (I_{VDD_OTP}, $I_{MVDD\_DPHYPLL}$)	25.2	25.2	25.2	mA	2.5V
	Group5 ($I_{AVDDH\_PLL[2:1]}$)	0.0	23.6	595.1	nA	3.3V
	Group6 (I_{AVDD}, I_{AVDD_ADC0}, I_{AVDD_EADC0}, $I_{VDD\_HSUSB[1:0]}$)	178.9	181.5	195.2	uA	3.3V
	Group7 (I_{MVDD})	16.2	18.2	40.9	mA	1.35V

	Group8 (I_{VBAT})	34.1	29.5	26.3	uA	3.0V
Current Consumption of NPD Mode T_A = 25°C, FOSC = 24 MHz Frequency of CPUCLK/DDR_CLK is 800/533 MHz. All IPs off, all GPIO are input with pull-up. HCLK = STOP MCLK = STOP and DRAM enter Slef-Refresh M4 CLK = STOP TSI CLK = STOP Core_1 @WFE(); M4 @PWD	Group1 (I_{VDD_CORE}, I_{VDD_PLL1}, $I_{AVDDL\_PLL[2:0]}$, I_{AVDDL_ROSC})	1.8	20.5	151.9	mA	1.25V
	Group3 ($I_{VDDIO[10:0]}$)	230.9	249.1	293.8	uA	3.3V
	Group4 (I_{VDD_OTP}, $I_{MVDD\_DPHYPLL}$)	8.9	10.1	30.4	uA	2.5V
	Group5 ($I_{AVDDH\_PLL[2:1]}$)	0.0	17.7	499.3	nA	3.3V
	Group6 (I_{AVDD}, I_{AVDD_ADC0}, I_{AVDD_EADC0}, $I_{VDD\_HSUSB[1:0]}$)	150.4	152.7	165.0	uA	3.3V
	Group7 (I_{MVDD})	4.8	5.9	25.0	mA	1.35V
	Group8 (I_{VBAT})	34.5	29.5	26.2	uA	3.0V
Current Consumption of DPD Mode T_A = 25°C, FOSC = 24 MHz Frequency of CPUCLK/DDR_CLK is 800/533 MHz. All IPs off, all GPIO are input with pull-up. HCLK = STOP MCLK = STOP and DRAM enter Slef-Refresh M4 CLK = STOP TSI CLK = STOP Core_1 @WFE(); M4 @PWD	Group1 (I_{VDD_CORE}, I_{VDD_PLL1}, $I_{AVDDL\_PLL[2:0]}$, I_{AVDDL_ROSC})	0.8	5.7	45.9	mA	1.25V
	Group3 ($I_{VDDIO[10:0]}$)	230.6	248.4	291.0	uA	3.3V
	Group4 (I_{VDD_OTP}, $I_{MVDD\_DPHYPLL}$)	8.9	10.0	28.3	uA	2.5V
	Group5 ($I_{AVDDH\_PLL[2:1]}$)	0.0	15.9	482.3	nA	3.3V
	Group6 (I_{AVDD}, I_{AVDD_ADC0}, I_{AVDD_EADC0}, $I_{VDD\_HSUSB[1:0]}$)	150.5	152.7	163.7	uA	3.3V
	Group7 (I_{MVDD})	4.8	5.9	18.8	mA	1.35V
	Group8 (I_{VBAT})	34.5	29.5	26.2	uA	3.0V

Current Consumption of Coremark Mode All IP be turn ON and CA35x2 and M4 run CoreMark CPU @800 MHz DDR @533 MHz HCLK= M4_CLK = 180 MHz TSI_CLK = 180 MHz	Group1 (I_{VDD_CORE}, I_{VDD_PLL1}, $I_{AVDDL\_PLL[2:0]}$, I_{AVDDL_ROSC})	382.6	421.4	590.0	mA	1.25V
	Group3 ($I_{VDDIO[10:0]}$)	2.6	2.5	2.4	mA	3.3V
	Group4 (I_{VDD_OTP}, $I_{MVDD\_DPHYPLL}$)	24.1	24.6	24.9	mA	2.5V
	Group5 ($I_{AVDDH\_PLL[2:1]}$)	526.1	517.1	510.1	uA	3.3V
	Group6 (I_{AVDD}, I_{AVDD_ADC0}, I_{AVDD_EADC0}, $I_{VDD\_HSUSB[1:0]}$)	171.8	175.9	193.3	uA	3.3V
	Group7 (I_{MVDD})	14.9	18.0	41.8	mA	1.35V
	Group8 (I_{VBAT})	33.2	29.3	26.4	uA	3.0V

8.3.5.3 *MA35D16F787C Typical Current Consumption (LQFP216 MCP with DDR2/128MB)*

Parameter	Symbol	Specification				Test Conditions
		TA = -40°C (Typ)	TA = 25°C (Typ)	TA = 85°C (Typ)	Unit	
Current Consumption of Normal Operating Mode-1 T_A = 25°C, FOSC = 24 MHz Frequency of CPUCLK/DDR_CLK is 800/533 MHz. All IPs on HCLK = 180 MHz MCLK = 533 MHz M4 CLK = 180 MHz TSI CLK = 180 MHz Core_1 @WFE(); M4 @while(1);	Group1 (I_{VDD_CORE}, I_{VDD_PLL1}, $I_{AVDDL\_PLL[2:0]}$, I_{AVDDL_ROSC})	254.8	306.2	594.5	mA	1.25V
	Group3 ($I_{VDDIO[10:0]}$)	2.5	2.5	2.3	mA	3.3V
	Group4 (I_{VDD_OTP}, $I_{MVDD\_DPHYPLL}$)	26.6	25.8	26.2	mA	2.5V
	Group5 ($I_{AVDDH\_PLL[2:1]}$)	0.0	28.0	674.1	nA	3.3V
	Group6 (I_{AVDD}, I_{AVDD_ADC0}, I_{AVDD_EADC0}, $I_{VDD\_HSUSB[1:0]}$)	179.1	180.2	197.3	uA	3.3V
	Group7 (I_{MVDD})	48.7	47.2	55.5	mA	1.8V
	Group8 (I_{VBAT})	34.8	29.3	26.6	uA	3.0V
Current Consumption of Idle Mode-1 T_A = 25°C, FOSC = 24 MHz Frequency of CPUCLK/DDR_CLK is 800/533 MHz. All IPs on HCLK = 180 MHz MCLK = 533 MHz M4 CLK = 180 MHz TSI CLK = 180 MHz Core_1 @WFE(); M4 @PWD	Group1 (I_{VDD_CORE}, I_{VDD_PLL1}, $I_{AVDDL\_PLL[2:0]}$, I_{AVDDL_ROSC})	169.7	229.0	545.7	mA	1.25V
	Group3 ($I_{VDDIO[10:0]}$)	2.5	2.5	2.3	mA	3.3V
	Group4 (I_{VDD_OTP}, $I_{MVDD\_DPHYPLL}$)	26.7	26.0	26.3	mA	2.5V
	Group5 ($I_{AVDDH\_PLL[2:1]}$)	0.0	31.9	786.9	nA	3.3V
	Group6 (I_{AVDD}, I_{AVDD_ADC0}, I_{AVDD_EADC0}, $I_{VDD\_HSUSB[1:0]}$)	179.0	180.7	199.6	uA	3.3V
	Group7 (I_{MVDD})	48.2	47.3	55.9	mA	1.8V

	Group8 (I_{VBAT})	34.8	29.4	26.6	uA	3.0V
Current Consumption of NPD Mode T_A = 25°C, FOSC = 24 MHz Frequency of CPUCLK/DDR_CLK is 800/533 MHz. All IPs off, all GPIO are input with pull-up. HCLK = STOP MCLK = STOP and DRAM enter Slef-Refresh M4 CLK = STOP TSI CLK = STOP Core_1 @WFE(); M4 @PWD	Group1 (I_{VDD_CORE}, I_{VDD_PLL1}, $I_{AVDDL\_PLL[2:0]}$, I_{AVDDL_ROSC})	6.0	63.2	365.6	mA	1.25V
	Group3 ($I_{VDDIO[10:0]}$)	221.0	269.1	296.3	uA	3.3V
	Group4 (I_{VDD_OTP}, $I_{MVDD\_DPHYPLL}$)	9.3	10.9	38.9	uA	2.5V
	Group5 ($I_{AVDDH\_PLL[2:1]}$)	0.0	24.8	678.7	nA	3.3V
	Group6 (I_{AVDD}, I_{AVDD_ADC0}, I_{AVDD_EADC0}, $I_{VDD\_HSUSB[1:0]}$)	151.0	153.2	169.5	uA	3.3V
	Group7 (I_{MVDD})	10.4	12.4	20.3	mA	1.8V
	Group8 (I_{VBAT})	34.9	29.6	26.5	uA	3.0V
Current Consumption of DPD Mode T_A = 25°C, FOSC = 24 MHz Frequency of CPUCLK/DDR_CLK is 800/533 MHz. All IPs off, all GPIO are input with pull-up. HCLK = STOP MCLK = STOP and DRAM enter Slef-Refresh M4 CLK = STOP TSI CLK = STOP Core_1 @WFE(); M4 @PWD	Group1 (I_{VDD_CORE}, I_{VDD_PLL1}, $I_{AVDDL\_PLL[2:0]}$, I_{AVDDL_ROSC})	1.7	16.3	105.3	mA	1.25V
	Group3 ($I_{VDDIO[10:0]}$)	220.8	269.3	290.6	uA	3.3V
	Group4 (I_{VDD_OTP}, $I_{MVDD\_DPHYPLL}$)	9.2	10.8	34.4	uA	2.5V
	Group5 ($I_{AVDDH\_PLL[2:1]}$)	0.0	22.0	573.5	nA	3.3V
	Group6 (I_{AVDD}, I_{AVDD_ADC0}, I_{AVDD_EADC0}, $I_{VDD\_HSUSB[1:0]}$)	151.1	153.1	166.8	uA	3.3V
	Group7 (I_{MVDD})	10.3	12.2	19.1	mA	1.8V
	Group8 (I_{VBAT})	34.9	29.7	26.4	uA	3.0V

Current Consumption of Coremark Mode All IP be turn ON and CA35x2 and M4 run CoreMark CPU @800 MHz DDR @533 MHz HCLK = M4_CLK = 180 MHz TSI_CLK = 180 MHz	Group1 (I_{VDD_CORE}, I_{VDD_PLL1}, $I_{AVDDL\_PLL[2:0]}$, I_{AVDDL_ROSC})	396.6	476.8	824.4	mA	1.25V
	Group3 ($I_{VDDIO[10:0]}$)	2.6	2.6	2.4	mA	3.3V
	Group4 (I_{VDD_OTP}, $I_{MVDD\_DPHYPLL}$)	26.4	26.3	26.1	mA	2.5V
	Group5 ($I_{AVDDH\_PLL[2:1]}$)	513.8	504.0	496.9	uA	3.3V
	Group6 (I_{AVDD}, I_{AVDD_ADC0}, I_{AVDD_EADC0}, $I_{VDD\_HSUSB[1:0]}$)	173.1	176.2	199.6	uA	3.3V
	Group7 (I_{MVDD})	48.3	48.7	57.8	mA	1.8V
	Group8 (I_{VBAT})	34.5	29.7	26.8	uA	3.0V

8.3.6 I/O DC Characteristics

8.3.6.1 *General Purpose I/O Type A (GPIO Type A) DC Characteristics*

DC Characteristics for 3.3V I/O Application

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
V_{DDIO}	I/O Supply Voltage	3.0	3.3	3.6	V	
V_{IH}	Input High Voltage	2.0	-	V_{DDIO}+0.3	V	TTL Input
V_{IL}	Input Low Voltage	-0.3	-	0.8	V	TTL Input
V_{OH}	Output High Voltage	2.4	-	-	V	TTL Output
V_{OL}	Output Low Voltage	-	-	0.4	V	TTL Output
I_{OH}	Source Current in Push-Pull Mode (T_A = 25^{O}C, V_{OH}=2.4V)	-	9.6	-	mA	DS (Driving Strength) = 000
		-	14.4	-	mA	DS (Driving Strength) = 001
		-	19.1	-	mA	DS (Driving Strength) = 010
		-	23.9	-	mA	DS (Driving Strength) = 011
		-	28.7	-	mA	DS (Driving Strength) = 100
		-	33.5	-	mA	DS (Driving Strength) = 101
		-	38.2	-	mA	DS (Driving Strength) = 110
		-	43.0	-	mA	DS (Driving Strength) = 111
I_{OL}	Sink Current in Push-Pull Mode (T_A = 25^{O}C, V_{OL}=0.4V)	-	5.3	-	mA	DS (Driving Strength) = 000
		-	8.0	-	mA	DS (Driving Strength) = 001
		-	10.8	-	mA	DS (Driving Strength) = 010
		-	13.3	-	mA	DS (Driving Strength) = 011
		-	16.1	-	mA	DS (Driving Strength) = 100
		-	18.7	-	mA	DS (Driving Strength) = 101
		-	21.5	-	mA	DS (Driving Strength) = 110
		-	24.1	-	mA	DS (Driving Strength) = 111
I_L	Input Leakage Current	-	±1	-	uA	

V_T	Threshold Point	-	0.41	-	V	
V_{T+}	Schmitt Trig Low to High Threshold Point	-	1.73	-	V	
V_{T-}	Schmitt Trig. High to Low Threshold Point	-	1.32	-	V	
R_{PU}	Pull-up Resistor	27	40	65	KΩ	
R_{PD}	Pull-down Resistor	30	47	83	KΩ	

DC Characteristics for 1.8V I/O Application

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
V_{DDIO}	I/O Supply Voltage	1.62	1.8	1.98	V	
V_{IH}	Input High Voltage	0.65* V_{DDIO}	-	V_{DDIO}+0.3	V	TTL Input
V_{IL}	Input Low Voltage	-0.3	-	0.35* V_{DDIO}	V	TTL Input
V_{OH}	Output High Voltage	V_{DDIO}-0.45	-	-	V	TTL Output
V_{OL}	Output Low Voltage	-	-	0.45	V	TTL Output
I_{OH}	Source Current in Push-Pull Mode (T_A = 25°C, V_{OH}=V_{DDIO}-0.45V)	-	2.9	-	mA	DS (Driving Strength) = 000
		-	4.4	-	mA	DS (Driving Strength) = 001
		-	5.8	-	mA	DS (Driving Strength) = 010
		-	7.3	-	mA	DS (Driving Strength) = 011
		-	8.6	-	mA	DS (Driving Strength) = 100
		-	10.1	-	mA	DS (Driving Strength) = 101
		-	11.5	-	mA	DS (Driving Strength) = 110
		-	13.0	-	mA	DS (Driving Strength) = 111
I_{OL}	Sink Current in Push-Pull Mode (T_A = 25°C, V_{OL}=0.45V)	-	3.5	-	mA	DS (Driving Strength) = 000
		-	5.1	-	mA	DS (Driving Strength) = 001
		-	7.0	-	mA	DS (Driving Strength) = 010
		-	8.6	-	mA	DS (Driving Strength) = 011
		-	10.5	-	mA	DS (Driving Strength) =

						100
		-	12.1	-	mA	DS (Driving Strength) = 101
		-	14.0	-	mA	DS (Driving Strength) = 110
		-	15.6	-	mA	DS (Driving Strength) = 111
I_L	Input Leakage Current		±10		uA	
V_T	Threshold Point		0.34		V	
V_{T+}	Schmitt Trig Low to High Threshold Point	-	1.05	-	V	
V_{T-}	Schmitt Trig. High to Low Threshold Point	-	0.71	-	V	
R_{PU}	Pull-up Resistor	53	90	197	KΩ	
R_{PD}	Pull-down Resistor	54	99	202	KΩ	

8.3.6.2 *General Purpose I/O Type B (GPIO Type B) DC Characteristics*

DC Characteristics for 3.3V I/O Application

Symbol	Description	Min.	Typ	Max	Unit	Test Conditions
V_{DDIO}	I/O Supply Voltage	2.7	3.3	3.63	V	
V_{IH}	Input High Voltage	0.625* V_{DDIO}	-	V_{DDIO}+0.3	V	TTL Input
V_{IL}	Input Low Voltage	-0.3	-	0.25* V_{DDIO}	V	TTL Input
V_{OH}	Output High Voltage	0.75* V_{DDIO}	-	-	V	TTL Output
V_{OL}	Output Low Voltage	-	-	0.125* V_{DDIO}	V	TTL Output
I_{OH}	Source Current in Push-Pull Mode (T_A = 25^{O}C, V_{OH}=0.75* V_{DDIO})	-	17.1	-	mA	DS (Driving Strength) = 000
		-	25.6	-	mA	DS (Driving Strength) = 001
		-	34.1	-	mA	DS (Driving Strength) = 010
		-	42.8	-	mA	DS (Driving Strength) = 011
		-	48.0	-	mA	DS (Driving Strength) = 100
		-	56.0	-	mA	DS (Driving Strength) = 101
		-	77.0	-	mA	DS (Driving Strength) = 110
		-	82.0	-	mA	DS (Driving Strength) = 111
I_{OL}	Sink Current in Push-Pull Mode (T_A = 25^{O}C, V_{OL}=0.125* V_{DDIO})	-	10.0	-	mA	DS (Driving Strength) = 000
		-	14.2	-	mA	DS (Driving Strength) = 001
		-	18.0	-	mA	DS (Driving Strength) = 010
		-	22.0	-	mA	DS (Driving Strength) = 011
		-	26.0	-	mA	DS (Driving Strength) = 100
		-	29.0	-	mA	DS (Driving Strength) = 101
		-	39.0	-	mA	DS (Driving Strength) = 110
		-	42.0	-	mA	DS (Driving Strength) = 111

I_L	Input Leakage Current	-	±1	-	uA	
V_T	Threshold Point	-	0.37	-	V	
V_{T+}	Schmitt Trig Low to High Threshold Point	-	1.65	-	V	
V_{T-}	Schmitt Trig. High to Low Threshold Point	-	1.28	-	V	
R_{PU}	Pull-up Resistor	43	50	60	KΩ	
R_{PD}	Pull-down Resistor	43	50	60	KΩ	

DC Characteristics for 1.8V I/O Application

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
V_{DDIO}	I/O Supply Voltage	1.65	1.8	1.95	V	
V_{IH}	Input High Voltage	0.65* V_{DDIO}	-	V_{DDIO}+0.3	V	TTL Input
V_{IL}	Input Low Voltage	-0.3	-	0.35* V_{DDIO}	V	TTL Input
V_{OH}	Output High Voltage	V_{DDIO}-0.45	-	-	V	TTL Output
V_{OL}	Output Low Voltage	-	-	0.45	V	TTL Output
I_{OH}	Source Current in Push-Pull Mode (T_A = 25°C, V_{OH}=V_{DDIO}-0.45V)	-	5.7	-	mA	DS (Driving Strength) = 000
		-	8.5	-	mA	DS (Driving Strength) = 001
		-	11.4	-	mA	DS (Driving Strength) = 010
		-	13.0	-	mA	DS (Driving Strength) = 011
		-	16.0	-	mA	DS (Driving Strength) = 100
		-	18.0	-	mA	DS (Driving Strength) = 101
		-	25.0	-	mA	DS (Driving Strength) = 110
		-	28.0	-	mA	DS (Driving Strength) = 111
I_{OL}	Sink Current in Push-Pull Mode (T_A = 25°C, V_{OL}=0.45V)	-	6.8	-	mA	DS (Driving Strength) = 000
		-	10.1	-	mA	DS (Driving Strength) = 001
		-	13.6	-	mA	DS (Driving Strength) = 010
		-	16.9	-	mA	DS (Driving Strength) = 011

		-	19.0	-	mA	DS (Driving Strength) = 100
		-	21.9	-	mA	DS (Driving Strength) = 101
		-	29.0	-	mA	DS (Driving Strength) = 110
		-	32.0	-	mA	DS (Driving Strength) = 111
I_L	Input Leakage Current		±1		uA	
V_T	Threshold Point		0.34		V	
V_{T+}	Schmitt Trig Low to High Threshold Point	-	1.04	-	V	
V_{T-}	Schmitt Trig. High to Low Threshold Point	-	0.70	-	V	
R_{PU}	Pull-up Resistor	43	50	60	KΩ	
R_{PD}	Pull-down Resistor	43	50	60	KΩ	

8.3.6.3 General Purpose I/O Type C (GPIO Type C) DC Characteristics

DC Characteristics for 3.3V I/O Application

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
V_{DDIO}	I/O Supply Voltage	3.0	3.3	3.6	V	
V_{IH}	Input High Voltage	2.0	-	V_{DDIO}+0.3	V	TTL Input
V_{IL}	Input Low Voltage	-0.3	-	0.8	V	TTL Input
V_{OH}	Output High Voltage	2.4	-	-	V	TTL Output
V_{OL}	Output Low Voltage	-	-	0.4	V	TTL Output
I_{OH}	Source Current in Push-Pull Mode (T_A = 25°C, V_{OH}=2.4V)	-	5.4	-	mA	DS (Driving Strength) = 000
		-	10.6	-	mA	DS (Driving Strength) = 001
		-	15.8	-	mA	DS (Driving Strength) = 010
		-	20.7	-	mA	DS (Driving Strength) = 011
		-	25.8	-	mA	DS (Driving Strength) = 100
		-	30.7	-	mA	DS (Driving Strength) = 101
		-	35.2	-	mA	DS (Driving Strength) = 110
		-	39.4	-	mA	DS (Driving Strength) = 111
I_{OL}	Sink Current in Push-Pull Mode (T_A = 25°C, V_{OL}=0.4V)	-	3.8	-	mA	DS (Driving Strength) = 000
		-	7.5	-	mA	DS (Driving Strength) = 001
		-	11.1	-	mA	DS (Driving Strength) = 010
		-	14.6	-	mA	DS (Driving Strength) = 011
		-	18	-	mA	DS (Driving Strength) = 100
		-	21.3	-	mA	DS (Driving Strength) = 101
		-	24.6	-	mA	DS (Driving Strength) = 110
		-	27.7	-	mA	DS (Driving Strength) = 111
I_L	Input Leakage Current	-	±1	-	uA	
V_T	Threshold Point	-	0.66	-	V	

V_{T+}	Schmitt Trig Low to High Threshold Point	-	1.8	-	V	
V_{T-}	Schmitt Trig. High to Low Threshold Point	-	1.14	-	V	
R_{PU}	Pull-up Resistor	35	55	90	KΩ	
R_{PD}	Pull-down Resistor	34	56	93	KΩ	

DC Characteristics for 1.8V I/O Application

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
V_{DDIO}	I/O Supply Voltage	1.62	1.8	1.98	V	
V_{IH}	Input High Voltage	0.65* V_{DDIO}	-	V_{DDIO}+0.3	V	TTL Input
V_{IL}	Input Low Voltage	-0.3	-	0.35* V_{DDIO}	V	TTL Input
V_{OH}	Output High Voltage	V_{DDIO}-0.45	-	-	V	TTL Output
V_{OL}	Output Low Voltage	-	-	0.45	V	TTL Output
I_{OH}	Source Current in Push-Pull Mode (T_A = 25°C, V_{OH}=V_{DDIO}-0.45V)	-	1.6	-	mA	DS (Driving Strength) = 000
		-	3.2	-	mA	DS (Driving Strength) = 001
		-	4.7	-	mA	DS (Driving Strength) = 010
		-	6.3	-	mA	DS (Driving Strength) = 011
		-	7.6	-	mA	DS (Driving Strength) = 100
		-	9.4	-	mA	DS (Driving Strength) = 101
		-	10.8	-	mA	DS (Driving Strength) = 110
		-	12.3	-	mA	DS (Driving Strength) = 111
I_{OL}	Sink Current in Push-Pull Mode (T_A = 25°C, V_{OL}=0.45V)	-	2.3	-	mA	DS (Driving Strength) = 000
		-	4.7	-	mA	DS (Driving Strength) = 001
		-	7.0	-	mA	DS (Driving Strength) = 010
		-	9.2	-	mA	DS (Driving Strength) = 011
		-	11.4	-	mA	DS (Driving Strength) = 100

		-	13.7	-	mA	DS (Driving Strength) = 101
		-	15.8	-	mA	DS (Driving Strength) = 110
		-	18	-	mA	DS (Driving Strength) = 111
I_L	Input Leakage Current		±10		uA	
V_T	Threshold Point		0.44		V	
V_{T+}	Schmitt Trig Low to High Threshold Point	-	1.03	-	V	
V_{T-}	Schmitt Trig. High to Low Threshold Point	-	0.59	-	V	
R_{PU}	Pull-up Resistor	66	120	228	KΩ	
R_{PD}	Pull-down Resistor	59	122	225	KΩ	

8.3.6.4 *DDR I/O DC Characteristics*

DDR3 Mode

The following table provides input and output DC threshold values and on-die-termination (ODT) recommended values. The conditions for the output threshold values are unterminated outputs loaded with 1 pF capacitor load. The ODT values are measured after impedance calibration.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$V_{IH(DC)}$	DC Input Voltage High	MV_{REF}+0.1	-	MV_{DD}	V	
$V_{IL(DC)}$	DC Input Voltage Low	V_{SS}-0.3	-	MV_{REF}-0.1	V	
V_{OH}	DC Output Logic High	0.8*MV_{DD}	-	-	V	
V_{OL}	DC Output Logic Low	-	-	0.2*MV_{DD}	V	
R_{tt}	Input Termination Resistance (ODT) to MV_{DD}/2	100 54 36	120 60 40	140 66 44	Ω	
Note: 1. Guaranteed by design						

Table 8.3-2 DDR3 Mode DC Characteristics

The following table provides the current value ranges of the power supply and the output ignoring the current direction (absolution value), output impedance calibrated to Z_{out}=34 ohms. The values are simulated parameters; in the event of test silicon, this parameter may not be measured. The leakage current is specified at 105℃ junction temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$I_{OHL(DC)}$	PAD pin, 34-ohm Output source/sink DC current, R_{tt}=120	4.72	5.06	5.51	mA	
$I_{OHL(DC)}$	PAD pin, 34-ohm Output source/sink DC current, R_{tt}=60	7.8	8.43	9.38	mA	
$I_{OHL(DC)}$	PAD pin, 34-ohm Output source/sink DC current, R_{tt}=40	9.94	10.77	12.14	mA	
$I_{OHL(DC)}$	PAD pin, 50-ohm Output source/sink DC current, R_{tt}=120	4.33	4.62	5.05	mA	
$I_{OHL(DC)}$	PAD pin, 50-ohm Output source/sink DC current, R_{tt}=60	6.75	7.23	8.01	mA	
$I_{OHL(DC)}$	PAD pin, 50-ohm Output source/sink DC current, R_{tt}=40	8.26	8.83	9.80	mA	
I_{MVDD}	MV_{DD} standby current; ODT=OFF	0.02	0.12	64.44	mA	
I_{MVDD}	Output Low D_{rv}/R_{tt}=34/60, I_{MVDD} DC current	0.46	0.88	1.66	mA	
I_{MVDD}	Output High D_{rv}/R_{tt}=34/60, I_{MVDD} DC current	8.54	9.59	11.16	mA	

I_{MVDD}	Input Low ODT/R_{tt}=60/34, I_{MVDD} DC current	11.77	13.39	16.22	mA	
I_{MVDD}	Input High ODT/R_{tt}=60/34, I_{MVDD} DC current	5.54	6.62	8.93	mA	
I_{LS}	Input leakage current, SSTL mode, unterminated	0.01	0.11	34.78	mA	
Note: 1. Guaranteed by design						

Table 8.3-3 DDR3 Mode Current Characteristics

The following table provides the DC power only for the I/O in receive mode for different system configurations. The parameters are simulated values; in the event of test silicon, this parameter may not be measured. For the total power, the designer should sum DC power and AC power.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
P_{RCV}	Input mode DC power dissipation, ODT=OFF	0.65	1.37	2.79	mW	
P_{RCV}	Input mode DC power dissipation, ODT/D_{rv}=120/34	7.2	8.98	14.74	mW	
P_{RCV}	Input mode DC power dissipation, ODT/D_{rv}=60/34	15.1	18.95	25.32	mW	
P_{RCV}	Input mode DC power dissipation, ODT/D_{rv}=40/34	22.58	26.71	34.06	mW	
P_{RCV}	Input mode DC power dissipation, ODT/D_{rv}=120/50	7	8.74	14.36	mW	
P_{RCV}	Input mode DC power dissipation, ODT/D_{rv}=60/50	14.74	18.38	24.59	mW	
P_{RCV}	Input mode DC power dissipation, ODT/D_{rv}=40/50	22.1	25.93	32.72	mW	
Note: 1. Guaranteed by design						

Table 8.3-4 DDR3 Mode DC Receive Mode Power Dissipation

The following table provides the DC power only for the I/O in drive mode for different system configurations. The parameters are simulated values; in the event of test silicon, this parameter may not be measured. The standby mode power is specified for 105℃ junction temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
P_{DRV}	Output mode DC power dissipation, R_{tt}=OFF	0.66	1.38	2.80	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =34/120	1.35	2.11	3.50	mW	
P_{DRV}	Output mode DC power	2.56	3.45	4.93	mW	

	dissipation, D_{rv}/R_{tt} =34/60					
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =34/40	3.79	4.82	6.47	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =50/120	1.5	2.29	3.72	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =50/60	2.74	3.67	5.26	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =50/40	3.82	4.89	6.68	mW	

Note:
1. Guaranteed by design

Table 8.3-5 DDR3 Mode DC Drive Mode Power Dissipation (PDR=0)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
P_{DRV}	Output mode DC power dissipation, R_{tt}=OFF	0.05	0.05	0.37	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =34/120	0.7	0.77	1.20	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =34/60	1.91	2.11	2.68	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =34/40	3.15	3.49	4.17	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =50/120	0.86	0.95	1.38	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =50/60	2.12	2.34	2.89	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =50/40	3.21	3.56	4.23	mW	
P_{STB}	Standby mode DC power dissipation (MV_{DD} rail)	0.0285	0.18	101.49	uW	

Note:
1. Guaranteed by design

Table 8.3-6 DDR3 Mode DC Drive Mode Power Dissipation (PDR=1)

DDR3L Mode

The following table provides input and output DC threshold values and on-die-termination (ODT) recommended values. The conditions for the output threshold values are unterminated outputs loaded with 1 pF capacitor load. The ODT values are measured after impedance calibration.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$V_{IH(DC)}$	DC Input Voltage High	MV_{REF}+0.09	-	MV_{DD}	V	

$V_{IL(DC)}$	DC Input Voltage Low	V_{SS}-0.3	-	MV_{REF}-0.09	V	
V_{OH}	DC Output Logic High	0.8*MV_{DD}	-	-	V	
V_{OL}	DC Output Logic Low	-	-	0.2*MV_{DD}	V	
R_{tt}	Input Termination Resistance (ODT) to MV_{DD}/2	100 54 36	120 60 40	140 66 44	Ω	
Note: 1. Guaranteed by design						

Table 8.3-7 DDR3L Mode DC Characteristics

The following table provides the current value ranges of the power supply and the output ignoring the current direction (absolution value), output impedance calibrated to Z_{out}=34 ohms. The values are simulated parameters; in the event of test silicon, this parameter may not be measured. The leakage current is specified at 105℃ junction temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$I_{OHL(DC)}$	PAD pin, 34-ohm Output source/sink DC current, R_{tt}=120	4.29	4.59	5.03	mA	
$I_{OHL(DC)}$	PAD pin, 34-ohm Output source/sink DC current, R_{tt}=60	7.14	7.70	8.47	mA	
$I_{OHL(DC)}$	PAD pin, 34-ohm Output source/sink DC current, R_{tt}=40	9.13	9.90	10.88	mA	
$I_{OHL(DC)}$	PAD pin, 50-ohm Output source/sink DC current, R_{tt}=120	3.84	4.16	4.77	mA	
$I_{OHL(DC)}$	PAD pin, 50-ohm Output source/sink DC current, R_{tt}=60	5.93	6.49	7.70	mA	
$I_{OHL(DC)}$	PAD pin, 50-ohm Output source/sink DC current, R_{tt}=40	7.21	7.93	9.57	mA	
I_{MVDD}	MV_{DD} standby current; ODT=OFF	0.02	0.10	56.78	mA	
I_{MVDD}	Output Low D_{rv}/R_{tt}=34/60, I_{MVDD} DC current	0.30	0.60	1.27	mA	
I_{MVDD}	Output High D_{rv}/R_{tt}=34/60, I_{MVDD} DC current	7.65	8.56	9.85	mA	
I_{MVDD}	Input Low ODT/R_{tt}=60/34, I_{MVDD} DC current	10.53	12.74	13.93	mA	
I_{MVDD}	Input High ODT/R_{tt}=60/34, I_{MVDD} DC current	4.55	6.48	7.47	mA	
I_{LS}	Input leakage current, SSTL mode, unterminated	0.01	0.09	31.79	mA	
Note: 1. Guaranteed by design						

Table 8.3-8 DDR3L Mode Current Characteristics

The following table provides the DC power only for the I/O in receive mode for different system configurations. The parameters are simulated values; in the event of test silicon, this parameter may not be measured. For the total power, the designer should sum DC power and AC power.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
P_{RCV}	Input mode DC power dissipation, ODT=OFF	0.38	0.85	2.00	mW	
P_{RCV}	Input mode DC power dissipation, ODT/D_{rv}=120/34	5.11	6.51	11.69	mW	
P_{RCV}	Input mode DC power dissipation, ODT/D_{rv}=60/34	12.08	16.36	20.28	mW	
P_{RCV}	Input mode DC power dissipation, ODT/D_{rv}=40/34	17.45	21.08	28.50	mW	
P_{RCV}	Input mode DC power dissipation, ODT/D_{rv}=120/50	4.97	6.34	11.38	mW	
P_{RCV}	Input mode DC power dissipation, ODT/D_{rv}=60/50	11.75	15.88	19.69	mW	
P_{RCV}	Input mode DC power dissipation, ODT/D_{rv}=40/50	17.04	20.52	27.69	mW	
Note: 1. Guaranteed by design						

Table 8.3-9 DDR3L Mode DC Receive Mode Power Dissipation

The following table provides the DC power only for the I/O in drive mode for different system configurations. The parameters are simulated values; in the event of test silicon, this parameter may not be measured. The standby mode power is specified for 105℃ junction temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
P_{DRV}	Output mode DC power dissipation, R_{tt}=OFF	0.38	0.85	2.00	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =34/120	0.92	1.42	2.61	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =34/60	1.90	2.49	3.84	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =34/40	2.91	3.61	5.16	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =50/120	1.08	1.58	2.73	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =50/60	2.08	2.70	4.03	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =50/40	2.93	3.69	5.28	mW	

Note:
1. Guaranteed by design

Table 8.3-10 DDR3L Mode DC Drive Mode Power Dissipation (PDR=0)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
P_{DRV}	Output mode DC power dissipation, R_{tt}=OFF	0.00	0.00	0.14	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =34/120	0.52	0.58	0.86	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =34/60	1.49	1.64	2.12	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =34/40	2.51	2.77	3.38	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =50/120	0.67	0.74	1.01	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =50/60	1.69	1.85	2.28	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =50/40	2.56	2.84	3.41	mW	
P_{STB}	Standby mode DC power dissipation (MV_{DD} rail)	0.02566	0.14	82.33	uW	
Note: 1. Guaranteed by design						

Table 8.3-11 DDR3L Mode DC Drive Mode Power Dissipation (PDR=1)

DDR2 Mode

The following table provides input and output DC threshold values and on-die-termination (ODT) recommended values. The conditions for the output threshold values are unterminated outputs loaded with 1 pF capacitor load. The ODT values are measured after impedance calibration.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$V_{IH(DC)}$	DC Input Voltage High	MV_{REF}+0.125	-	MV_{DD}+0.3	V	
$V_{IL(DC)}$	DC Input Voltage Low	V_{SS}-0.3	-	MV_{REF}-0.125	V	
V_{OH}	DC Output Logic High	MV_{DD}-0.28	-	-	V	
V_{OL}	DC Output Logic Low	-	-	MV_{DD}+0.28	V	
R_{tt}	Input Termination Resistance (ODT) to $MV_{DD}/2$	120 60 40	150 75 50	180 90 60	Ω	

Note:
1. Guaranteed by design

Table 8.3-12 DDR2 Mode DC Characteristics

The following table provides the current value ranges of the power supply and the output ignoring the current direction (absolution value), output impedance calibrated to Z_{out}=18 ohms. The values are simulated parameters; in the event of test silicon, this parameter may not be measured. The leakage current is specified at 105℃ junction temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
$I_{OHL(DC)}$	PAD pin, 18-ohm Output source/sink DC current, R_{tt}=150	5.05	5.45	5.84	mA	
$I_{OHL(DC)}$	PAD pin, 18-ohm Output source/sink DC current, R_{tt}=75	9.09	9.89	10.73	mA	
$I_{OHL(DC)}$	PAD pin, 18-ohm Output source/sink DC current, R_{tt}=50	12.4	13.37	15.08	mA	
$I_{OHL(DC)}$	PAD pin, 40-ohm Output source/sink DC current, R_{tt}=150	4.56	4.98	5.40	mA	
$I_{OHL(DC)}$	PAD pin, 40-ohm Output source/sink DC current, R_{tt}=75	7.61	8.47	9.29	mA	
$I_{OHL(DC)}$	PAD pin, 40-ohm Output source/sink DC current, R_{tt}=50	9.77	11.00	12.13	mA	
I_{MVDD}	MV_{DD} standby current; ODT=OFF	0.03	0.17	88.52	mA	
I_{MVDD}	Output Low D_{rv}/R_{tt}=18/75, I_{MVDD} DC current	1.17	2.16	3.77	mA	
I_{MVDD}	Output High D_{rv}/R_{tt}=18/75, I_{MVDD} DC current	10.47	12.33	14.67	mA	
I_{MVDD}	Input Low ODT/R_{tt}=75/18, I_{MVDD} DC current	13.02	16.47	19.86	mA	
I_{MVDD}	Input High ODT/R_{tt}=75/18, I_{MVDD} DC current	4.76	6.73	9.04	mA	
I_{LS}	Input leakage current, SSTL mode, unterminated	0.02	0.14	43.35	mA	
Note: 1. Guaranteed by design						

Table 8.3-13 DDR2 Mode Current Characteristics

The following table provides the DC power only for the I/O in receive mode for different system configurations. The parameters are simulated values; in the event of test silicon, this parameter may not be measured. For the total power, the designer should sum DC power and AC power.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions

P_{RCV}	Input mode DC power dissipation, ODT=OFF	1.88	3.78	7.14	mW	
P_{RCV}	Input mode DC power dissipation, ODT/D_{rv}=150/18	13.55	17.06	27.57	mW	
P_{RCV}	Input mode DC power dissipation, ODT/D_{rv}=75/18	20.64	28.65	36.56	mW	
P_{RCV}	Input mode DC power dissipation, ODT/D_{rv}=50/18	27.36	36.82	46.83	mW	
P_{RCV}	Input mode DC power dissipation, ODT/D_{rv}=150/40	12.86	16.30	26.38	mW	
P_{RCV}	Input mode DC power dissipation, ODT/D_{rv}=75/40	19.55	26.93	34.70	mW	
P_{RCV}	Input mode DC power dissipation, ODT/D_{rv}=50/40	25.8	34.34	43.06	mW	
Note: 1. Guaranteed by design						

Table 8.3-14 DDR2 Mode DC Receive Mode Power Dissipation

The following table provides the DC power only for the I/O in drive mode for different system configurations. The parameters are simulated values; in the event of test silicon, this parameter may not be measured. The standby mode power is specified for 105℃ junction temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
P_{DRV}	Output mode DC power dissipation, R_{tt}=OFF	1.99	3.98	7.49	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =18/150	2.46	4.44	7.92	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =18/75	3.52	5.54	9.05	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =18/50	4.83	6.91	10.60	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =40/150	2.75	4.74	8.25	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =40/75	4.12	6.22	9.86	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =40/50	5.53	7.82	11.66	mW	
Note: 1. Guaranteed by design						

Table 8.3-15 DDR2 Mode DC Drive Mode Power Dissipation (PDR=0)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions

P_{DRV}	Output mode DC power dissipation, R_{tt}=OFF	0.73	1.26	2.39	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =34/120	1.16	1.72	2.92	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =34/60	2.17	2.83	4.20	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =34/40	3.48	4.19	5.75	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =50/120	1.42	2.02	3.37	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =50/60	2.77	3.50	5.09	mW	
P_{DRV}	Output mode DC power dissipation, D_{rv}/R_{tt} =50/40	4.21	5.10	6.82	mW	
P_{STB}	Standby mode DC power dissipation (MV_{DD} rail)	0.051	0.31	168.19	uW	

Note:

1. Guaranteed by design

Table 8.3-16 DDR2 Mode DC Drive Mode Power Dissipation (PDR=1)

8.4 AC Electrical Characteristics

8.4.1 Internal 12 MHz High Speed RC Oscillator (HIRC)

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
AV_{DD_ROSC}	Operating Voltage	1.25		1.31	V	
f_{HIRC}	Oscillator Frequnecy	11.4	12	12.6	MHz	±5%
f_{duty}	Duty	40	50	60	%	
I_{HIRC}	Operating Current	-	20	-	µA	
T_{on} [*1]	Startup Time When Power On	-	20	-	µS	

Note:

1. Guaranteed by design, not tested in production.

`

8.4.2 Internal 32 kHz Low Speec RC Oscillator (LIRC)

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
V_{BAT}	Digital Operating Voltage	2.0	3.0	3.6	V	
f_{LIRC}	Oscillator Frequnecy	20.8	32	43.2	kHz	±35%
f_{duty}	Duty	40	50	60	%	
I_{HIRC} [*1]	Operating Current	-	0.4	-	µA	
T_{on} [*1]	Startup Time When Power On	-	600	-	µS	

Note:

1. Guaranteed by design, not tested in production.

8.4.3 External 24 MHz High Speed Crystal (HXT) Characteristics

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
V_{HXT}	Operation Voltage	3.0	3.3	3.6	V	$V_{HXT} = V_{DDIO0}$
f_{HXT}	Clock Frequency	-	24	-	MHz	-
T_s	Start-up Time	-	1.566		mS	
Rf[*1]	Feedback Resistor		1.5		Mohm	

Note:

1. Guaranteed by design, not tested in production.

8.4.3.1 *Typical Crystal Application Circuits*

Crystal	ESR (ohm)	C1, C2
24 MHz	24	20 pf

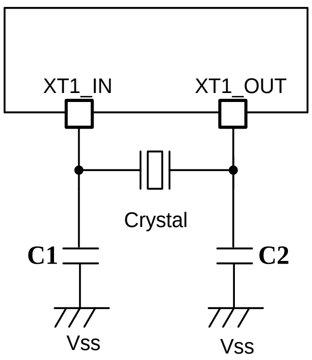


Figure 8-4 Typical HXT Crystal Application Circuit

8.4.4 External 32.768 kHz Low Speed Crystal (LXT) Characteristics

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
V_{LXT}	Operation Voltage	3.0	3.3	3.6	V	$V_{LXT} = V_{BAT}$
f_{LXT}	Clock Frequency	-	32.768	-	kHz	-
T_s [*1]	Start-up Time	-	500	2000	mS	
I_{LXT} [*1]	Operating Current		1.2	2	uA	T_A=25°C, V_{BAT}=3.3V

Note:

1. Guaranteed by characterization results, not tested in production.

8.4.4.1 *Typical Crystal Application Circuits*

Crystal	C1	C2
32.768 kHz	20 pf	20 pf

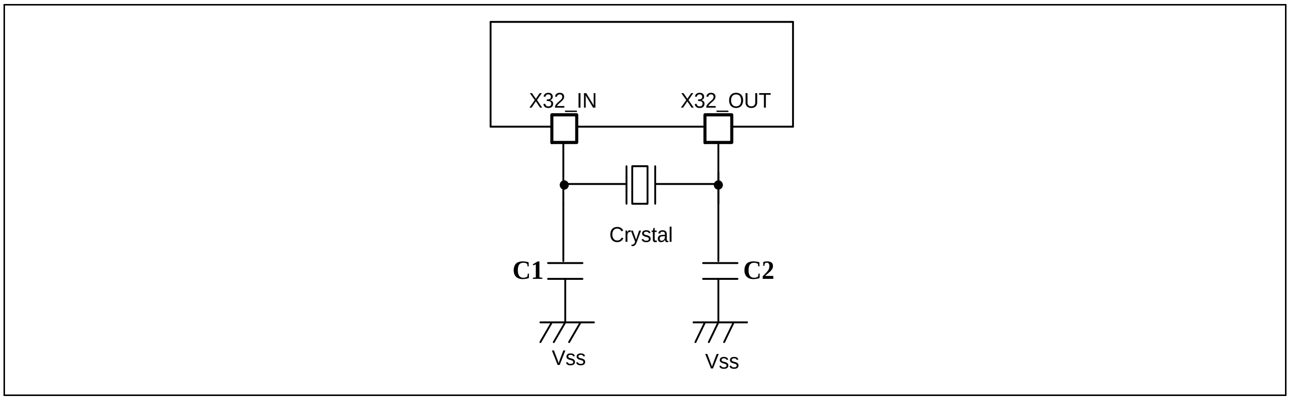


Figure 8-5 Typical LXT Crystal Application Circuit

8.4.5 Power Sequence and nRESET Timing

When $T_{VDDIO*} \geq T_{MVDD} \geq T_{VDD\_CORE}$ (the time of delay gap between < 5 ms is prefer).

Note:

1. The time of delay gap is meaning that timing between T_{VDDIO*} with T_{VDD_CORE}.
2. If the time of delay gap < 5 ms will be effective to prevent that transient phenomenon by power-on.

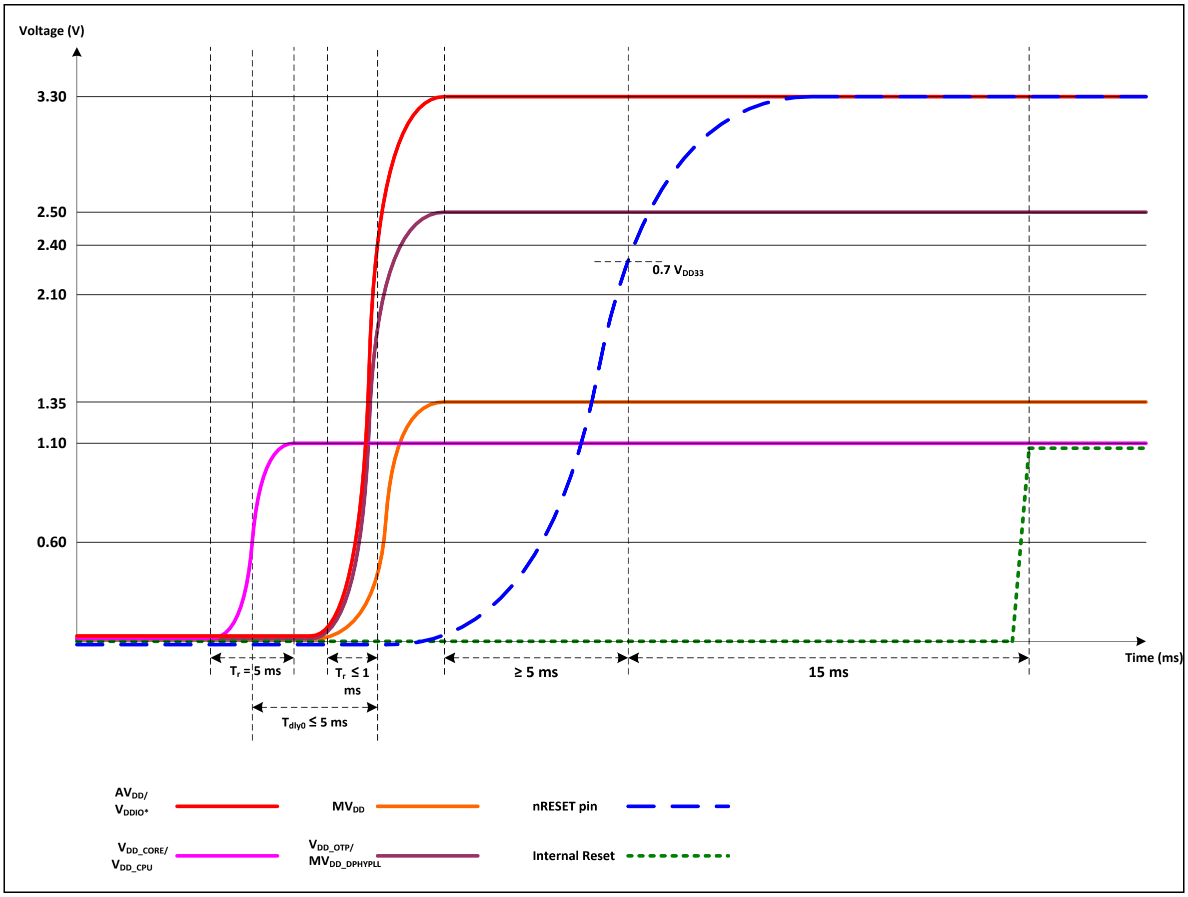


Figure 8-6 Power-up Sequence and nRESET Timing

8.4.5.1 *Power Down Sequence*

Power down sequence between AV_{DD}/V_{DDIO*}, V_{DD_CORE}/V_{DD_CPU} and MV_{DD} is don't care.

Note:

1. T_{VDD_CORE} represents V_{DD_CORE}/V_{DD_CPU} powered time.
2. T_{MVDD} represents MV_{DD} powered time.
3. T_{VDDIO*} represents V_{DDIO} /AV_{DD} powered time.

8.4.6 Operating Conditions at Power-up

Symbol	Description	Min	Max	Unit
T_{VDDIO} [*1]	V_{DDIO} Rise Time Rate	5.5	580	us/V
TA_{VDD} [*2]	A_{VDD} Rise Time Rate	5.5	580	
T_{VDD_OTP} [*3]	V_{DD_OTP} Rise Time Rate	4.2	1250	
T_{VDD_CORE} [*4]	V_{DD_CORE} Rise Time Rate	500	10000	

Note:

1. All $T_{VDDIO[0:10]}$ have same condition
2. T_{AVDD}, T_{AVDD_ADC0}, T_{AVDD_EADC0}, $T_{AVDDH\_PLL[1:2]}$ have same condition
3. $T_{MVDD\_DPHYPLL}$ and T_{VDD_OTP} have same condition
4. T_{VDD_CPU}, T_{VDD_PLL1}, T_{AVDDL_ROSC}, $T_{AVDDL\_PLL[0:2]}$ have same condition

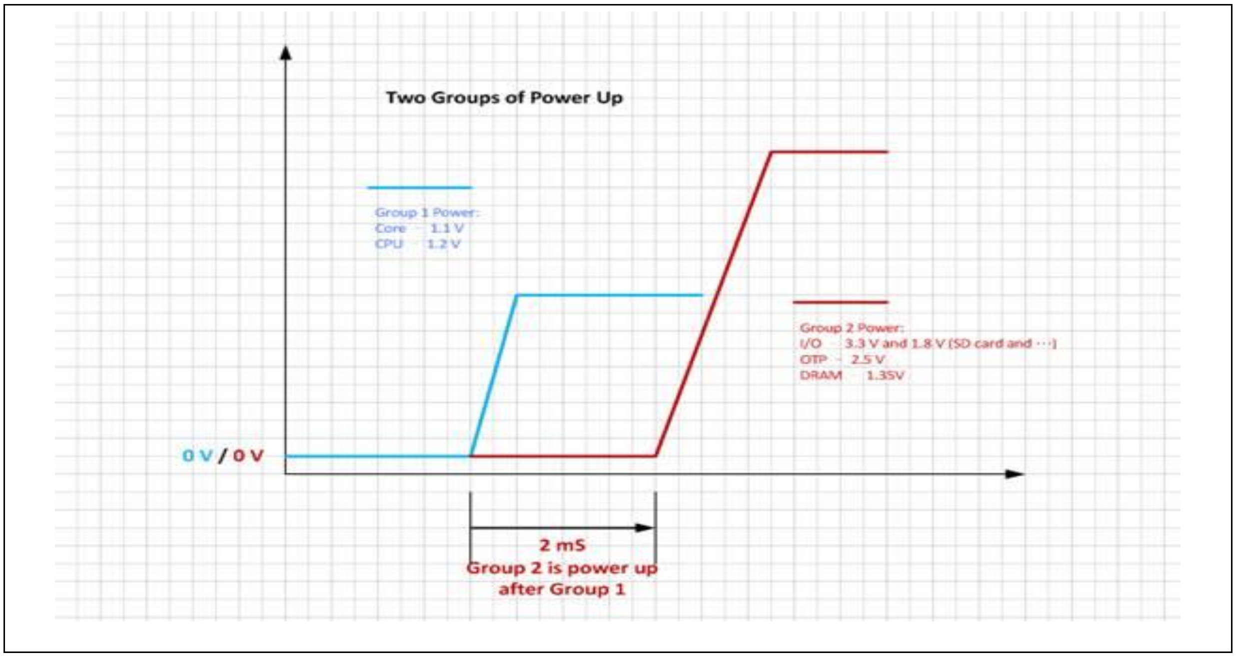


Figure 8-7 Power Sequence and nRESET

8.4.7 PLL Characteristics

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
AV_{DDL_PLL0} [*1]	Operating Voltage Range	1.20		1.31	V	Dedicated Analog Power Supply
f_{PLL_IN}	Input Clock Frequency	1	-	24	MHz	
f_{VCO_OUT}	VCO Frequency	500	-	1500	MHz	
f_{PLL_OUT}	Output Clock Frequency	62.5	-	1500	MHz	
RMS	Period Jitter	-	54	-	ps	VCO freq = 960 MHz; Clean Power T=25℃, AV_{DDL_PLL0} = 1.2V
PK_PK		-	200	-	ps	
I_{OP}	Power Dissipation		3.5		mA	XIN=24MHz; T=25℃, AV_{DDL_PLL0} = 1.2V
I_{PD} [*2]	Power Dissipation (Power down mode)	--	1		uA	T=25℃, AV_{DDL_PLL0} = 1.2V
T_L	Pull_in Time + Locking Time	--	--	0.5	ms	

Note:

1. For the CA-PLL and SYS-PLL are PLL.
2. Guaranteed by design, not tested in production.

8.4.8 Advanced PLL Characteristics

The advanced PLL is a programmable PLL suitable for high speed clock generation, supporting integer mode, fraction mode and spread-spectrum mode.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
AV_{DDH_PLL1} AV_{DDH_PLL2}	3.3v Analog Power Supply	3.0	3.3	3.6	V	
AV_{DDL_PLL1} AV_{DDL_PLL2}	1.1V Analog Power Supply	1.20		1.31	V	
V_{DD_PLL1}	1.1V Digital Power Supply	1.20		1.31	V	
T_J	Operating Junction Temperature Range	-40	25	105	^{o}C	
T_L	Locked Time	-	500	-	us	
I_{DD}	Supply Current (Integer Mode)	-	1	-	mA	When Fvco=0.8GHz
		-	3	-	mA	When Fvco=2.4GHz
IPD	Leakage Current (PD Mode)	-	1	-	uA	f_{REF} = 0 MHz.
f_{REF}	Input Reference Clock Frequency	1		24	MHz	
f_{REF}/M	Input Divider Clock Frequency	1		24	MHz	Integer mode
		10		24	MHz	Fraction or spread-spectrum mode
f_{VCO}	VCO Output Clock Frequency	600		2400	MHz	
f_{PLL}	PLL Output Clock Frequency	85.7		2400	MHz	
$T_{PJ(p-p)}$	Period Jitter(p-p) [*1]	+/-2.5% of VCO period			ps	Integer mode, at output divider = 0/1, clean AVDDL_PLL1 and AVDDL_PLL2. For other output divider configurations, please check Note 1.
$T_{C2C(p-p)}$	Cycle to Cycle Jitter(p-p) [*1]	+/-3.5% of VCO period			ps	
$T_{PJ(p-p)}$	Period Jitter(p-p) [*1]	+/-5% of VCO period			ps	Fraction mode, at output divider = 0/1, clean AVDDL_PLL1 and AVDDL_PLL2. For other output divider configurations, please check Note 1.
$T_{C2C(p-p)}$	Cycle to Cycle Jitter(p-p) [*1][*2]	+/-7% of VCO period			ps	Fraction/SSC mode, at output divider = 0/1, clean AVDDL_PLL1 and AVDDL_PLL2. For other output divider configurations, please check Note 1, 2.
	Spread Range	0	-1.5	-3	%	
F_{mod}	Modulation Frequency	10	30	50	kHz	

Note:

1. For output divider >=2, the period jitter and cycle to cycle jitter at CLKO is related to the VCO frequency (F_{VCO}). It can be calculated by the following equations:
   Integer mode:

Period Jitter, $T_{PJ(p-p)}$=2*2.5% *T_{VCO}*sqrt(DP); Cycle-to-Cycle Jitter, $T_{C2C(p-p)}$=2*3.5% *T_{VCO}*sqrt(output divider); Fraction mode: Period Jitter, $T_{PJ(p-p)}$=2*5% *T_{VCO}*sqrt(output divider); Cycle-to-Cycle Jitter, $T_{C2C(p-p)}$=2*7% *T_{VCO}*sqrt(output divider); SSC mode: Cycle-to-Cycle Jitter, $T_{C2C(p-p)}$=2*7% *T_{VCO}*sqrt(output divider); T_{VCO} =1/F_{VCO}; 2. As SSC modulation can be seen as low frequency jitter, so cycle to cycle jitter is meaningful for SSC mode.

8.4.9 DLL Characteristics

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
V_{DD_CORE}	Digital Supply Voltage	1.20		1.31	V	
F_{REF}	Input Clock CLK Frequency	100	200	300	MHz	
T_{lock}	Lock-In Time	-	-	2048	Cycle	From simulation
$T_{REFRESH\_DLL}$	Pulse Width of REFRESH_DLI	4	-	-	Cycle	From simulation
$T_{Refresh}$	Slave Refresh Tim	-	-	2	Cycle	From simulation
t_{delay}	Delay Time of One Step	-	94	-	ps	From simulation
DC_{ref}	Reference Duty Cycle	-	50	-	%	From simulation
DC_{dqso}	Duty Cycle Degradation	-2	0	+2	%	From simulation
T_J	Junction Temperature	-40	25	105	^oC	
I_{dm}	Master DLL Operation Current	-	550	-	uA	From simulation
I_{ds}	Slave DLL Operation Current	-	170	-	uA	
I_{pdm}	Master DLL Leakage Current	-	2	-	uA	From simulation
I_{pds}	Slave DLL Leakage Current	-	1	-	uA	
Note: Test condition: F_{REF}=200MHz, and PARAM_DQS_PHASE=0011						

8.5 Analog Characteristics

8.5.1 12-bit SAR Enhanced Analog-to-Digital Converter (EADC)

Description		Min	Typ.	Max	Unit
Resolution			12		Bit
Analog input					
Input Sampling Capacitor(Cs)[*7]			5		pF
Input Sampling Resistance (Rs)	SPEED=0		2500		Ω
	SPEED=1		600		Ω
Positive Reference(V_{REF_EADC0})		1.6	V_{REF_EADC0}	AV_{DD_EADC0}	V
Negitive Reference(A_{VSS})		0		0.1	V
Input range[3](Single-End Mode)			V_{REF_EADC0}- 0		V
Input range[3](Differential Mode)			2*(V_{REF_EADC0}- 0)		Vpp
Performance					
DNL		-1.5	1.06	4.5	LSB
INL		-3	0.96	3.5	LSB
SNR @Fin=50KHz		54	62		dB
THD @Fin=50KHz		54	-62		dB
Offset Error before calibration		-25		+25	LSB
Offset Error after calibration		-5		7	LSB
Timing Characteristics					
Input Clock Frequency(F_{CLK}), SPEED=0			16	80	MHz
Input Clock Frequency(F_{CLK}), SPEED=1				16	MHz
Conversion Cycle(t_C)			17+K[*6]		CLK
Sample Rate(Fs)	SPEED=0			0.94	MSPS
	SPEED=1			4.7	MSPS
Start-up Time from ADC Power Down Mode[*4]			5[*7]		us
Start-up Time from Fully Power Down Mode[*5]			1[*7]		ms

Note:

1. Specifications are estimated and subject to change without notice.
2. AV_{DD_EADC0} should be larger than V_{REF_EADC0}.
3. Input Range is decreased by the offset error before calibration.
4. ADC Power Down: PD_ADC=1 PD_REF=0
5. Fully Power Down: PD_ADC=1 PD_REF=1; the start-up time depends on the V_{REF_EADC0} value and external-decap on V_{REF_EADC0}, typical case V_{REF_EADC0}=2.5V, decap=1uF.
6. K =0, 2, 4, 6, controlled by SEL_SMP[1:0]. Below description will take K=0 for example unless otherwise noted.
7. Design guarantee.

8.5.2 12-bit SAR Analog-to-Digital Converter (ADC)

Description		Min	Typ.	Max	Unit
Resolution		12			Bit
Analog input					
Input Sampling Capacitor(C_S)[*1]			7.8		pF
Input Sampling Switch[*1] Resistance[*1] (R_S)	SPEED=0		1000		Ω
	SPEED=1		3500		Ω
Touch Screen Driver Impedance[*1]				20	Ω
Full scale input Range		0		AV_{DD_ADC0}	V
Performance					
DNL			+/-1.5		LSB
INL			+/-3		LSB
SNR2,3		54	62		dB
THD2,3		54	-62		dB
Offset Error			+/-9		LSB
Timing Characteristics					
Input Clock Frequency(F_{CLK}), SPEED=0				16	MHz
Input Clock Frequency(F_{CLK}), SPEED=1				3.2	MHz
Conversion Cycle(t_C)			22		CLK Cycle
Sample Rate(Fs)	SPEED=0			727	Msps
	SPEED=1			145	Ksps
Start-up Time From Power Down				100	us

Note:

1. Design guarentee.

8.5.3 Low Voltage Detection (LVD) and Low Voltage Reset (LVR)

Symbol	Description	Min	Typ.	Max	Unit	Test Conditions
AV_{DD}	3.3V Analog power	3.0	3.3	3.6	V	
V_{THR_1}	VDT AV_{DD} Level 1	-	2.8	-	V	
V_{THF_1}		-	2.75	-	V	
V_{THR_2}	VDT AV_{DD} Level 2	-	2.6	-	V	
V_{THF_2}		-	2.55	-	V	
V_{R_RST}	LVR AV_{DD}	-	2.4	-	V	
V_{F_RST}		-	2.35	-	V	
td	Drive Delay	-	0.5[*1]	-	uS	
Iq	Quiescent Current	-	0.9[*1]	-	uA	

Note:

1. Guaranteed by characterization results, not tested in production.

8.5.4 Power-On Reset (POR33)

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
AV_{DD}	Power Supply	-	3.3	-	V	-
SR_PO[*1]	Power On Slew Rate	5.7	-	600	V/ms	-
SR_PD[*1]	Power Down Slew Rate	-	-	20	V/ms	
V_{TR}	Reset Trigger Level	-	2.4	-	V	72%AV_{DD}
V_{TF}	Reset Deassert Level	-	2.3	-	V	-
V_{HYS}	Hysteresis Window		100		mV	
I_{DD}[*1]	Quiescent Current		10		uA	

Note:

1. Guaranteed by characterization results, not tested in production.

8.5.5 Power-On Reset (POR25)

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
V_{DD_OTP}	Power Supply	-	2.5	-	V	-
SR_PO[*1]	Power On Slew Rate	2	-	600	V/ms	-
SR_PD[*1]	Power Down Slew Rate	-	-	20	V/ms	
V_{TR}	Reset Trigger Level	-	2.1	-	V	-
V_{TF}	Reset Deassert Level	-	2.0	-	V	-
V_{HYS}	Hysteresis Window		100		mV	
I_{DD}[*1]	Quiescent Current		10		uA	

Note:

1. Guaranteed by characterization results, not tested in production.

8.5.6 Power-On Reset (POR11)

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
V_{DD_CORE}	1.2V Supply Voltage	1.1	1.2	1.3	V	
V_{TR} [*1]	V_{DD_CORE} Power up Trigger Level.	0.6			V	
V_{TF}	V_{DD_CORE} Power down Trigger Level.	0.7			V	
V_{HYS} [*1]	Hysteresis	100			mV	
Icc [*1]	Current From V_{DD_CORE} to V_{SS}		6		uA	
Tr [*1]	Rising Time of V_{DD_CORE}	500n		10m	Sec	

Note:

1. Guaranteed by characterization results, not tested in production.

8.5.7 Temperature Sensor

Temperature sensor is a CMOS smart sensor which monitors temperature on-chip. It monitors chip temperature within the range of -40℃~125℃.

AV_{DD} =3.3V±10%, unless otherwise noted.

Symbol	Description	Min	Typ	Max	Unit
AV_{DD}	Power Supply	3.0	3.3	3.6	V
T_{OP}	Operating Temperature Range	-40	25	105	^{O}C
I_{OP}	Operating Current (F_{CLK}=100KHz)	-	200		uA
I_{PD}	Power Down Current	-	2		uA
T_{CONV}	Data Conversion Time (F_{CLK}=100KHz)	-	350		ms
F_{CLK}	Clock Input Frequency[*1]	10	100	200	KHz
Temperature Sensor Characteristics					
T_{RNG}[*2]	Temperature Measure Range	-40	-	125	^{O}C
T_{RSLT}[*2]	Temperature Measure Resolution	-	0.1	-	^{O}C/LSB
T_{INACC}[*2]	Inaccuracy of Temperature Sensor	-5	-	5	^{O}C
Note: 1. The actual sampling rate is CLK/2^{15} 2. Guaranteed by characterization results, not tested in production.					

8.5.8 USB 2.0 PHY

8.5.8.1 *Low/Full-Speed DC Electrical Specifications*

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
V_{OL} [*2]	Output Low (Driven)	-	-	0.3	V	1.5k RPU on DP to 3.6V
V_{OH} [*2]	Output High (Driven)	2.8	-	-	V	15k RPD on DP, DM to V_{SS}
V_{DI} [*2]	Differential Input Sensitivity	0.2	-	-	V	$\lvert V_{USB0\_DP}–V_{USB0\_DM}\rvert$
V_{CM} [*2]	Differential Common-Mode Range	0.8	-	2.5	V	
V_{IL} [*2]	Single-Ended Input Low	-	-	0.8	V	-
V_{IH} [*2]	Single-Ended Input High	2.0	-	-	V	-
R_{PU} [*2]	Pull-Up Resistor	1.35	1.5	1.65	kΩ	
R_{PD_DP} [*2]	D+ Pull-Down Resistor	13.5	15	16.5	kΩ	
R_{PD_DM} [*2]	D- Pull-Down Resistor	13.5	15	16.5	kΩ	
Z_{DRV} [*2]	Driver Output Resistance	28	-	44	Ω	Steady state drive[*1]
C_{IN} [*2]	Transceiver Low-Speed Donwstream Port Capacitance	200		600	pF	Pin to V_{SS}
C_{IN} [*2]	Transceiver Low-Speed Upstream Port Capacitance	50		150	pF	Pin to V_{SS}
C_{IN} [*2]	Transceiver Full-Speed Capacitance		50		pF	

Note:

1. Driver output resistance doesn’t include series resistor resistance.
2. Guaranteed by design, not tested in production.

8.5.8.2 *High-Speed DC Electrical Specifications*

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
V_{HSDI} [*1]	High Speed Differential Input Signal Level	150	-	-	mV	$\lvert V_{USB0\_DP}–V_{USB0\_DM}\rvert$
V_{HSQ} [*1]	High Speed Squelch Detection Threshold	100	125	150	mV	$\lvert V_{USB0\_DP}–V_{USB0\_DM}\rvert$
V_{HSCM} [*1]	High Speed Common Mode Voltage Range	-50	-	500	mV	
V_{HSOH} [*1]	High Speed Data Signaling High	300	400	440	mV	
V_{HSOL} [*1]	High Speed Data Signaling Low	-10	0	10	mV	
V_{CHIRPJ} [*1]	Chirp J Level	700	-	1100	mV	
V_{CHIRPK} [*1]	Chirp K Level	-900	-	-500	mV	

R_{HSDRV} [*1]	High Speed Driver Output Resistance	40.5	45	49.5	Ω	

Note:

1. Guaranteed by design, not tested in production.

8.5.8.3 *USB Low-Speed Driver AC Electrical Characteristics*

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
T_{LRISE} [*1]	Rise Time	75	-	300	ns	CL=200pF, 10% to 90% of $\|V_{OH}-V_{OL}\|$
T_{LFALL} [*1]	Fall Time	75	-	300	ns	CL=200pF, 10% to 90% of $\|V_{OH}-V_{OL}\|$
V_{LCR} [*1]	Crossover Voltage	1.3	-	2.0	V	Excluding the first transition from idle state

Note:

1. Guaranteed by design, not tested in production.

8.5.8.4 *USB Full-Speed Driver AC Electrical Characteristics*

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
V_{FRISE} [*1]	Rise Time	4	-	20	ns	CL=50pF, 10% to 90% of $\|V_{OH}-V_{OL}\|$
V_{FFALL} [*1]	Fall Time	4	-	20	ns	CL=50pF, 10% to 90% of $\|V_{OH}-V_{OL}\|$
V_{FCR} [*1]	Crossover Voltage	1.3	-	2.0	V	Excluding the first transition from idle state

Note:

1. Guaranteed by design, not tested in production.

8.5.8.5 *USB High-Speed Driver AC Electrical Characteristics*

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
V_{HRISE} [*1]	High Speed Driver Rise Time	500	-	900	ps	CL<10pF
V_{HFALL} [*1]	High Speed Driver Fall Time	500	-	900	ps	CL<10pF

Note:

1. Guaranteed by design, not tested in production.

8.6 Communications Characteristics

8.6.1 EBI Dynamic Characteristics

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
t_{ACS}	Address Setup Time to EBI_nCS Falling Edge	-	0	-	T_{CLK} [*1]	-
t_{COS}	EBI_nCS Setup Time to EBI_nWE or EBI_nOE Falling Edge	-	1	-	T_{CLK} [*1]	-
t_{ACC}	EBI_nWE or EBI_nOE Active Low Time	3	-	32	T_{CLK} [*1]	-
t_{COH}	EBI_nCS Hold Time from EBI_nWE or EBI_nOE Rising Edge	0	-	8	T_{CLK} [*1]	-
t_{DS}	EBI_DATA Read Setup Time to EBI_nOE Rising Edge	3	-	-	T_{CLK} [*1]	-

Note:

1. T_{CLK} is the period of EBI's operating clock.

Table 8.6-1 EBI Dynamic Characteristics

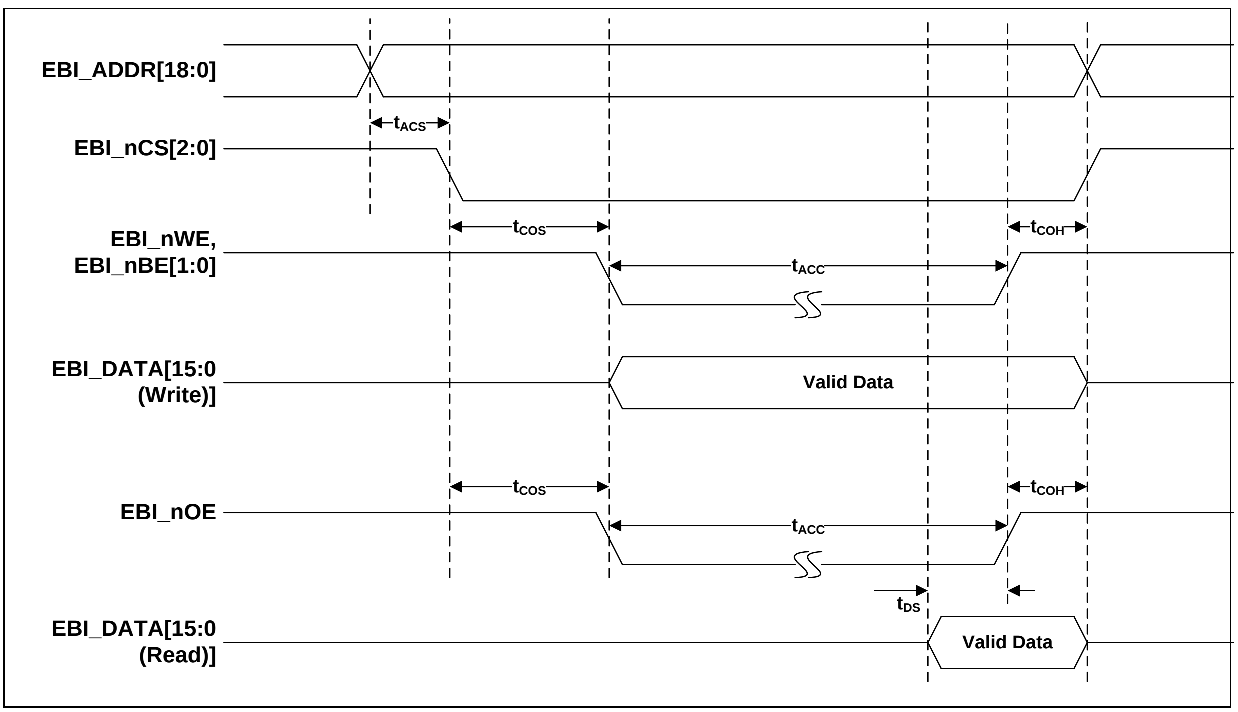


Figure 8-8 EBI Timing Diagram

8.6.2 I²C Dynamic Characteristics

Symbol	Description	Standard Mode[*1][*2]		Fast Mode[*1][*2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL Low Period	4.7	-	1.3	-	µs
t_{HIGH}	SCL High Period	4	-	0.6	-	µs
$t_{SU; STA}$	Repeated START Condition Setup Time	4.7	-	0.6	-	µs
$t_{HD; STA}$	START Condition Hold Time	4	-	0.6	-	µs
$t_{SU; STO}$	STOP Condition Setup Time	4	-	0.6	-	µs
t_{BUF}	Bus Free Time	4.7[*3]	-	1.2[*3]	-	µs
$t_{SU;DAT}$	Data Setup Time	250	-	100	-	ns
$t_{HD;DAT}$	Data Hold Time	0[*4]	3.45[*5]	0[*4]	0.8[*5]	µs
t_r	SCL/SDA Rise Time	-	1000	20+0.1C_b	300	ns
t_f	SCL/SDA Fall Time	-	300	-	300	ns
C_b	Capacitive Load For Each Bus Line	-	400	-	400	pF

Note:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-2 I²C Dynamic Characteristics

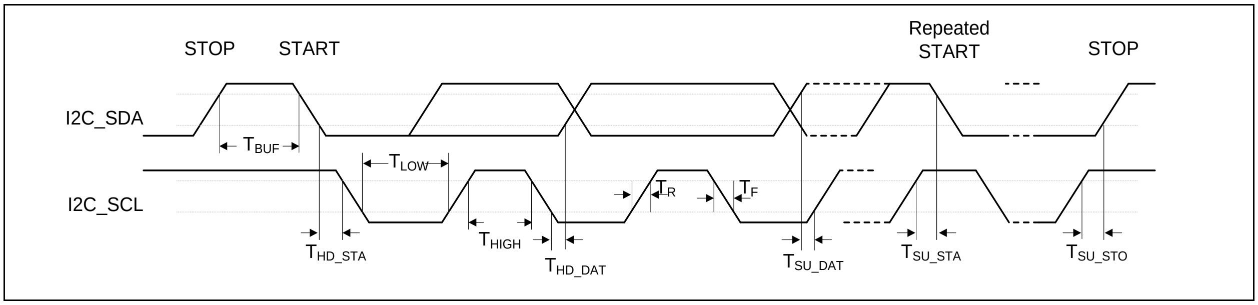


Figure 8-9 I²C Timing Diagram

8.6.3 SPI Dynamic Characteristics

8.6.3.1 *SPI Master Mode Dynamic Characteristics*

Symbol	Description	Specificaitons				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/T_{SPICLK}$	SPI Clock Frequency	-	-	100	MHz	$3.0\ V \leq V_{DD} \leq 3.6\ V$, $C_L = 30\ pF$
t_{CLKH}	Clock Output High Time	$T_{SPICLK} / 2$			ns	
t_{CLKL}	Clock Output Low Time	$T_{SPICLK} / 2$			ns	
t_{DS}	Data Input Setup Time	1.3	-	-	ns	
t_{DH}	Data Input Hold Time	3.3	-	-	ns	
t_V	Data Output Valid Time	-	-	1.0	ns	
Note:						

Table 8.6-3 SPI Master Mode Dynamic Characteristics

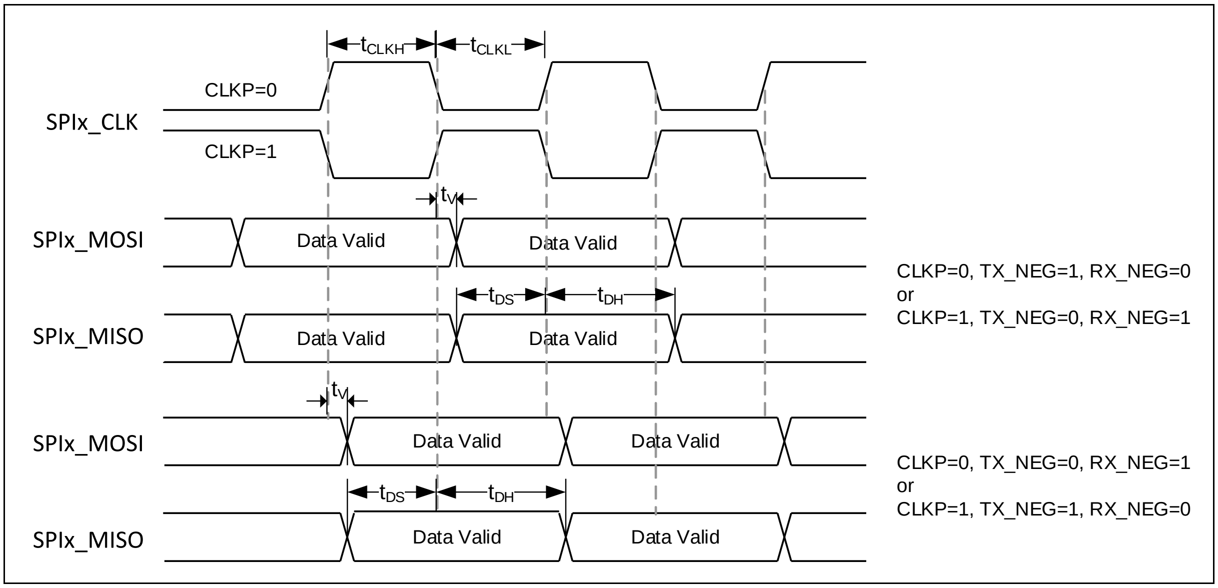


Figure 8-10 SPI Master Mode Timing Diagram

8.6.3.2 *SPI Slave Mode Dynamic Characteristics*

Symbol	Description	Specificaitons				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/T_{SPICLK}$	SPI Clock Frequency	-	-	21.5	MHz	3.0 V ≤ V_{DDIO} ≤ 3.6 V, CL = 30 pF
t_{CLKH}	Clock Output High Time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock Output Low Time	T_{SPICLK} / 2			ns	
t_{SS}	Slave Select Setup Time	1 T_{SPICLK} + 2ns	-	-	ns	3.0 V ≤ V_{DDIO} ≤ 3.6 V, CL = 30 pF
t_{SH}	Slave Select Hold Time	1 T_{SPICLK}	-	-	ns	
t_{DS}	Data Input Setup Time	1.8	-	-	ns	
t_{DH}	Data Input Hold Time	3.8	-	-	ns	
t_V	Data Output Valid Time	-	-	23.2	ns	3.0 V ≤ V_{DDIO} ≤ 3.6 V, CL = 30 pF
Note:						

Table 8.6-4 SPI Slave Mode Dynamic Characteristics

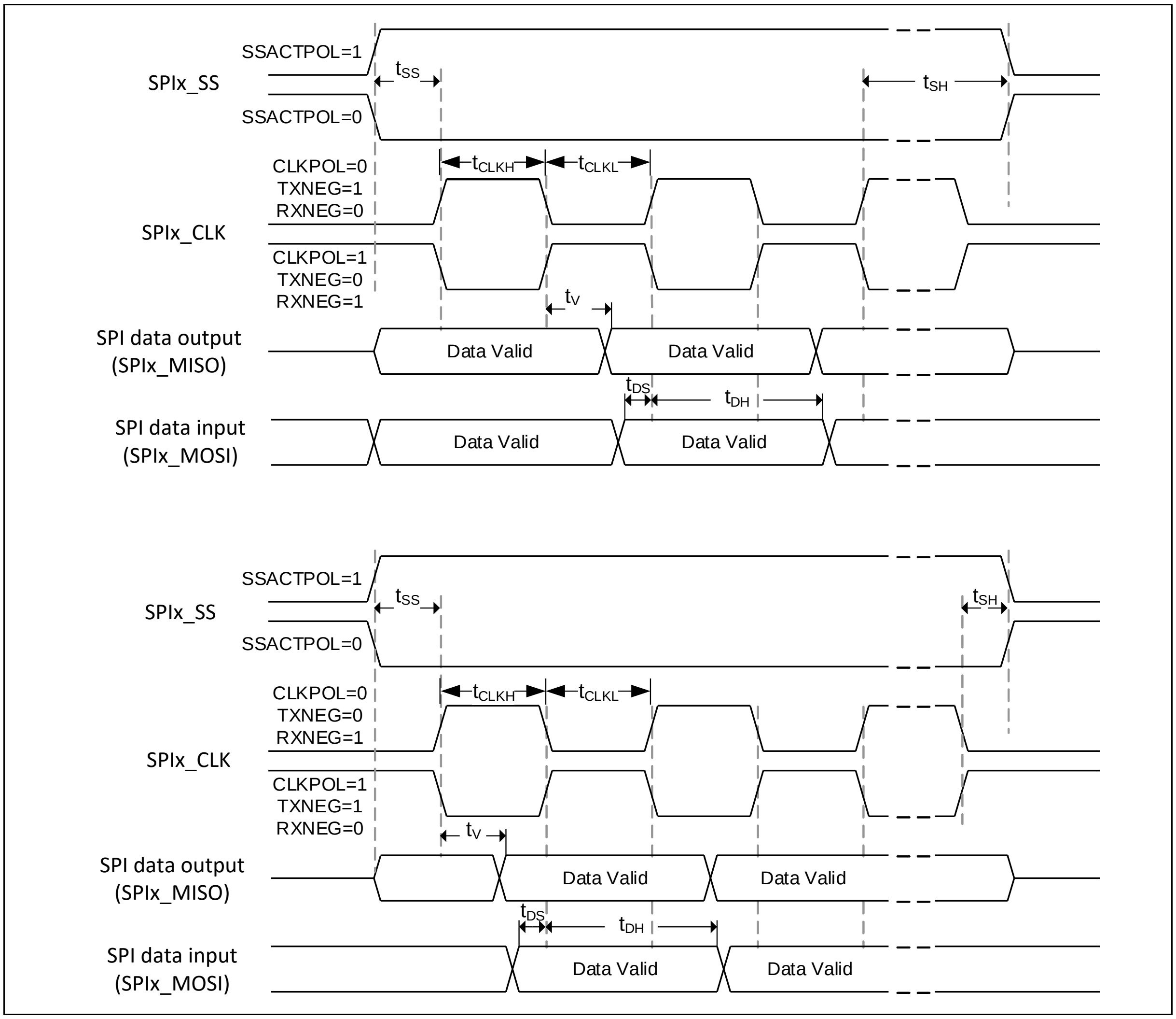


Figure 8-11 SPI Slave Mode Timing Diagram

8.6.4 QSPI Dynamic Characteristics

8.6.4.1 *QSPI Master Mode Dynamic Characteristics*

Symbol	Description	Specificaitons				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} 1/ T_{SPICLK}	SPI Clock Frequency	-	-	100	MHz	3.0 V ≤ V_{DDIO} ≤ 3.6 V, C_L = 30 pF
t_{CLKH}	Clock Output High Time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock Output Low Time	T_{SPICLK} / 2			ns	
t_{DS}	Data Input Setup Time	4.0	-	-	ns	
t_{DH}	Data Input Hold Time	5.0	-	-	ns	
t_V	Data Output Valid Time	-	-	3.9	ns	
Note:						

Table 8.6-5 QSPI Master Mode Dynamic Characteristics

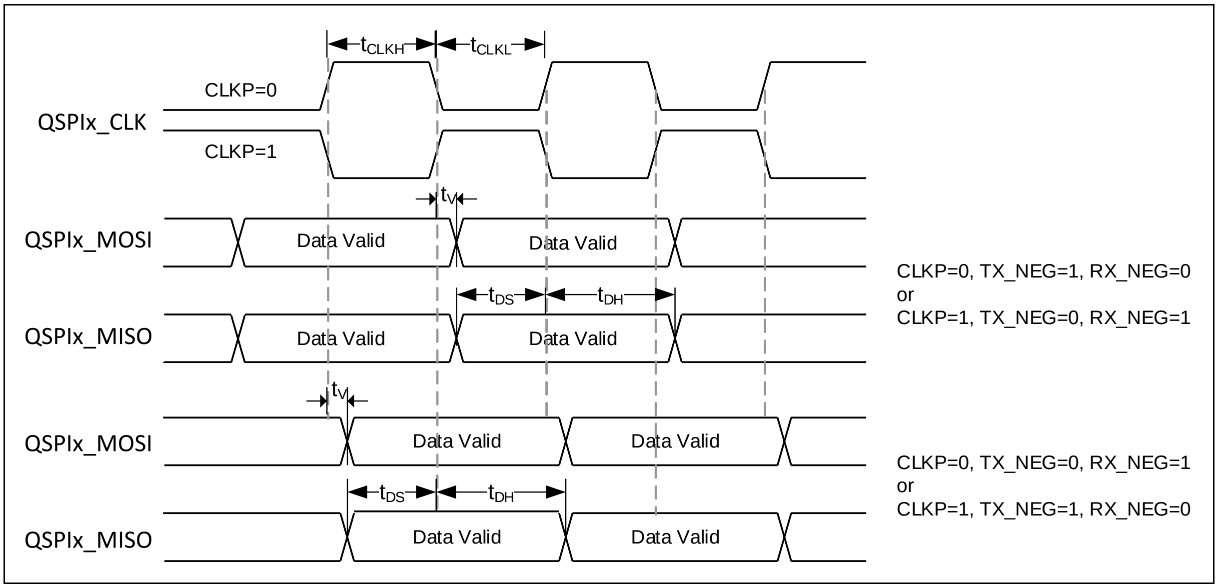


Figure 8-12 QSPI Master Mode Timing Diagram

8.6.4.2 *QSPI Slave Mode Dynamic Characteristics*

Symbol	Description	Specificaitons				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/T_{SPICLK}$	SPI Clock Frequency	-	-	18	MHz	3.0 V ≤ V_{DDIO} ≤ 3.6 V, CL = 30 pF
t_{CLKH}	Clock Output High Time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock Output Low Time	T_{SPICLK} / 2			ns	
t_{SS}	Slave Select Setup Time	1 T_{SPICLK} + 2ns	-	-	ns	3.0 V ≤ V_{DDIO} ≤ 3.6 V, CL = 30 pF
t_{SH}	Slave Select Hold Time	1 T_{SPICLK}	-	-	ns	
t_{DS}	Data Input Setup Time	4.1	-	-	ns	
t_{DH}	Data Input Hold Time	5.1	-	-	ns	
t_V	Data Output Valid Time	-	-	27.6	ns	3.0 V ≤ V_{DDIO} ≤ 3.6 V, CL = 30 pF
Note:						

Table 8.6-6 QSPI Slave Mode Dynamic Characteristics

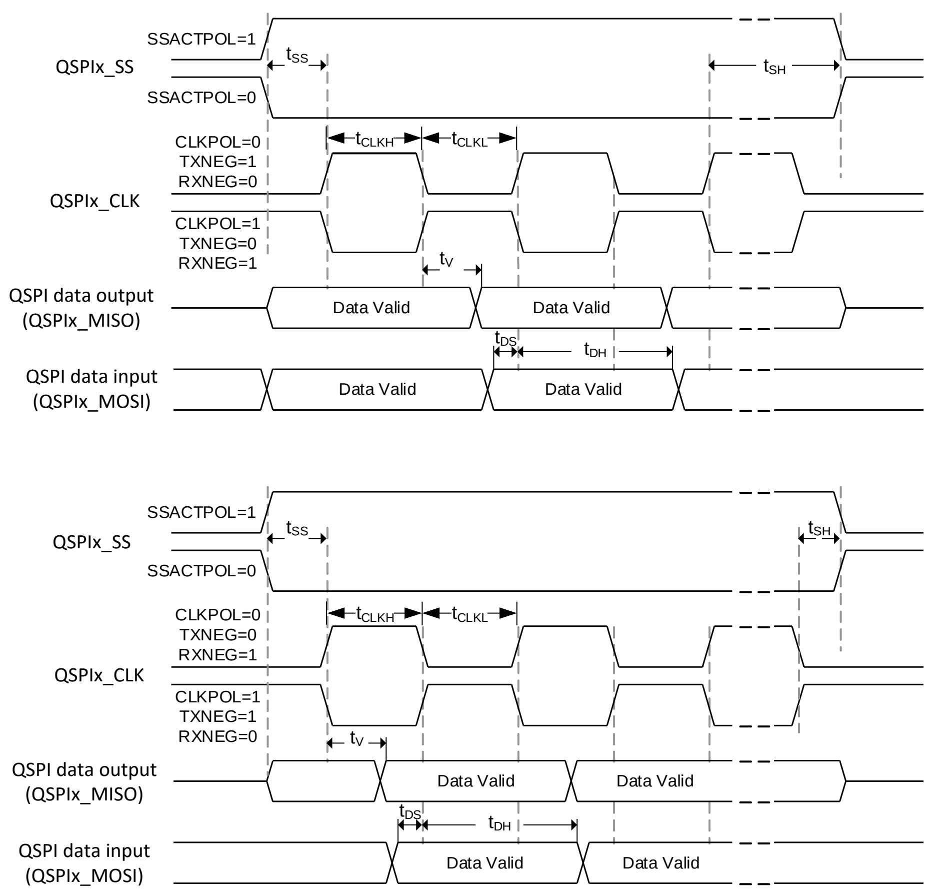


Figure 8-13 QSPI Slave Mode Timing Diagram

8.6.5 I²S Dynamic Characteristics

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
$t_{P\_I2S\_BITCLK}$	I2S_BITCLK Period	50	-	-	ns	-
$t_{H\_I2S\_BITCLK}$	I2S_BITCLK High Time	25	-	-	ns	-
$t_{L\_I2S\_BITCLK}$	I2S_BITCLK Low Time	25	-	-	ns	-
$t_{DLY\_I2S\_DO}$	I2S_BITCLK Rising to Valid I2S_WS or I2S_DATAO Delay	-	-	6	ns	-
$t_{HD\_I2S\_DO}$	I2S_WS or I2S_DATAO Hold Time from I2S_BITCLK Rising	1	-	-	ns	
$t_{SU\_I2S\_DI}$	I2S_DATAI Setup Time to I2S_BITCLK Rising	5	-	-	ns	-
$t_{HD\_I2S\_DI}$	I2S_DATAI Hold Time from I2S_BITCLK Rising	3	-	-	ns	-

Table 8.6-7 I²S Dynamic Characteristics

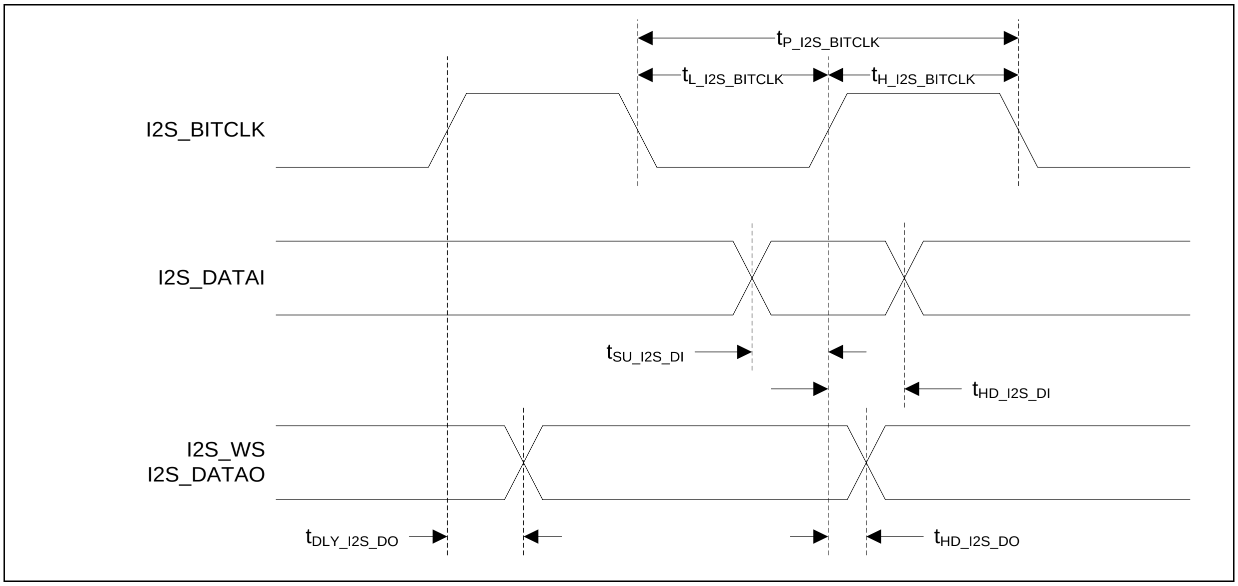


Figure 8-14 I²S Timing Diagram

8.6.6 Ethernet Dynamic Characteristics

8.6.6.1 *RMII Dynamic Characteristics*

Symbol	Description	Min	Typ	Max	Unit	Test Condition
$t_{P\_RMII\_REFCLK}$	RMII_REFCLK Period	-	20.0 +/- 50 ppm	-	ns	-
$t_{H\_RMII\_REFCLK}$	RMII_REFCLK High Time	8.0	10.0	12.0	ns	-
$t_{L\_RMII\_REFCLK}$	RMII_REFCLK Low Time	8.0	10.0	12.0	ns	-
$t_{DLY\_RMII\_TX}$	RMII_REFCLK Rising to Valid RMII_TXEN, RMII_TXDATA0 and RMII_TXDATA1 Delay	-	-	17.0	ns	-
$t_{SU\_RMII\_RX}$	RMII_CRSDV, RMII_RXDATA0 and RMII_RXDATA1 Setup Time to RMII_REFCLK Rising	4	-	-	ns	-
$t_{HD\_RMII\_RX}$	RMII_CRSDV, RMII_RXDATA0 and RMII_RXDATA1 Hold Time from RMII_REFCLK Rising	2	-	-	ns	-

Table 8.6-8 RMII Dynamic Characteristics

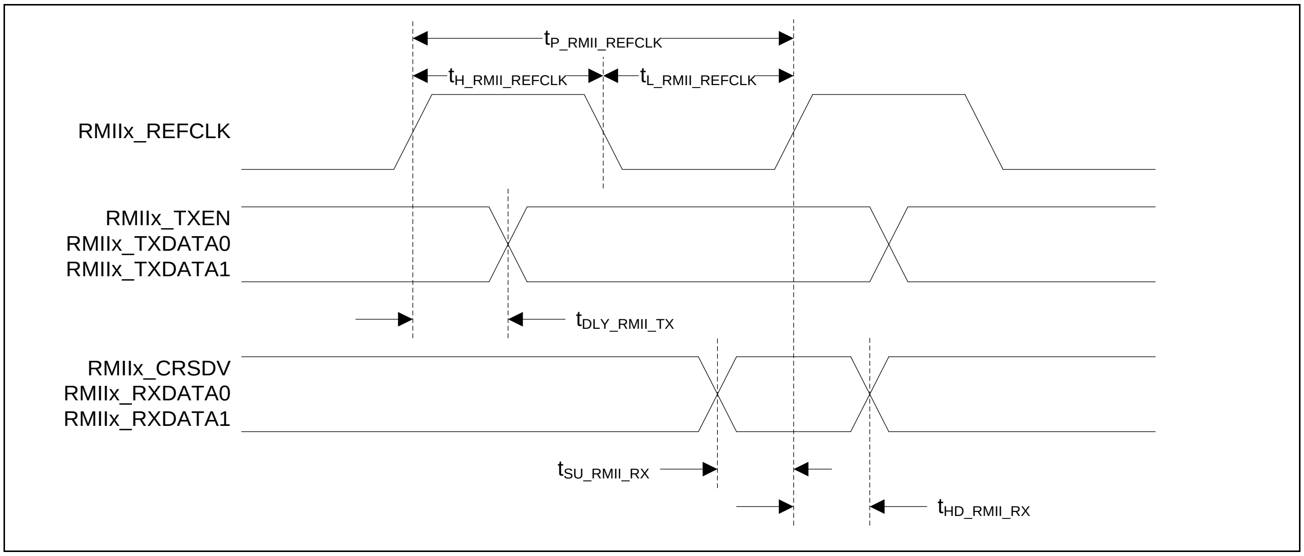


Figure 8-15 RMII Interface Timing Diagram

8.6.6.2 *RGMII Dynamic Characteristics*

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
t_{RGMII_CLK}	RGMII_REFCLK Period	7.2	8	8.8	ns	-
t_{RGMII_CLKH}	RGMII_REFCLK High Time	3.6	4	4.4	ns	-
t_{RGMII_CLKL}	RGMII_REFCLK Low Time	3.6	4	4.4	ns	-
t_{SKEW_TX}	RGMII_TXCTL and RGMII_TXD to RGMII_TXCLK Output Skew at Transmitter	-1.5	-	0.3	ns	-
t_{SKEW_RX}	RGMII_RXCTL and RGMII_RXD to RGMII_RXCLK Output Skew at Receiver	1	-	2.6	ns	-

Table 8.6-9 RGMII Dynamic Characteristics

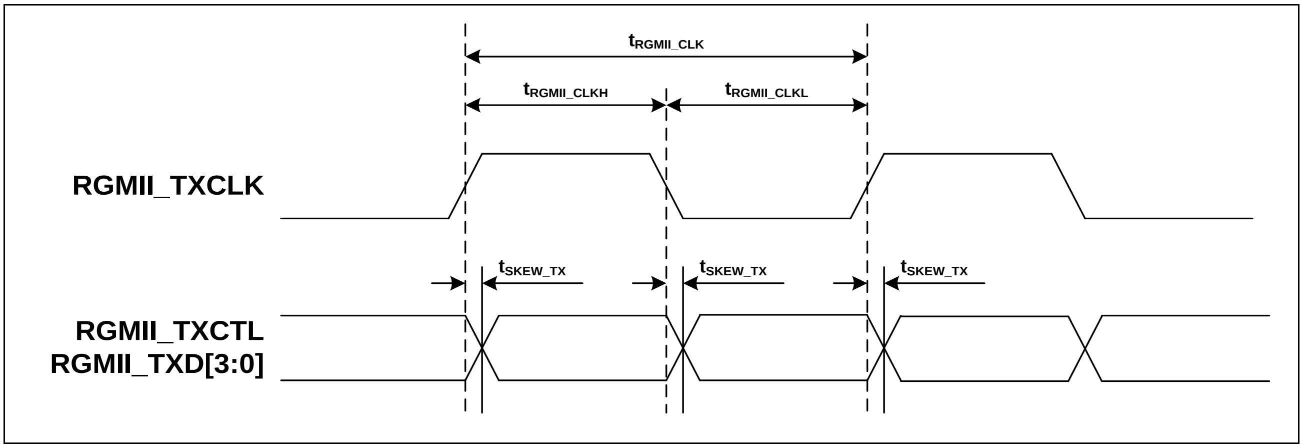


Figure 8-16 RGMII Transmit Timing Diagram

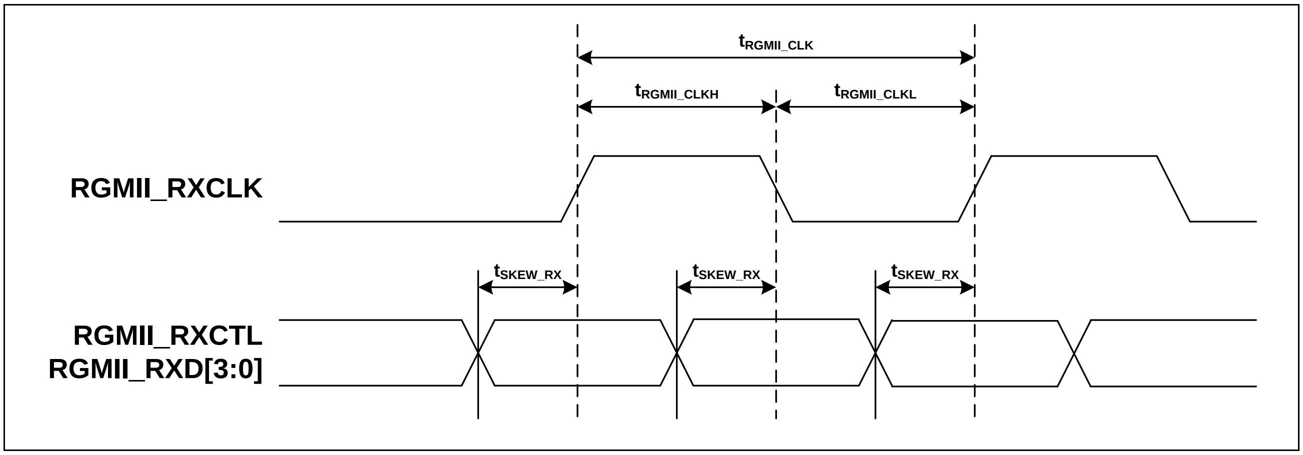


Figure 8-17 RGMII Receive Timing Diagram

8.6.6.3 *Ethernet PHY Management Interface Dynamic Characteristics*

Symbol	Description	Min	Typ	Max	Unit	Test Condition
$t_{P\_RMII\_MDC}$	RMII_MDC Period	400	-	-	ns	-
$t_{H\_RMII\_MDC}$	RMII_MDC High Time	200	-	-	ns	-
$t_{L\_RMII\_MDC}$	RMII_MDC Low Time	200	-	-	ns	-
$t_{DLY\_RMII\_MDIOWR}$	RMII_MDC Falling to Valid RMII_MDIO Delay	-	-	10	ns	-
$t_{SU\_RMII\_MDIORD}$	RMII_MDIO Setup Time to RMII_MDC Rising	10	-	-	ns	-
$t_{HD\_RMII\_MDIORD}$	RMII_MDIO Hold Time from RMII_MDC Rising	10	-	-	ns	-

Table 8.6-10 Ethernet PHY Management Interface Dynamic Characteristics

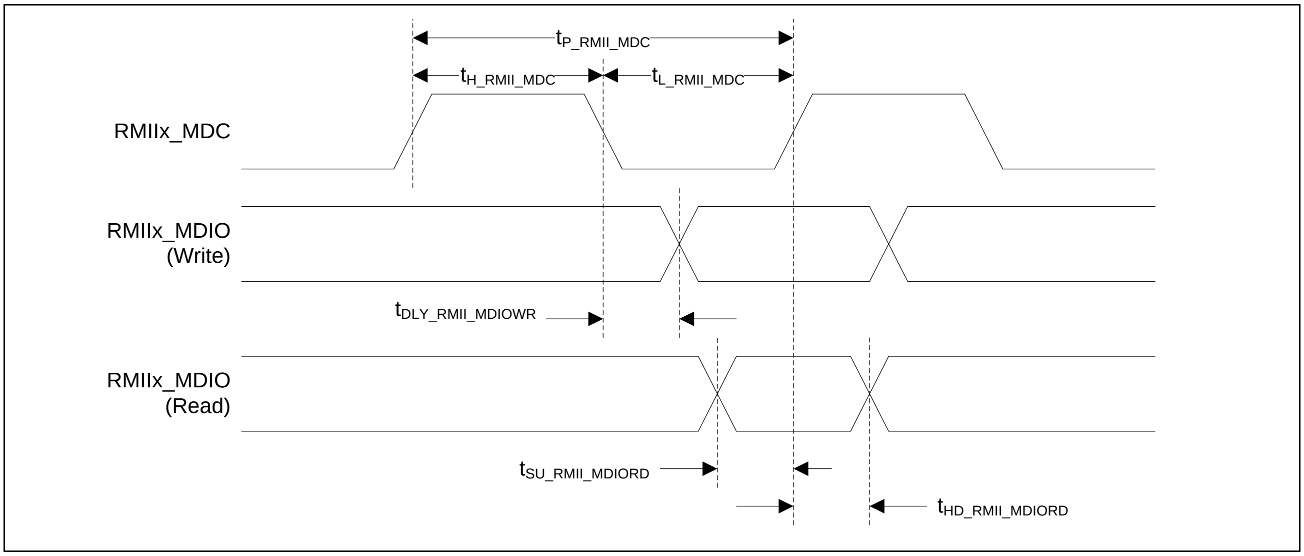


Figure 8-18 Ethernet PHY Management Interface Timing Diagram

8.6.7 NAND Dynamic Characteristics

8.6.7.1 *NAND Default Mode Dynamic Characteristics*

Symbol	Description	Min	Typ	Max	Unit	Test Condition
$t_{H\_nWE\_nRD}$	NAND_nWE and NAND_nRE High Time	-	20[*1]	-	ns	-
$t_{L\_nWE\_nRD}$	NAND_nWE and NAND_nRE Low Time	-	35[*2]	-	ns	-
$t_{DLY\_DATA\_OUT}$	NAND_nWE Falling to Valid NAND_DATA Delay	-	-	60[*3]	ns	-
$t_{HD\_DATA\_OUT}$	NAND_DATA Hold Time from NAND_nWE Rising	21[*3]	-	-	ns	-
$t_{SU\_DATA\_IN}$	NAND_DATA Setup Time to NAND_nRE Rising	16[*3]	-	-	ns	-
$t_{HD\_DATA\_IN}$	NAND_DATA Hold Time from NAND_nRE Rising	22[*3]	-	-	ns	-

Note:

1. NAND controller operating clock is 200 MHz and HI_WID (FMI_NANDTMCTL[15:8]) is 0x1.
2. NAND controller operating clock is 200 MHz and LO_WID (FMI_NANDTMCTL[7:0]) is 0x5.
3. NAND controller operating clock is 200 MHz.

Table 8.6-11 NAND Default Mode Dynamic Characteristics

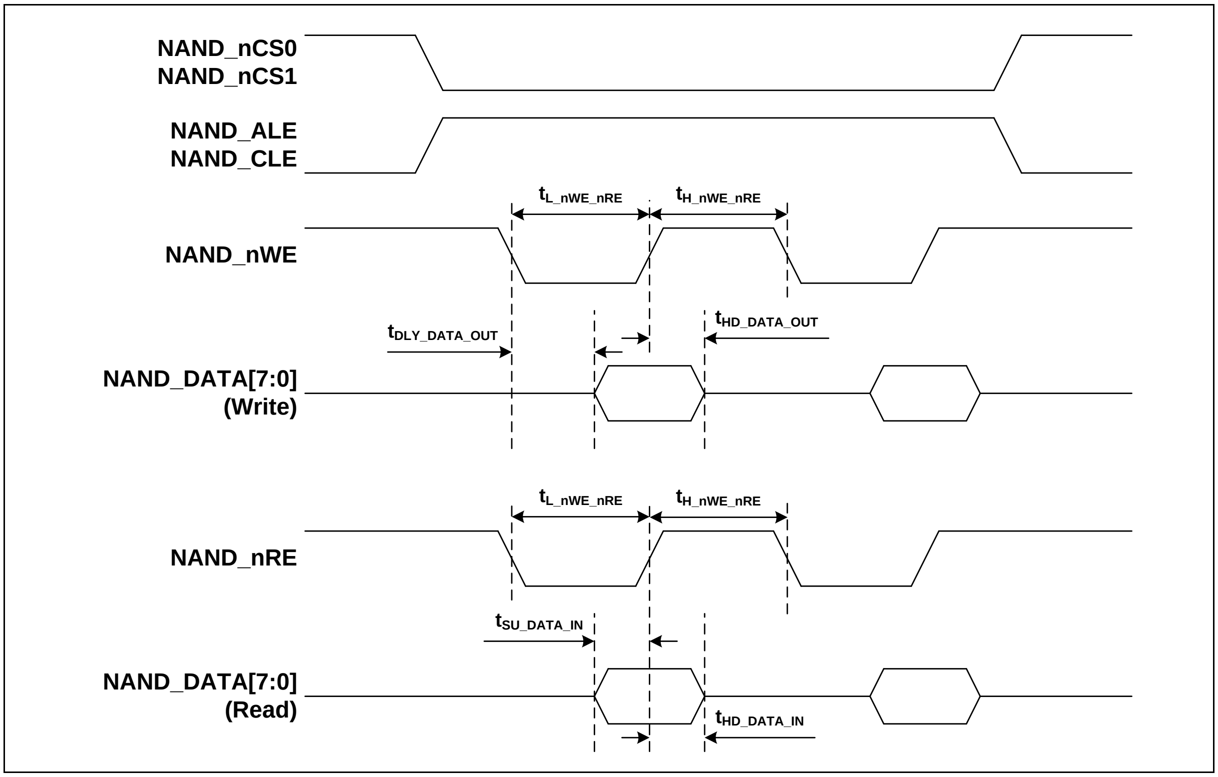


Figure 8-19 NAND Default Mode Timing Diagram

8.6.7.2 *NAND Read EDO Mode Dynamic Characteristics*

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
$t_{H\_nWE\_nRD}$	NAND_nWE and NAND_nRD High Time	-	20[*1]	-	ns	-
$t_{L\_nWE\_nRD}$	NAND_nWE and NAND_nRD Low Time	-	20[*2]	-	ns	-
$t_{DATA\_IN\_DLY}$	NAND_DATA Input Delay Time from NAND_nRE Rising	6.5[*3]	-	40[*3]	ns	-

Note:

1. NAND controller operating clock is 200 MHz and HI_WID (FMI_NANDTMCTL[15:8]) is 0x1.
2. NAND controller operating clock is 200 MHz and LO_WID (FMI_NANDTMCTL[7:0]) is 0x5.
3. NAND controller operating clock is 200 MHz.

Table 8.6-12 NAND Read EDO Mode Dynamic Characteristics

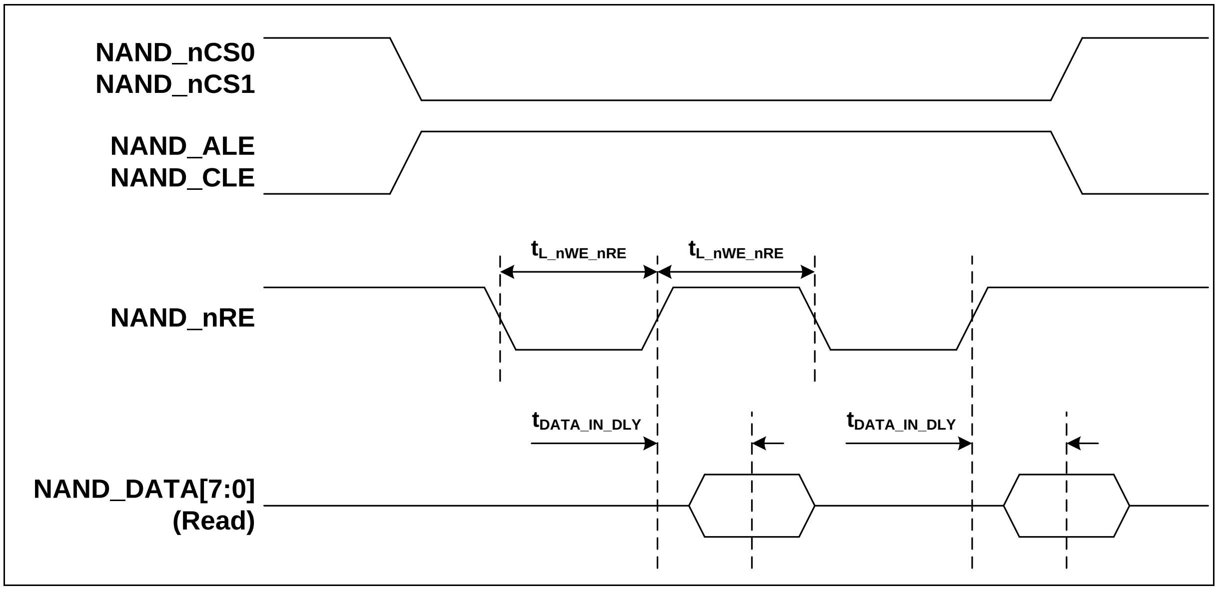


Figure 8-20 NAND Read EDO Mode Timing Diagram

8.6.8 SD/eMMC Dynamic Characteristics

8.6.8.1 *SD Default Mode Dynamic Characteristics*

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
$t_{P\_SD\_CLK}$	SD_CLK Period (Data Transfer Mode)	40	-	-	ns	-
$t_{P\_SD\_CLK\_ID}$	SD_CLK Period (Identification Mode)	2,500	-	-	ns	
$t_{H\_SD\_CLK}$	SD_CLK High Time	-	20	-	ns	-
$t_{L\_SD\_CLK}$	SD_CLK Low Time	-	20	-	ns	-
$t_{SU\_SD\_IN}$	SD_DATA Setup Time to SD_CLK Rising	5	-	-	ns	-
$t_{HD\_SD\_IN}$	SD_DATA Hold Time from SD_CLK Rising	5	-	-	ns	-
$t_{DLY\_SD\_OUT}$	SD_CLK Falling to Valid SD_DATA Delay	-	-	14	ns	-

Table 8.6-13 SD Default Mode Dynamic Characteristics

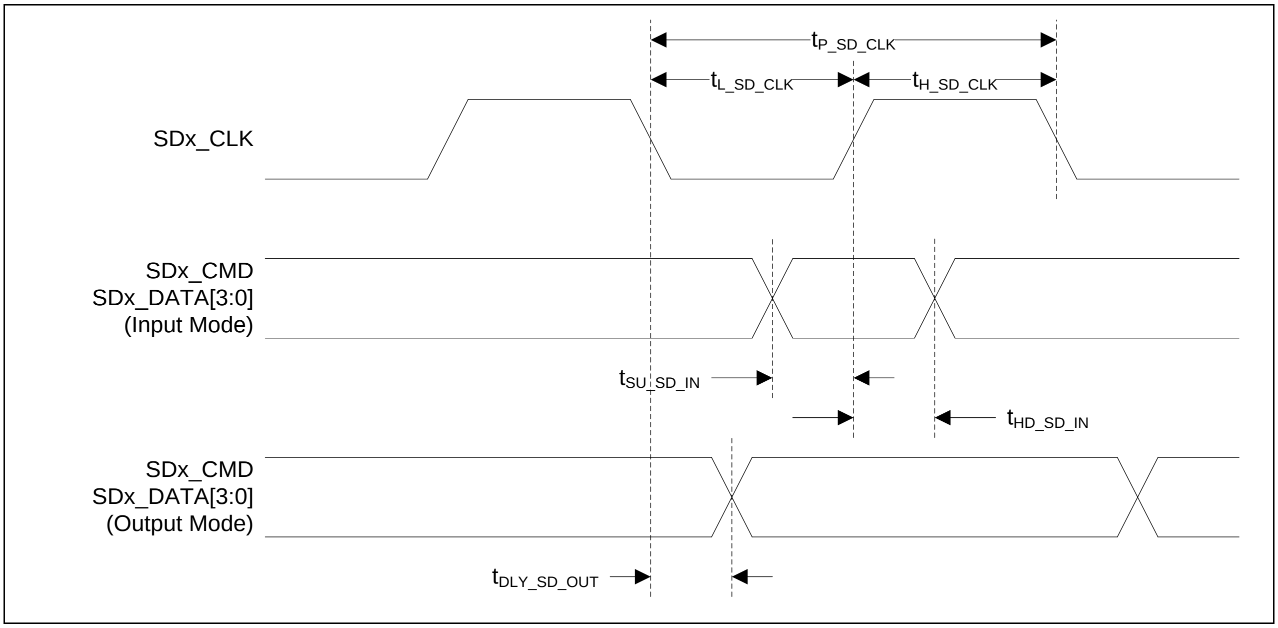


Figure 8-21 SD Default Mode Timing Diagram

8.6.8.2 *SD High-Speed Mode Dynamic Characteristics*

Symbol	Description	Min	Typ	Max	Unit	Test Condition
$t_{P\_SD\_CLK}$	SD_CLK Period	20	-	-	ns	-
$t_{H\_SD\_CLK}$	SD_CLK High Time	7	-	-	ns	-
$t_{L\_SD\_CLK}$	SD_CLK Low Time	7	-	-	ns	-
$t_{SU\_SD\_IN}$	SD_DATA Setup Time to SD_CLK Rising	6	-	-	ns	-
$t_{HD\_SD\_IN}$	SD_DATA Hold Time from SD_CLK Rising	2	-	-	ns	-
$t_{DLY\_SD\_OUT}$	SD_CLK Falling to Valid SD_DATA Delay	-	-	14	ns	-
$t_{HD\_SD\_OUT}$	SD_DATA Hold Time from SD_CLK Rising	2.5	-	-	ns	-

Table 8.6-14 SD High-Speed Mode Dynamic Characteristics

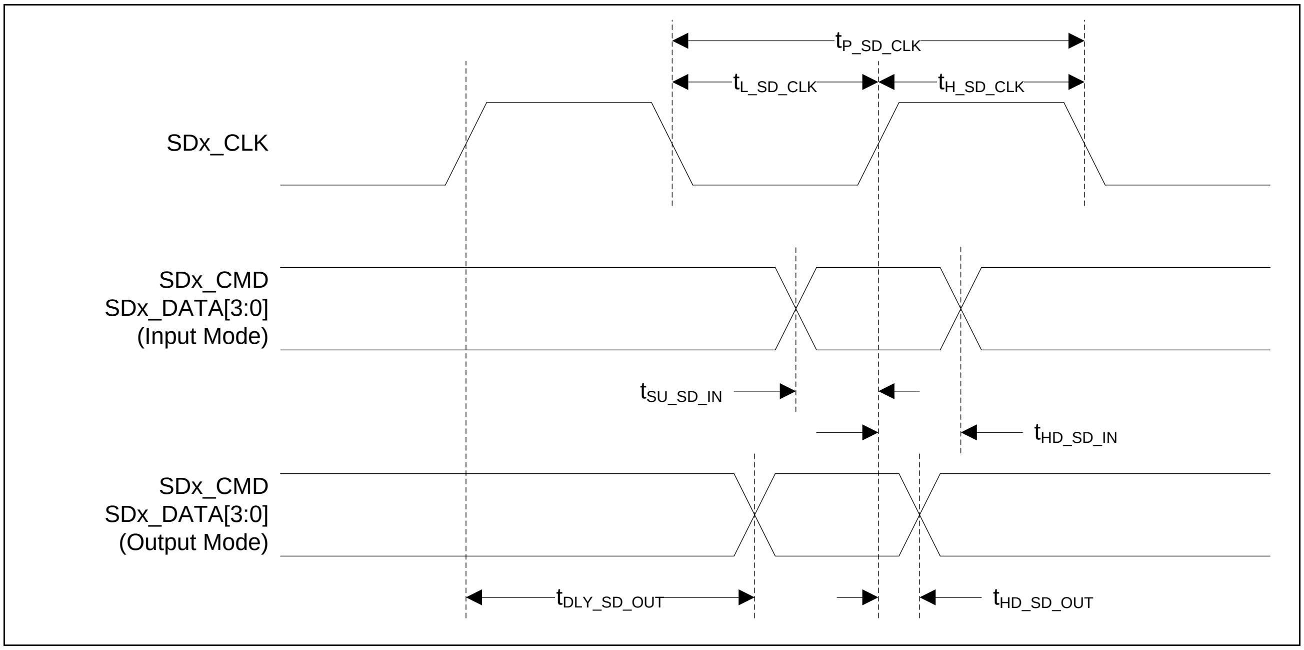


Figure 8-22 SD High-Speed Mode Timing Diagram

8.6.8.3 *SD3.0 SDR104 Mode Dynamic Characteristics*

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
$t_{P\_SD\_CLK}$	SD_CLK Period	4.807	-	-	ns	-
$t_{H\_SD\_CLK}$	SD_CLK High Time	1.44	-	-	ns	-
$t_{L\_SD\_CLK}$	SD_CLK Low Time	1.44	-	-	ns	-
$t_{SU\_SD\_IN}$	SD_DATA Setup Time to SD_CLK Rising	1.4	-	-	ns	-
$t_{HD\_SD\_IN}$	SD_DATA Hold Time from SD_CLK Rising	1	-	-	ns	-
$t_{DLY\_SD\_OUT}$	SD_CLK Falling to Valid SD_DATA Delay	-	-	9.7	ns	-
$T_{SD\_OUT\_W}$	Outupt Data Valid Window	2.8	-	-	ns	-

Table 8.6-15 SD3.0 SDR104 Mode Dynamic Characteristics

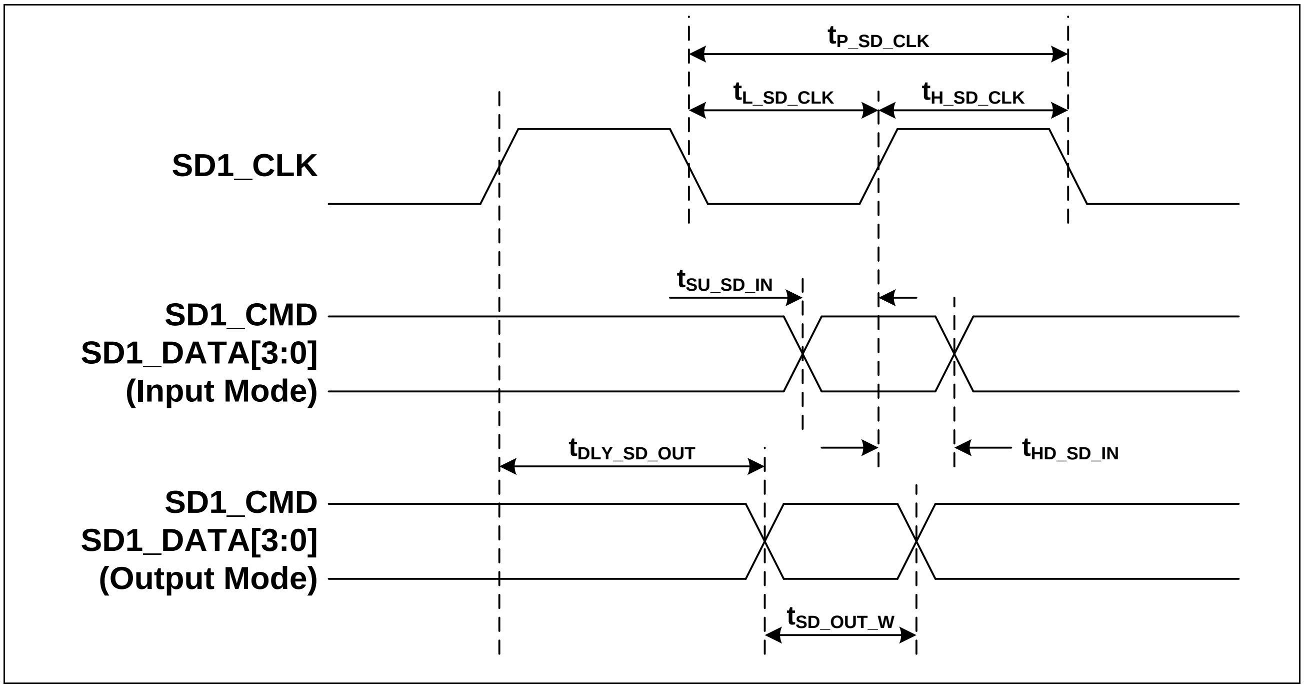


Figure 8-23 SD3.0 SDR104 Mode Timing Diagram

8.6.8.4 *eMMC HS200 Mode Dynamic Characteristics*

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
$t_{P\_eMMC\_CLK}$	eMMC_CLK Period	4.807	-	-	ns	-
$t_{H\_eMMC\_CLK}$	eMMC_CLK High Time	1.44	-	-	ns	-
$t_{L\_eMMC\_CLK}$	eMMC_CLK Low Time	1.44	-	-	ns	-
$t_{SU\_eMMC\_IN}$	eMMC_DATA Setup Time to eMMC_CLK Rising	1.4	-	-	ns	-
$t_{HD\_eMMC\_IN}$	eMMC_DATA Hold Time from eMMC_CLK Rising	1	-	-	ns	-
$t_{DLY\_eMMC\_OUT}$	eMMC_CLK Falling to Valid eMMC_DATA Delay	-	-	9.7	ns	-
$T_{eMMC\_OUT\_W}$	Outupt Data Valid Window	1.6	-	-	ns	-

Table 8.6-16 eMMC HS200 Mode Dynamic Characteristics

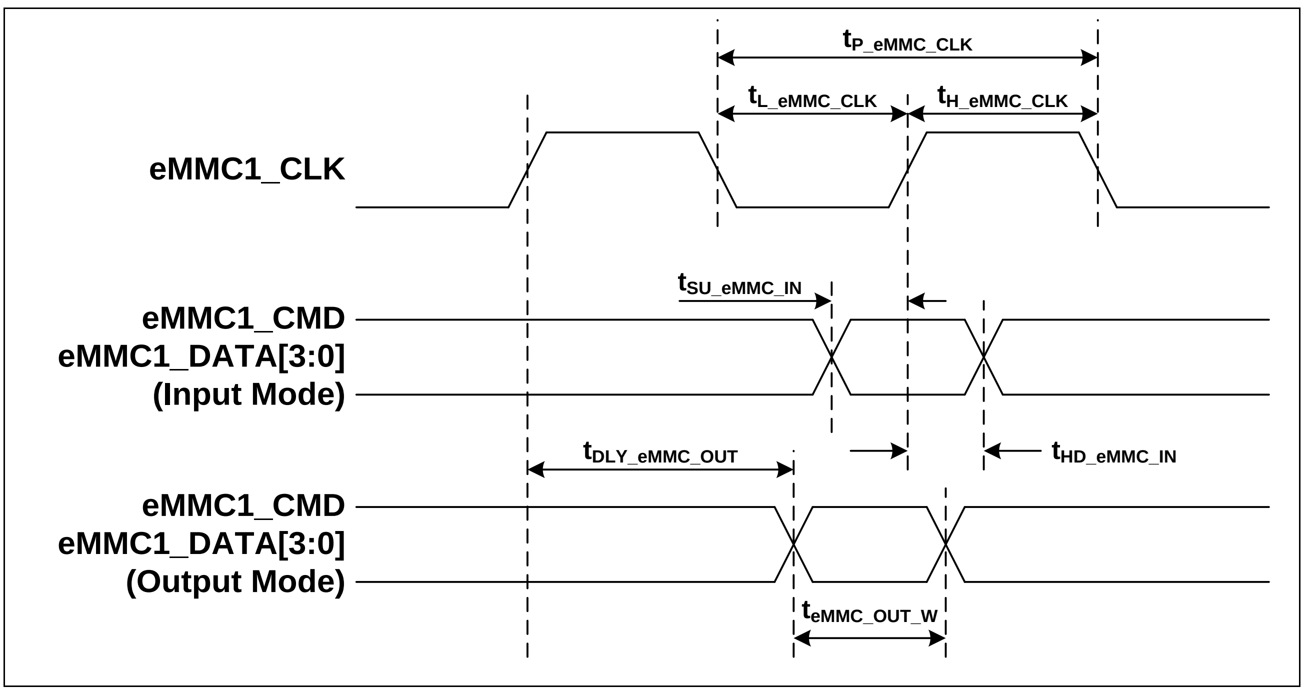


Figure 8-24 eMMC HS200 Mode Timing Diagram

8.6.9 CCAP Dynamic Characteristics

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
$t_{P\_CCAP\_PIXCLK}$	CCAP_PIXCLK Period	10.42	-	-	ns	-
$t_{H\_CCAP\_PIXCLK}$	CCAP_PIXCLK High Time	-	5.21	-	ns	-
$t_{L\_CCAP\_PIXCLK}$	CCAP_PIXCLK Low Time	-	5.21	-	ns	-
$t_{SU\_CCAP\_IN}$	CCAP_HSYNC, CCAP_VSYNC, CCAP_FIELD and CCAP_DATA Setup Time to CCAP_PIXCLK Rising	4.5	-	-	ns	-
$t_{HD\_CCAP\_IN}$	CCAP_HSYNC, CCAP_VSYNC, CCAP_FIELD and CCAP_DATA Hold Time from CCAP_PIXCLK Rising	2.5	-	-	ns	-

Table 8.6-17 CCAP Dynamic Characteristics

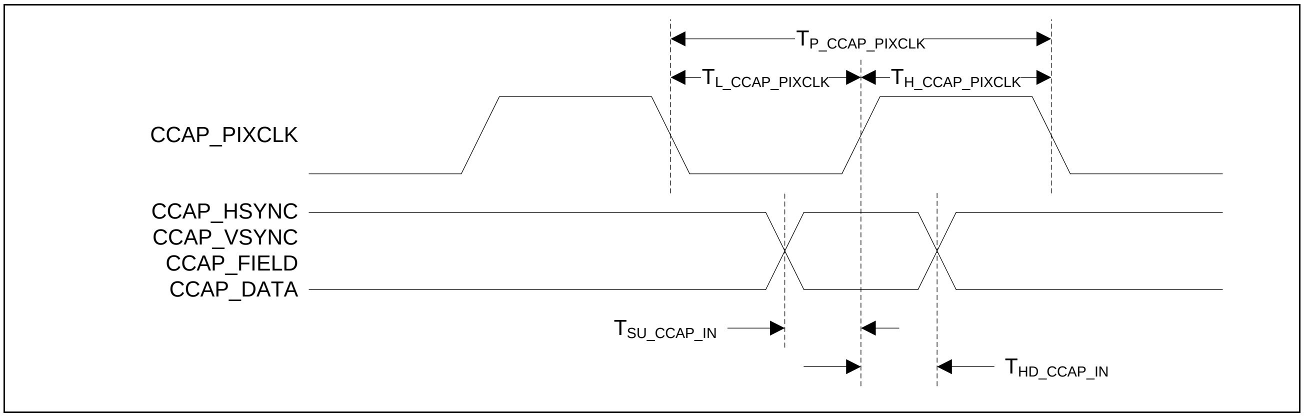


Figure 8-25 CCAP Timing Diagram

8.6.10 LCD Dynamic Characteristics

8.6.10.1 *LCD Sync Mode Dynamic Characteristics*

Symbol	Description	Min	Typ	Max	Unit	Test Condition
f_{LCM_CLK} $1/t_{LCM\_CLK}$	LCM_CLK Clock Frequency	-	-	150	MHz	-
t_{CLKH}	LCM_CLK Clock High Time	-	$t_{LCM\_CLK}/2$	-	ns	-
t_{CLKL}	LCM_CLK Clock Low Time	-	$t_{LCM\_CLK}/2$	-	ns	-
t_V	LCM_HSYNC, LCM_VSYNC, LCM_DEN and LCM_DATA[23:0] Output Valid Time	-	-	2.5	ns	-
t_H	LCM_HSYNC, LCM_VSYNC, LCM_DEN and LCM_DATA[23:0] Output Hold Time	0.5	-	-	ns	-

Table 8.6-18 LCD Sync Mode Dynamic Characteristics

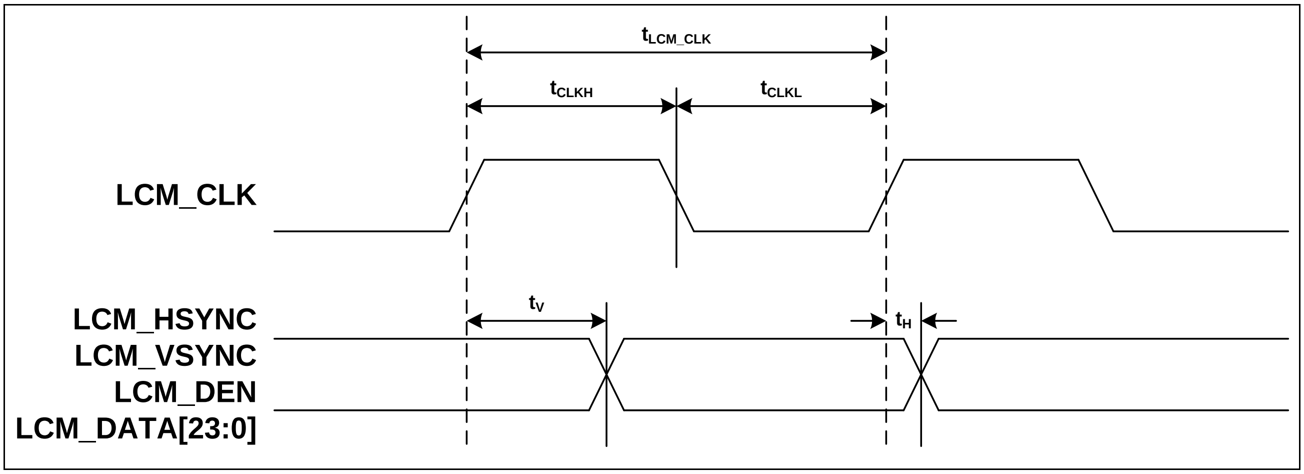


Figure 8-26 LCD Sync Mode Timing Diagram

8.6.10.2 *LCD MPU Mode I80 Dynamic Characteristics*

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
t_{LCM_I80WR}	MPU I80 Mode Write Period	3	-	1024	t_{LCM_CLK}[1]	
t_{I80WR_ACT}	MPU I80 Mode Write Active Cycle	1		1024	t_{LCM_CLK}[1]	
t_{I80WR_DEACT}	MPU I80 Mode Write De-Active Cycle	1	-	1024	t_{LCM_CLK}[1]	
t_{LCM_I80RD}	MPU I80 Mode Read Period	3	-	1024	t_{LCM_CLK}[1]	
t_{I80RD_ACT}	MPU I80 Mode Read Active Cycle	1		1024	t_{LCM_CLK}[1]	
t_{I80RD_DEACT}	MPU I80 Mode Read De-Active Cycle	1		1024	t_{LCM_CLK}[1]	
t_{DS}	MPU I80 Mode Read Data Setup Time	2	-	-	t_{LCM_CLK}[1]	
t_{DH}	MPU I80 Mode Read Data Hold Time	1	-	-	t_{LCM_CLK}[1]	

Table 8.6-19 LCD MPU I80 Mode Dynamic Characteristics

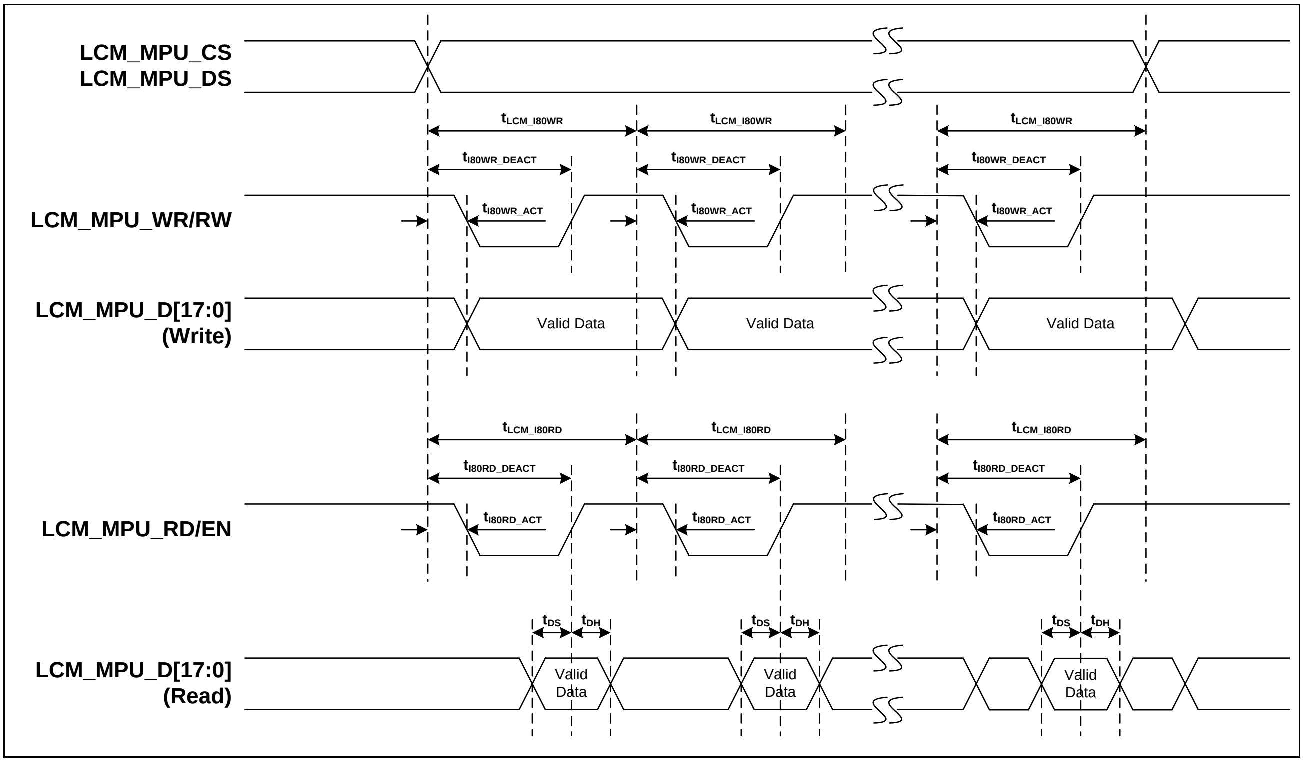


Figure 8-27 LCD MPU I80 Mode Timing Diagram

8.6.10.3 *LCD MPU Mode M68 Dynamic Characteristics*

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
$t_{LCM\_M68WREN}$	MPU M68 Mode Write Data Enable Period	3	-	1024	t_{LCM_CLK}[1]	
$t_{M68WREN\_ACT}$	MPU M68 Mode Write Data Enable Active Cycle	1	-	1024	t_{LCM_CLK}[1]	
$t_{M68WREN\_DEACT}$	MPU M68 Mode Write Data Enable De-Active Cycle	1	-	1024	t_{LCM_CLK}[1]	
$t_{LCM\_M68RDEN}$	MPU M68 Mode Read Data Enable Period	3	-	1024	t_{LCM_CLK}[1]	
$t_{M68RDEN\_ACT}$	MPU M68 Mode Read Data Enable Active Cycle	1	-	1024	t_{LCM_CLK}[1]	
$t_{M68RDEN\_DEACT}$	MPU M68 Mode Read Data Enable De-Active Cycle	1	-	1024	t_{LCM_CLK}[1]	
t_{DS}	MPU M68 Mode Read Data Setup Time	2	-	-	t_{LCM_CLK}[1]	
t_{DH}	MPU M68 Mode Read Data Hold Time	1	-	-	t_{LCM_CLK}[1]	

Table 8.6-20 LCD MPU M68 Mode Dynamic Characteristics

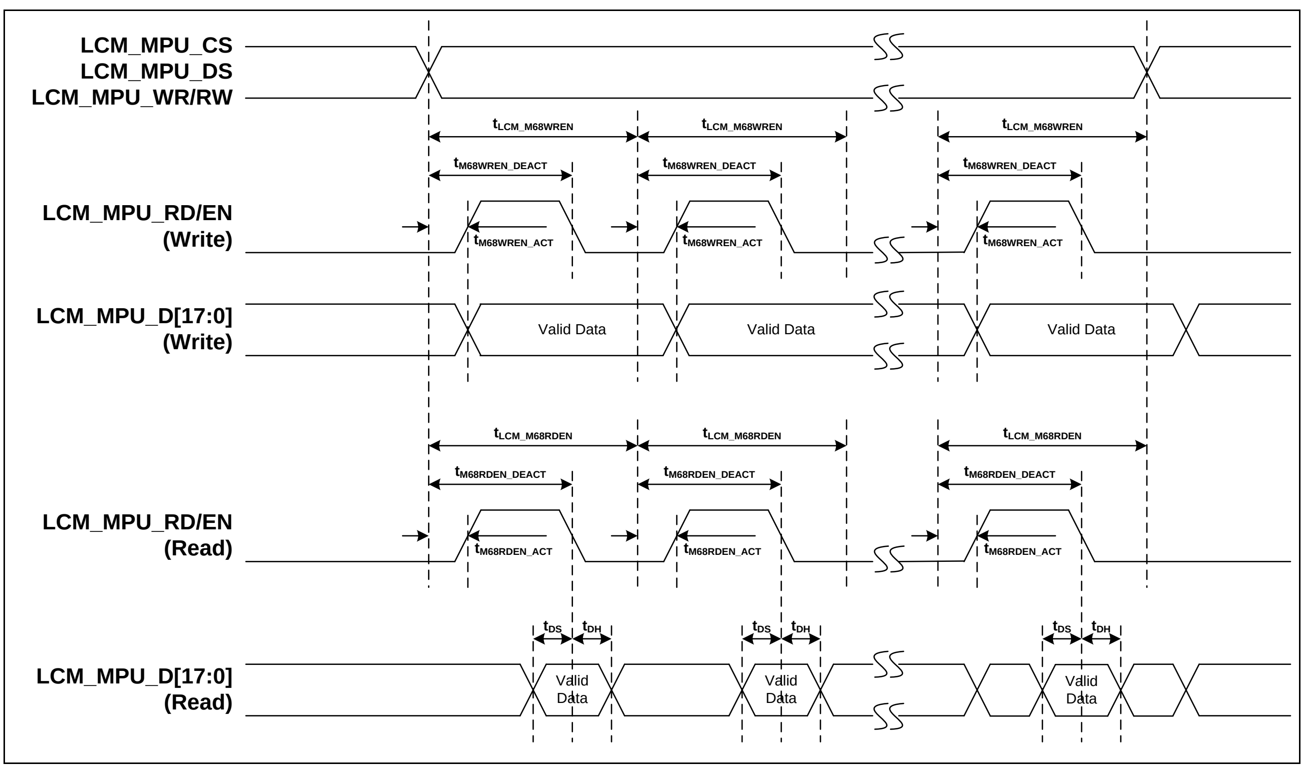


Figure 8-28 LCD MPU M68 Mode Timing Diagram

8.7 OTP Memory DC Characteristics

Symbol	Description	Min	Typ	Max	Unit	Test Conditions
I_{VDD_OTP} [*1]	OTP Consumption On V_{DD_OTP}	-	8	15	mA	Programming
		-	0.7	1.5	mA	Reading
		-	5	25	uA	Standby

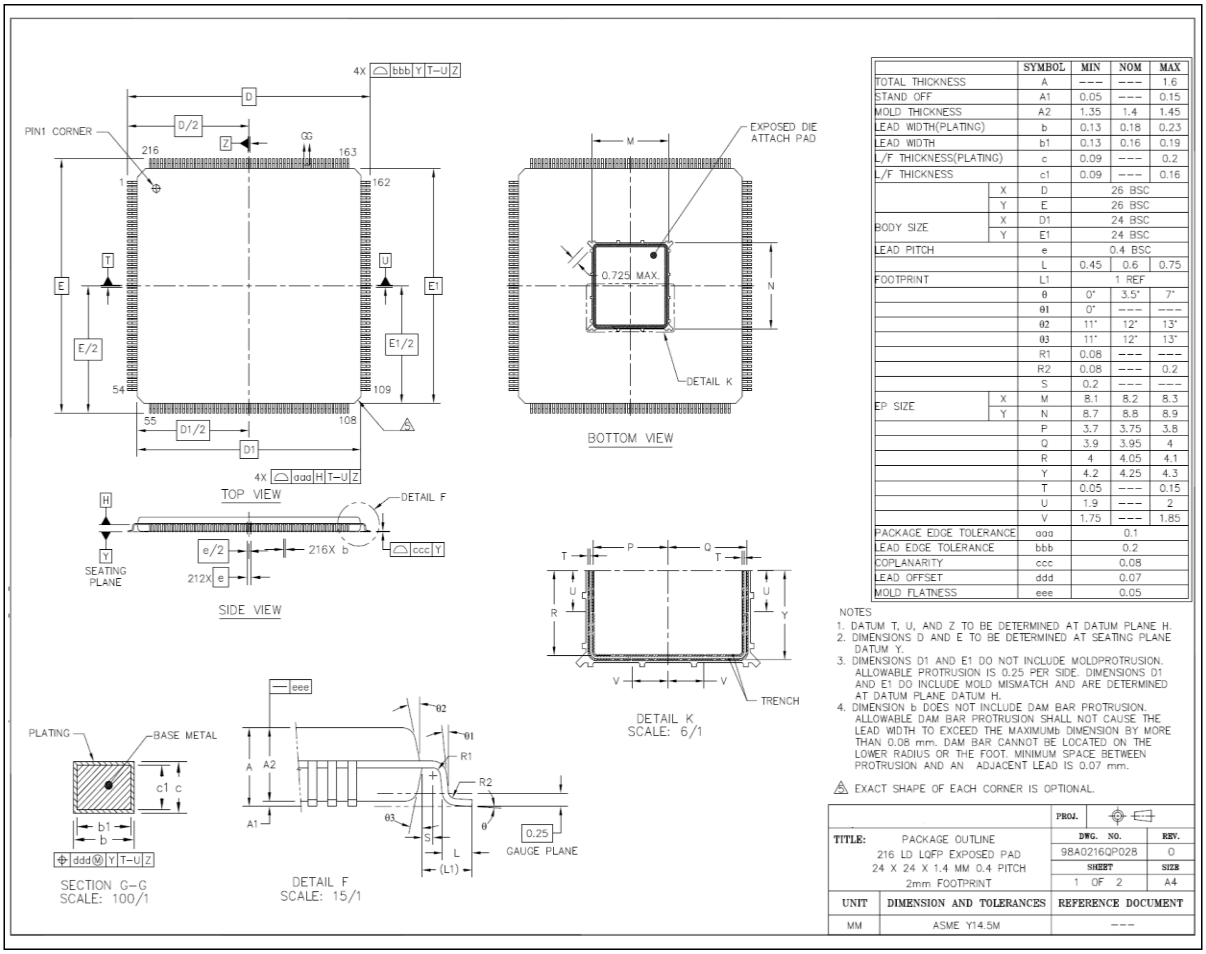
Note:

1.Guaranteed by design, not tested in production.

9 PACKAGE DIMENSIONS

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

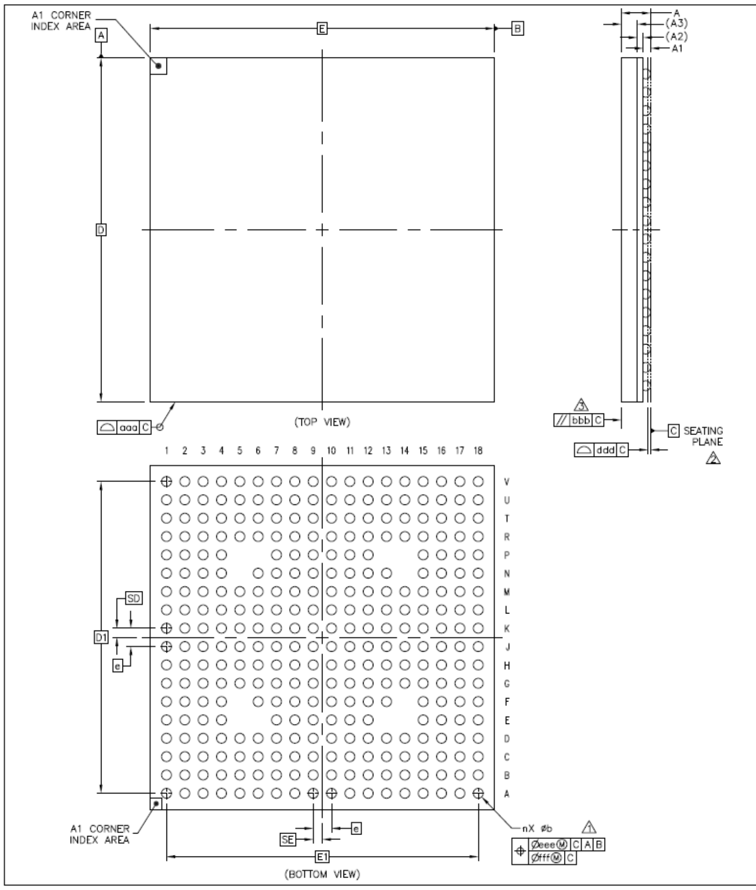
9.1 LQFP-EP 216-Pin (24x24x1.4mm, footprint 2.0mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
	X	D	26 BSC		
	Y	E	26 BSC		
BODY SIZE	X	D1	24 BSC		
	Y	E1	24 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
EP SIZE	X	M	8.1	8.2	8.3
	Y	N	8.7	8.8	8.9
		P	3.7	3.75	3.8
		Q	3.9	3.95	4
		R	4	4.05	4.1
		Y	4.2	4.25	4.3
		T	0.05	---	0.15
		U	1.9	---	2
		V	1.75	---	1.85
PACKAGE EDGE TOLERANCE		aaa	0.1		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

Figure 9-1 LQFP-EP 216-Pin Package Demension

9.2 BGA 312-Ball (15x15x1.4mm, 0.8mm pitch)



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.4
STAND OFF	A1	0.27	---	0.37
SUBSTRATE THICKNESS	A2		0.26	REF
MOLD THICKNESS	A3		0.7	REF
BODY SIZE	D		15	BSC
	E		15	BSC
BALL DIAMETER			0.4	
BALL OPENING			0.35	
BALL WIDTH	b	0.38	---	0.48
BALL PITCH	e		0.8	BSC
BALL COUNT	n		312	
EDGE BALL CENTER TO CENTER	D1		13.6	BSC
	E1		13.6	BSC
BODY CENTER TO CONTACT BALL	SD		0.4	BSC
	SE		0.4	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.12	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

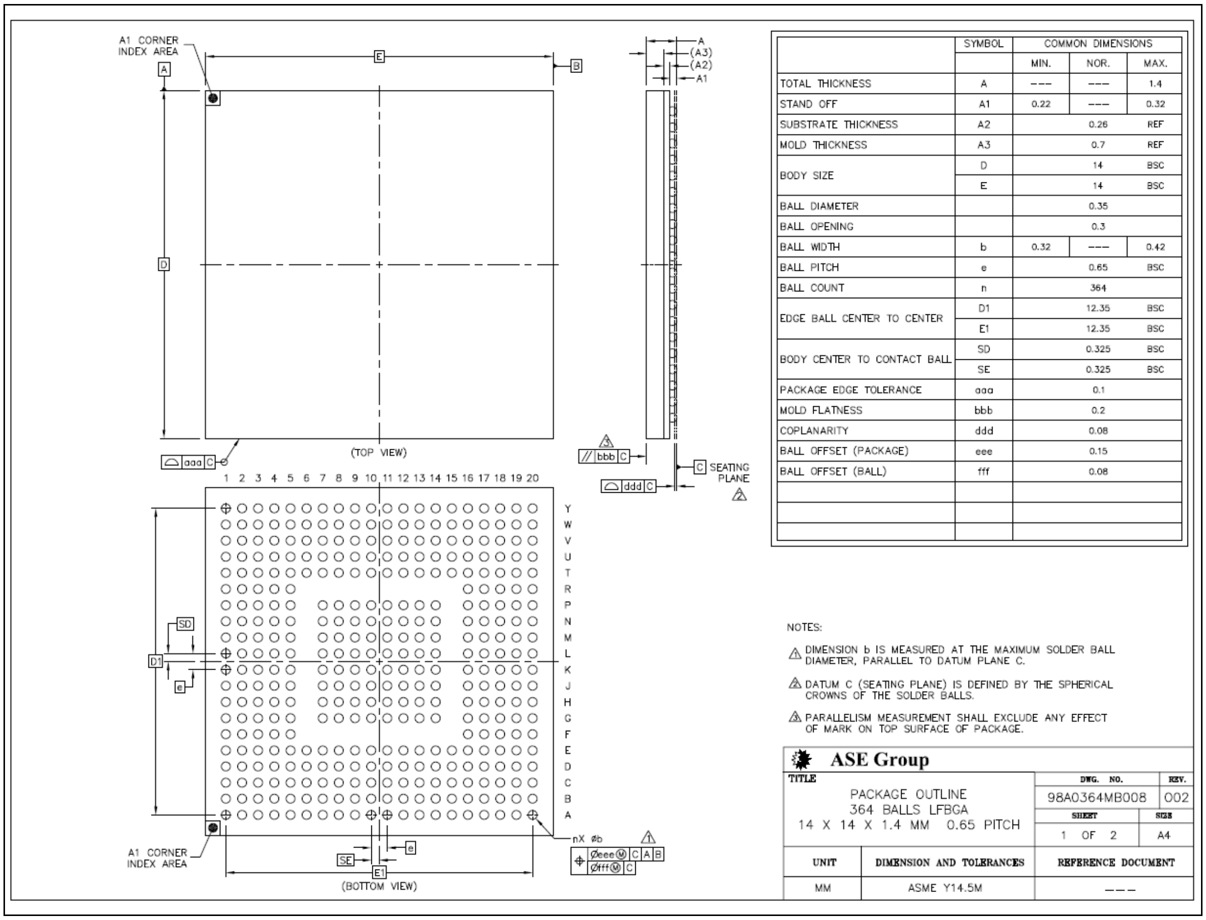
ASE Group

TITLE	DWG. NO.	REV.
PACKAGE OUTLINE 312 BALLS LFBGA 15 X 15 X 1.4 MM 0.8 PITCH	98A0312MB004	002
	SHEET: 1 OF 2	SIZE: A4

UNIT	DIMENSION AND TOLERANCES	REFERENCE DOCUMENT
MM	ASME Y14.5M	---

Figure 9-2 BGA 312-Ball Package Demension

9.3 BGA 364-Ball (14x14x1.4mm, 0.65mm pitch)



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.4
STAND OFF	A1	0.22	---	0.32
SUBSTRATE THICKNESS	A2		0.26	REF
MOLD THICKNESS	A3		0.7	REF
BODY SIZE	D		14	BSC
	E		14	BSC
BALL DIAMETER			0.35	
BALL OPENING			0.3	
BALL WIDTH	b	0.32	---	0.42
BALL PITCH	e		0.65	BSC
BALL COUNT	n		364	
EDGE BALL CENTER TO CENTER	D1		12.35	BSC
	E1		12.35	BSC
BODY CENTER TO CONTACT BALL	SD		0.325	BSC
	SE		0.325	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

Figure 9-3 BGA 364-Ball Package Demension

9.4 Thermal Characteristics

9.4.1 Thermal Performance of Package under Forced Convection

PKG type	PCB condition	θ ja (°C/W)			Psi JT (°C/W)	θ jc (°C/W)	θ jb (°C/W)
		0 m/s	1 m/s	2m/s			
LQFP-EP 216-Pin 24x24 - Ambient	JEDEC JESD 51-7, 2S2P	17.6	13.50	12.40	0.41	7.10	10.03
LFBGA 312-Ball 15x15 - Ambient	JEDEC JESD 51-9, 2S2P	21.70	18.40	17.40	0.29	6.10	10.22
LFBGA 364-Ball 14x14 - Ambient	JEDEC JESD 51-9, 2S2P	25.10	22.20	21.10	0.37	8.60	13.82

Table 9.4-1 Thermal Performance of Package

9.4.2 Thermal Performance Terminology

The major thermal dissipation paths can be illustrated as following

T_J: the maximum junction temperature;

T_A: the ambient or environment temperature;

T_C: the top center of compound surface temperature;

T_B: the bottom center of PCB surface temperature;

P: total input power

1. Junction to ambient thermal resistance, θ_{JA}, **defined as:**

$$\theta_{JA} = \frac{T_J - T_A}{P} \; ; \qquad (1)$$

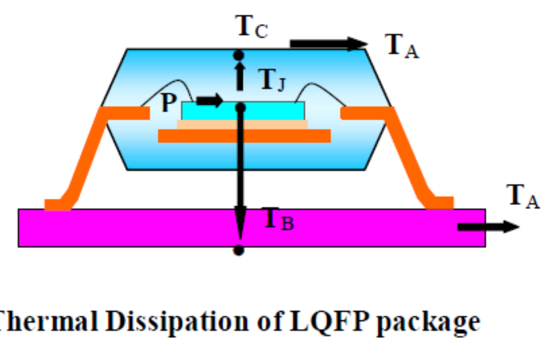


Figure 9-4 Junction to Ambient Thermal Resistance

2. Junction to case thermal resistance, θ_{JC}, **defined as:**

$$\theta_{JC} = \frac{T_J - T_C}{P} \; ; \qquad (2)$$

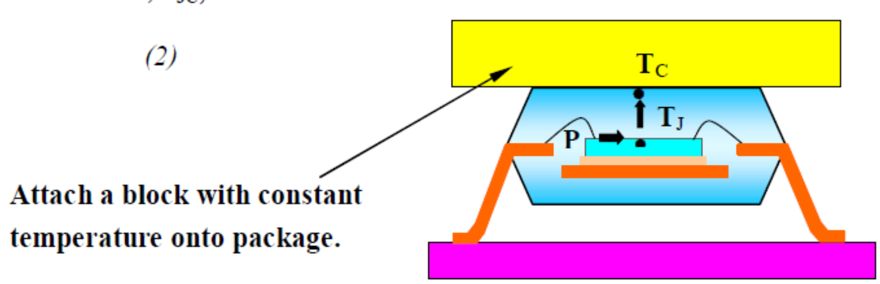


Figure 9-5 Junction to Case Thermal Resistance

9.4.3 Simulation Conditions

Input Power	**Main Die: 1.5W** **DRAM Die: 0.5 W**
Test Board (PCB)	FR4 PCB thickness is 1.6mm Copper thickness is 2-OZ for Microstrip (Top/Bottom) layer Copper thickness is 1-OZ for stripline (Inner) layer LQFP216 follows JESD 51-7, 2S2P PCB is size 3”x 4.5” BGA follows JESD 51-9, 2S2P PCB size is 4”x 4.5”
Control Condition	Air Flow = 0, 1, 2, 3 m/s

Table 9.4-2 Thermal Characteristics Simulation Conditions

9.5 PCB Reflow Profile Suggestion

9.5.1 Profile Setting Consideration

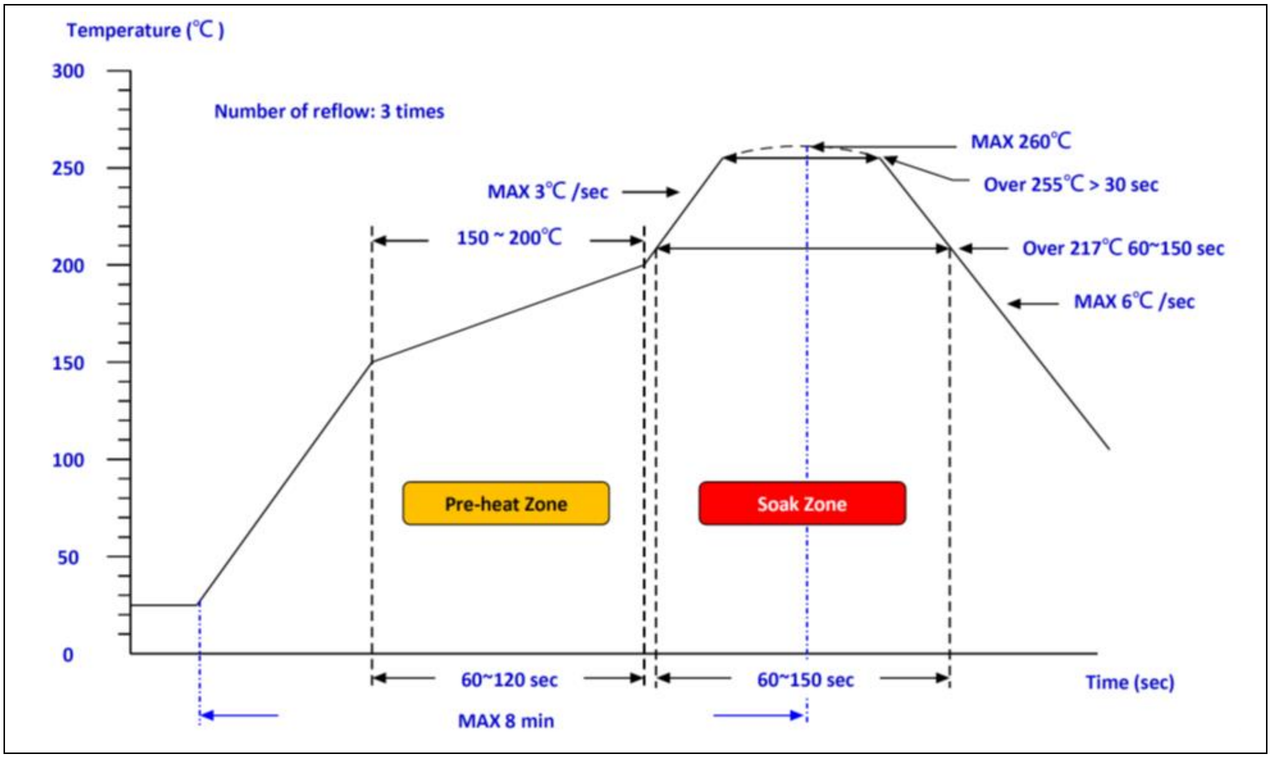


Figure 9-6 PCB Reflow Profile Diagram

Profile Feature	Sn-Pb Eutestic Assembly		Pb-Free Eutestic Assembly	
	Large Body	Small Body	Large Body	Small Body
Average ramp-up rate (T_L to T_P)	< 3°C/second		< 3°C/second	
Preheat • Temperature Min (Ts_{min}) • Temperature Max (Ts_{max}) • Time (min to max) (ts)	100°C 150°C 60-120 seconds		150°C 200°C 60-120 seconds	
Time maintained above: • Temperature (T_L) • Time (t_L)	183°C 60-150 seconds		217°C 60-150 seconds	
Peak Temperature (T_p)	225+0/-5°C		245+5/-5°C	
Time within 5°C of actual Peak Temperature (t_p)	10-20 seconds		10-30 seconds	
Ramp-down Rate	6°C/second max.		6°C/second max.	
Time 25°C to Peak Temperature	6 minutes max.		8 minutes max.	
Note:				

1. All temperatures refer to topside of the package, measured on the package body surface. 2. Depends on other parts on board density and follower solder paste manufacturer’s guideline.

Table 9.5-1 PCB Reflow Profile Parameters

9.5.2 Profile Suggestion

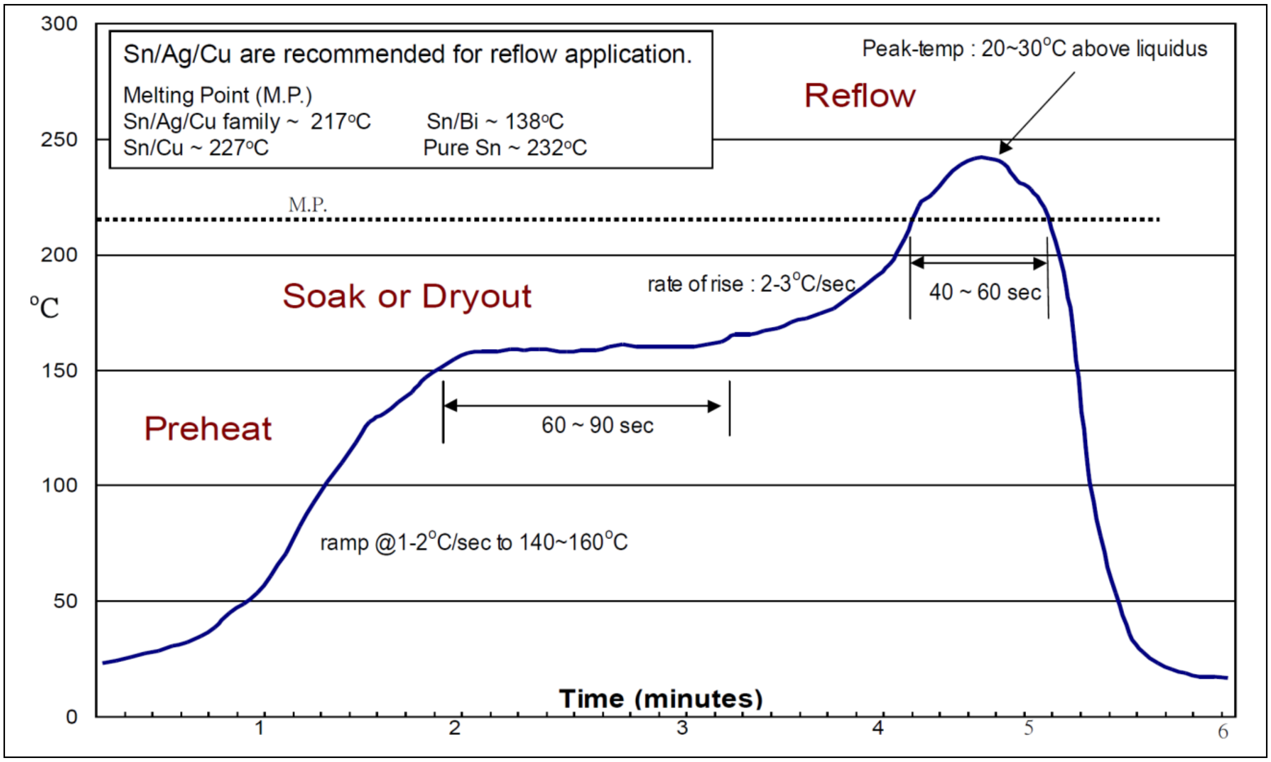


Figure 9-7 Profile Suggestion for MA35D1 Series

9.5.3 PCB Assembly Considerations

This profile is designed for use with 96.5Sn/3Ag/0.5Cu and can serve as a general guideline in establishing a reflow profile.

Reflow Profile:

- Heating-up@1~3°C/sec to 140°C
- Preheat@140-150°C for 120~160 sec
- Ramp@2~3 °C/sec to peak temperature (220 ~ 225°C), temperature over 183°C for 45~75 sec
- Cooling down to room temperature@4~2°C/sec to avoid undesired intermetallic compound layer.

9.6 PKG Baking and Vacuumed

The moisture-sensitivity caution label (Figure 9-8) is applied to the outside of the sealed moisture-barrier bag. This label contains detailed information specific to the device (moisture-sensitivity level, shelf life, etc.).

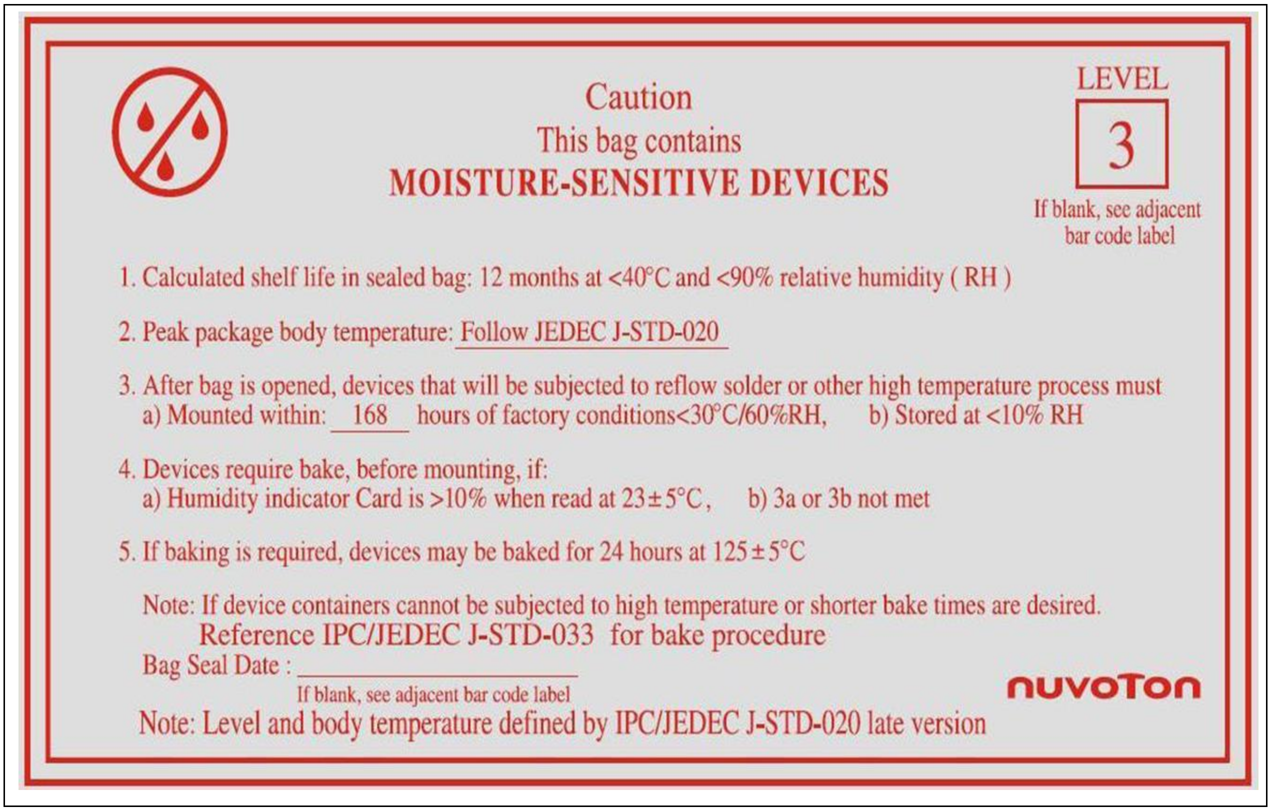


Figure 9-8 Cautions for PKG Baking

10 ABBREVIATIONS

10.1 Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
AIC	Advanced Interrupt Controller
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
AMBA	Advanced Microcontroller Bus Architecture
BCH	Bose–Chaudhuri–Hocquenghem
BPS	Bit Per Second
CAN	Controller Area Network
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
DDR	Double Data Rate
DDR2	Double Data Rate 2
DMA	Direct Memory Access
EBI	External Bus Interface
ECC	Elliptic Curve Cryptography
ECC	Error Correcting code
EHCI	Enhance Host Controller Interface
EINT	External Interrupt pin
EMAC	Ethernet MAC Controller
eMMC	Embedded Multimedia Card
ETU	Elementary time unit
FIFO	First In, First Out
FIQ	Fast Interrupt
FMI	Flash Memory Interface
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HMAC	keyed-Hash Message Authentication Code
HSUSBD	High Speed USB 2.0 Device Controller
HXT	12 MHz External High Speed Crystal Oscillator
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound

LIN	Local Interconnect Network
LPDDR	Low Power DDR
LSB	Least Significant Bit
LVD	Low Voltage Detect
LVR	Low Voltage Reset
LXT	32.748 kHz External Low Speed Crystal Oscillator
MLC	Multi-Level Cell NAND Flash
MMU	Memory Management Unit
MSB	Most Significant Bit
OHCI	Open Host Controller Interface
PCLK	The Clock of Advanced Peripheral Bus
PCM	Pulse Code Modulation
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PMBus	Power Management Bus
PRNG	Pseudo Random Number Generator
PWM	Pulse Width Modulation
RMII	Reduced Media Independent Interface
RSA	Rivest、Shamir and Adleman Cryptography
RTC	Real Time Clock
SC	Smart Card
SD	Secure Digital
SDHC	Secure Digital High Capacity
SDIC	SDRAM Interface Controller
SDIO	Secure Digital Input Output
SDR	Single Data Rate
SHA	Secure Hash Algorithm
SLC	Single Level Cell NAND Flash
SMBus	System Management Bus
SPI	Serial Peripheral Interface
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

WDT	Watchdog Timer
WWDT	Window Watchdog Timer

11 REVISION HISTORY

Date	Revision	Description
2022.10.5	1.00	Initial version.

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.