NuMicro® Family

1T 8051-based Microcontroller

MUG51TB9AE
Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1 GENERAL DESCRIPTION

MUG51TB9AE is a Flash embedded 1T 8051-based low-power microcontroller. It runs up to 7.3728 MHz with 16 Kbytes embedded Flash memory, 1 Kbytes embedded SRAM, 4 Kbytes Flash loader memory (LDROM), 1.8V ~ 5.5V operating voltage, and -40°C ~105°C operating temperature. MUG51TB9AE supports enhanced low current consumption at 200 μA while CPU power-on before Flash memory is initialized. Its low-power feature makes it suitable for battery-free device which harvests power from the magnetic field of coil such as stylus pen powered by EMR (Electro-magnetic Resonance) technology and RFID card.

The MUG51TB9AE features low current consumption at 200 μA while CPU power-on before Flash memory is initialized. It is suitable for battery-free devices such as stylus pen powered by EMR (Electro-magnetic Resonance) technology and RFID card. The current consumption is less than 1.3 mA in normal run mode at 7.3728 MHz, and less than 1 μA in Power-down mode.

The MUG51TB9AE provides rich peripherals including 24 general purpose I/Os with internal inverter, four 16-bit Timers/Counters, 2 sets of UARTs with frame error detection and automatic address recognition, 1 set of ISO7816 Smartcard interface, 1 set of SPI, 2 sets of I^2C, 6 enhanced PWM output channels with dead zone control, 2 sets of analog comparators, eight-channel shared pin interrupt for all I/O ports, low voltage reset (LVR) and brown-out detector (BOD) to enhance product performance, reduce external components and form factor simultaneously.

The MUG51TB9AE includes the QFN33 (4mm x 4mm) package.

1.1 Key Features and Application

Product Line	UART	ISO 7816-3	I^2C	SPI	Timer	PWM	PDMA	ACMP
MUG51TB9AE	2	1	2	1	4	6	2	2

Table 1.1-1 MUG51TB9AE Key Features Support Table

The MUG51TB9AE is suitable for a wide range of applications such as:

- Stylus pen
- RFID card

2 FEATURES

Core and System	
8051	• Fully static design 8-bit high performance 1T 8051-based CMOS microcontroller • Instruction set fully compatible with MCS-51 • 4-priority-level interrupts capability • Dual Data Pointers (DPTRs)
Power on Reset (POR)	• POR with 1.55V threshold voltage level
Brown-out Detector (BOD)	• 7-level selection, with brown-out interrupt and reset option. (4.4V / 3.7V / 3.0V / 2.7V / 2.4V / 2.0V / 1.8V)
Low Voltage Reset (LVR)	• LVR with 1.7V threshold voltage level
Security	• 96-bit Unique ID (UID) • 128-bit Unique Customer ID (UCID) • 128-bytes security protection memory SPROM
Memories	
Flash	• Up to 16 Kbytes of APROM for User Code • 4/3/2/1 Kbytes of Flash for loader (LDROM) configure from APROM for In-System-Programmable (ISP) • Flash Memory accumulated with pages of 128 Bytes from APROM by In-Application-Programmable (IAP) means whole APROM can be use as Data Flash • An additional 128 bytes security protection memory SPROM • Code lock for security by CONFIG
SRAM	• 256 Bytes on-chip RAM • Additional 1 Kbyte on-chip auxiliary RAM (XRAM) accessed by MOVX instruction
PDMA	• Three modes: peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer • Source address and destination address must be word alignment in all modes. • Memory-to-memory mode: transfer length must be word alignment.

Clocks	
Internal Clock Source	• Default 7.3728 MHz median speed internal oscillator (MIRC) trimmed to ±1% (accuracy at 25 ˚C, 3.3 V), ±2% in 0~70˚C • 38.4 kHz low-speed internal oscillator (LIRC) calibrating to ±2% by software from median speed internal oscillator
Timers	
16-bit Timer	• Two 16-bit Timers/Counters 0 and 1 compatible with standard 8051 • One 16-bit Timer 2 with three-channel input capture module with GPIO or ACMP output as input source select • One 16-bit auto-reload Timer 3, which can be the baud rate clock source of UARTs
Watchdog	• 6-bit free running up counter for WDT time-out interval • Selectable time-out interval is 1.66 ms ~ 3413.12 ms since WDT_CLK = 38.4 kHz (LIRC) • Able to wake up from Power-down or Idle mode • Interrupt or reset selectable on watchdog time-out
Wake-up Timer	• 16-bit free running up counter for time-out interval • Clock sources from LIRC • Able self Wake-up wake up from Power-down or Idle mode, and auto reload count value • Supports Interrupt
PWM	• Up to 6 output pins can be selected • Supports maximum clock source frequency up to F_{SYS} • Supports up to three PWM modules; each module provides 6 output channels • Supports independent mode for PWM output • Supports complementary mode for 3 complementary paired PWM output channels • Dead-time insertion with 8-bit resolution • Supports 16-bit resolution PWM counter • Supports mask function and tri-state enable for each PWM pin • Supports brake function
Analog Interfaces	
Analog Comparator (ACMP)	• Supports up to two comparators: ACMP0, ACMP1 • Supports hysteresis function

	• Supports wake-up function • Supports Comparator Reference Voltage (CRV) • Selectable input sources of negative input • 4 positive sources from pins • 4 negative sources include pin, bandgap voltage, and CRV
Communication Interfaces	
UART	• Supports up to two UARTs: UART0, UART1 • Supports 1 Smart Card configuration as UART function as UART2 • UART baud rate clock from MIRC • Full-duplex asynchronous communications • Programmable 9th bit • TXD and RXD pins of UART0 exchangeable via software
I²C	• Two sets of I²C devices • Master/Slave mode • Bidirectional data transfer between masters and slaves • Multi-master bus (no central master) • 7-bit addressing mode • Standard mode (100 kbps) and Fast mode (400 kbps) • Supports 8-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows • Multiple address recognition (four slave addresses with mask option) • Supports hold time programmable
SPI	• One set of SPI device • Supports Master or Slave mode operation • Supports MSB first or LSB first transfer sequence • Slave mode up to 4 MHz
ISO 7816-3	• One set of ISO 7816-3 device • Supports ISO 7816-3 compliant T=0, T=1 • Supports full-duplex UART mode
GPIO	• Four I/O modes: – Quasi-bidirectional mode – Push-Pull Output mode – Open-Drain Output mode

	– Input only with high impendence mode • Schmitt trigger input / TTL mode selectable • Supports internal inverter and buffer • Each I/O pin configured as interrupt source with edge/level trigger setting • Standard interrupt pins INT0 and INT1 • Supports high drive and high sink current I/O • I/O pin internal pull-up or pull-down resistor enabled in input mode • Maximum I/O speed is F_{SYS} • Enabling the pin interrupt function will also enable the wake-up function • Supports 5V-tolerance function
ESD & EFT	
ESD	• HBM ± 7 kV
EFT	• > ± 4.4 kV
Latch-up	• 150 mA

3 PART INFORMATION

3.1 MUG51TB9AE Package Type

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

Part No.	QFN33 (4x4mm)
MUG51TB9AE	MUG51TB9AE

3.2 MUG51TB9AE Naming Rule

MUG	51	T	B	9	A	E
Core	**Line**	**Package**	**Flash**	**SRAM**	**Reserve**	**Temperature**
1T 8051 Ultra Low power	51: Base	B: MSOP10 (3x3 mm) D: TSSOP14 (4.4x5.0 mm) E: TSSOP28 (4.4x9.7 mm) F: TSSOP20 (4.4x6.5 mm) L: LQFP48 (7x7 mm) M: LQFP44(10x10 mm) O: SOP20 (300 mil) P: LQFP32 (7x7 mm) S: LQFP64 (7x7 mm) T: QFN33 (4x4 mm) U: SOP28 (300 mil) X: QFN20 (3x3mm)	A: 8 KB B: 16 KB C: 32 KB D: 64 KB	0: 2 KB 1: 4 KB 2: 8/12 KB 3: 16 KB 6: 32 KB 8: 64 KB 9: 1 KB A: 96 KB		E:-40°C ~ 105°C

3.3 MUG51TB9AE Selection Guide

Part Number		MUG51TB9AE
		TB9AE
Flash (KB)		16
SRAM (KB)		1
LDROM (KB)		4
SPROM (Bytes)		128
System Frequency (MHz)		7.3728
PLL (MHz)		-
I/O		24
16-bit Timer		4
Connectivity	UART	2
	SPI	1
	I²C	2
	ISO 7816-3	1
BPWM		6
PDMA		2
CRC		CRC - 8
CRC- Configurable		-
Analog Comparator		2
12-bit DAC		-
Temperature Sensor		-
Internal Voltage Reference		-
Package		QFN33

Note:
1. ISP ROM programmable 1/2/3/4 KB Flash for user program loader (LDROM) shared from ARPOM.
2. ISO 7816-3 configurable as standard UART function.

4 PIN CONFIGURATION

4.1 Pin Configuration

Users can find pin configuaration informations in chapter 4 or by using NuTool - PinConfigure. The NuTool - PinConfigure contains all Nuvoton NuMicro Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

4.1.1 MUG51TB9AE Pin Diagram

4.1.1.1 QFN33 Package

Corresponding Part Number: MUG51TB9AE

MUG51TB9AE

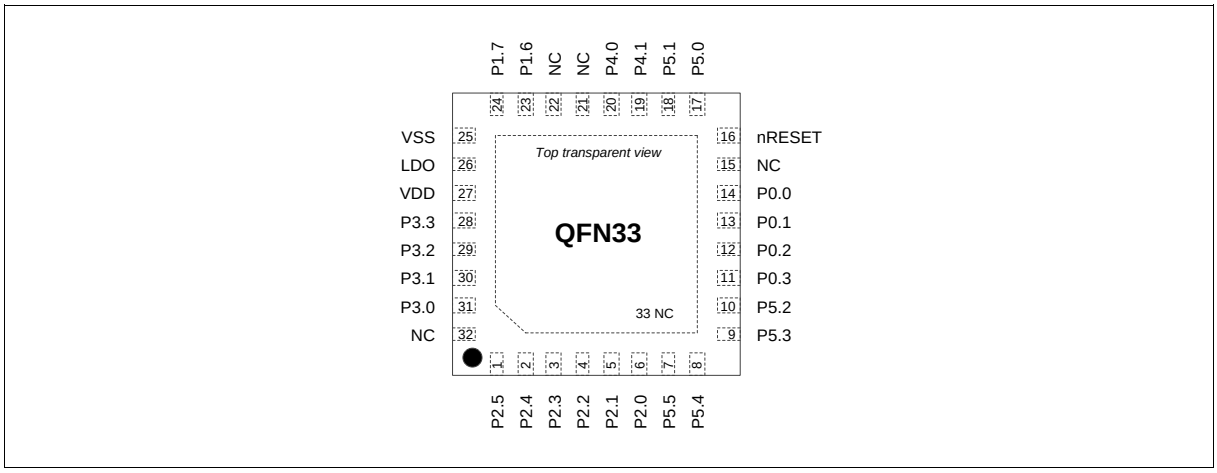


Figure 4.1-1 MUG51TB9AE Pin Assignment

4.1.2 MUG51TB9AE Multi Function Pin Diagram

4.1.2.1 QFN33 Package

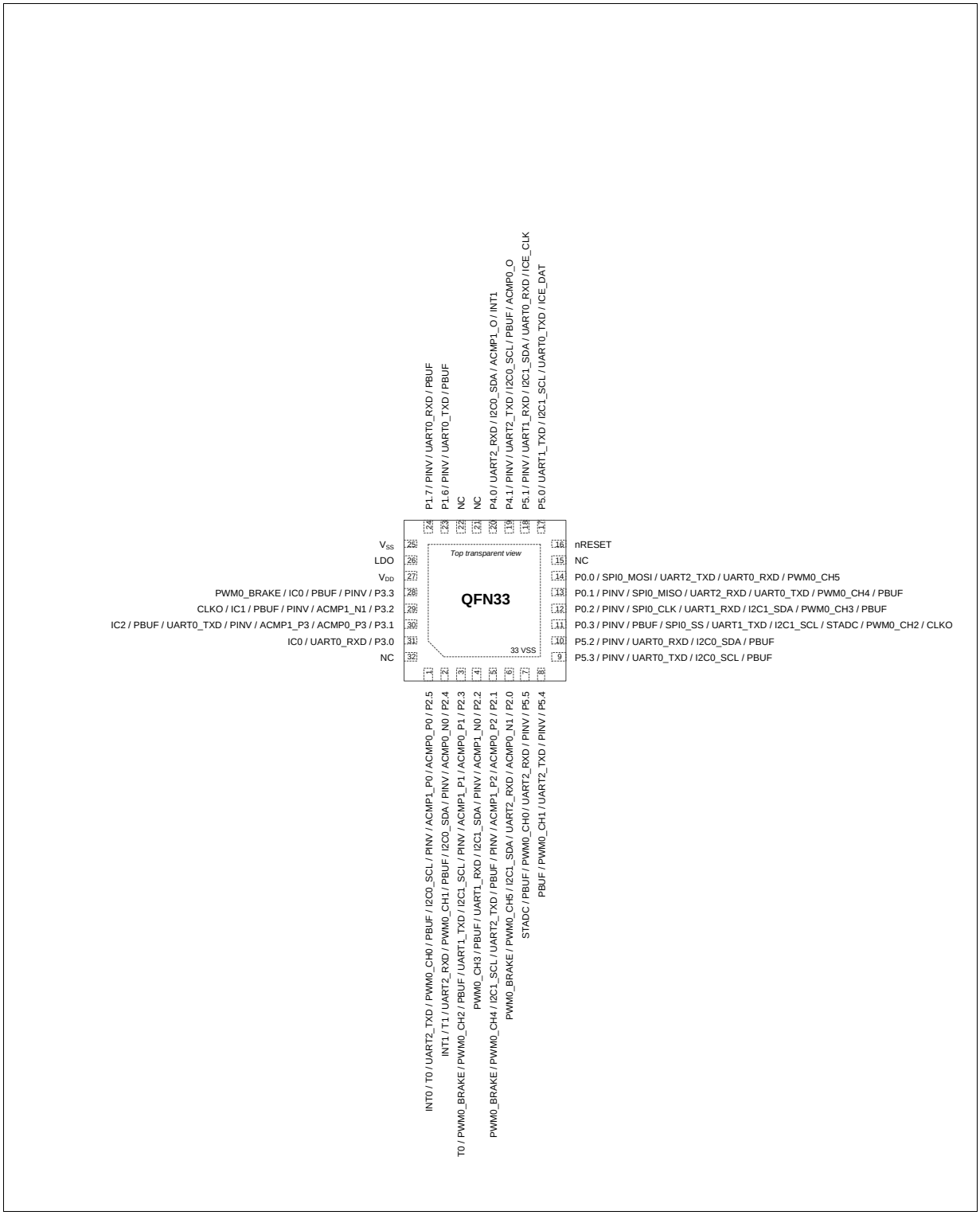


Figure 4.1-2 MUG51TB9AE Multi-Function Pin Assignment

Pin	MUG51TC9AE Pin Function
1	P2.5 / ACMP0_P0 / ACMP1_P0 / PINV / I2C0_SCL / PBUF / PWM0_CH0 / UART2_TXD / T0 / INT0
2	P2.4 / ACMP0_N0 / PINV / I2C0_SDA / PBUF / PWM0_CH1 / UART2_RXD / T1 / INT1
3	P2.3 / ACMP0_P1 / ACMP1_P1 / PINV / I2C1_SCL / UART1_TXD / PBUF / PWM0_CH2 / PWM0_BRAKE / T0
4	P2.2 / ACMP1_N0 / PINV / I2C1_SDA / UART1_RXD / PBUF / PWM0_CH3
5	P2.1 / ACMP0_P2 / ACMP1_P2 / PINV / PBUF / UART2_TXD / I2C1_SCL / PWM0_CH4 / PWM0_BRAKE
6	P2.0 / ACMP0_N1 / UART2_RXD / I2C1_SDA / PWM0_CH5 / PWM0_BRAKE
7	P5.5 / PINV / UART2_RXD / PWM0_CH0 / PBUF / STADC
8	P5.4 / PINV / UART2_TXD / PWM0_CH1 / PBUF
9	P5.3 / PINV / UART0_TXD / I2C0_SCL / PBUF
10	P5.2 / PINV / UART0_RXD / I2C0_SDA / PBUF
11	P0.3 / PINV / PBUF / SPI0_SS / UART1_TXD / I2C1_SCL / STADC / PWM0_CH2 / CLKO
12	P0.2 / PINV / SPI0_CLK / UART1_RXD / I2C1_SDA / PWM0_CH3 / PBUF
13	P0.1 / PINV / SPI0_MISO / UART2_RXD / UART0_TXD / PWM0_CH4 / PBUF
14	P0.0 / SPI0_MOSI / UART2_TXD / UART0_RXD / PWM0_CH5
15	NC
16	nRESET
17	P5.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT
18	P5.1 / PINV / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK
19	P4.1 / PINV / UART2_TXD / I2C0_SCL / PBUF / ACMP0_O
20	P4.0 / UART2_RXD / I2C0_SDA / ACMP1_O / INT1
21	NC
22	NC
23	P1.6 / PINV / UART0_TXD / PBUF
24	P1.7 / PINV / UART0_RXD / PBUF
25	V_{SS}
26	LDO
27	V_{DD}
28	P3.3 / PINV / PBUF / IC0 / PWM0_BRAKE
29	P3.2 / ACMP1_N1 / PINV / PBUF / IC1 / CLKO
30	P3.1 / ACMP0_P3 / ACMP1_P3 / PINV / UART0_TXD / PBUF / IC2
31	P3.0 / UART0_RXD / IC0
32	NC

4.2 Pin Description

4.2.1 MUG51TB9AE Pin Mapping

	Pin Number
Pin Name	**33**
P2.5	1
P2.4	2
P2.3	3
P2.2	4
P2.1	5
P2.0	6
P5.5	7
P5.4	8
P5.3	9
P5.2	10
P0.3	11
P0.2	12
P0.1	13
P0.0	14
NC	15
nRESET	16
P5.0	17
P5.1	18
P4.1	19
P4.0	20
NC	21
NC	22
P1.6	23
P1.7	24
V_{SS}	25
LDO	26
V_{DD}	27
P3.3	28
P3.2	29
P3.1	30
P3.0	31
NC	32

4.2.2 MUG51TB9AE Pin Functional Description

As default all GPIO type is defined as input mode. User should setting the GPIO Mode by PxMx register.

A: Analog suggest disable digial function O: output, I: input, I/O: bi-direction (Quasi)

Group	Pin Name	Type	Description
ACMP0	ACMP0_N0	A	Analog comparator 0 negative input 0 pin.
	ACMP0_N1		Analog comparator 0 negative input 1 pin.
	ACMP0_O	O	Analog comparator 0 output pin.
	ACMP0_P0	A	Analog comparator 0 positive input 0 pin.
	ACMP0_P1		Analog comparator 0 positive input 1 pin.
	ACMP0_P2		Analog comparator 0 positive input 2 pin.
	ACMP0_P3		Analog comparator 0 positive input 3 pin.
ACMP1	ACMP1_N0	A	Analog comparator 1 negative input 0 pin.
	ACMP1_N1		Analog comparator 1 negative input 1 pin.
	ACMP1_O	O	Analog comparator 1 output pin.
	ACMP1_P0	A	Analog comparator 1 positive input 0 pin.
	ACMP1_P1		Analog comparator 1 positive input 1 pin.
	ACMP1_P2		Analog comparator 1 positive input 2 pin.
	ACMP1_P3		Analog comparator 1 positive input 3 pin.
CLKO	CLKO	O	Clock Out
I2C0	I2C0_SCL	I/O	I2C0 clock pin.
	I2C0_SDA	I/O	I2C0 data input/output pin.
I2C1	I2C1_SCL	I/O	I2C1 clock pin.
	I2C1_SDA	I/O	I2C1 data input/output pin.
IC0	IC0	I/O	Input Capture channel 0
IC1	IC1	I/O	Input Capture channel 1
IC2	IC2	I/O	Input Capture channel 2
ICE	ICE_CLK	I	Serial wired debugger clock pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin
	ICE_DAT	O	Serial wired debugger data pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin
INT0	INT0	I	External interrupt 0 input pin.
INT1	INT1	I	External interrupt 1 input pin.
nRESET	nRESET	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. **Note:** It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

Group	Pin Name	Type	Description
PWM0	PWM0_BRAKE	I	PWM0 Brake input pin.
	PWM0_CH0	I/O	PWM0 channel 0 output/capture input.
	PWM0_CH1	I/O	PWM0 channel 1 output/capture input.
	PWM0_CH2	I/O	PWM0 channel 2 output/capture input.
	PWM0_CH3	I/O	PWM0 channel 3 output/capture input.
	PWM0_CH4	I/O	PWM0 channel 4 output/capture input.
	PWM0_CH5	I/O	PWM0 channel 5 output/capture input.
SPI0	SPI0_CLK	I/O	SPI0 serial clock pin.
	SPI0_MISO	I/O	SPI0 MISO (Master In, Slave Out) pin.
	SPI0_MOSI	I/O	SPI0 MOSI (Master Out, Slave In) pin.
	SPI0_SS	I/O	SPI0 slave select pin.
T0	T0	I/O	External count input to Timer/Counter 0 or its toggle output.
T1	T1	I/O	External count input to Timer/Counter 1 or its toggle output.
UART0	UART0_RXD	I	UART0 data receiver input pin.
	UART0_TXD	O	UART0 data transmitter output pin.
UART1	UART1_RXD	I	UART1 data receiver input pin.
	UART1_TXD	O	UART1 data transmitter output pin.
UART2	UART2_RXD	I	UART2 data receiver input pin.
	UART2_TXD	O	UART2 data transmitter output pin.

5 BLOCK DIAGRAM

5.1 MUG51TB9AE Full Function Block

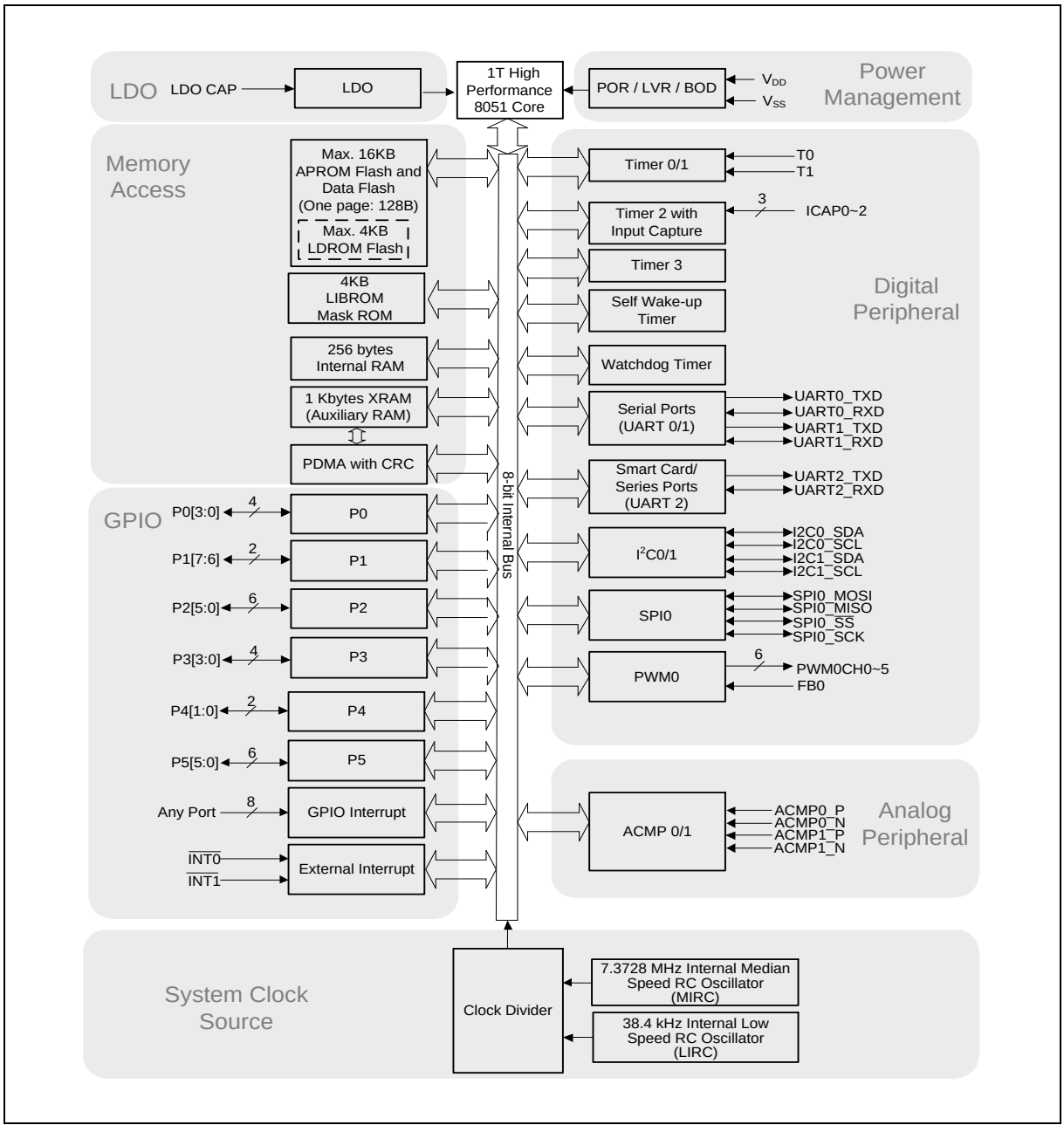


Figure 5.1-1 Functional Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 Memory Organization

A standard 80C51 based microcontroller divides the memory into two different sections, Program Memory and Data Memory. The Program Memory is used to store the instruction codes, whereas the Data Memory is used to store data or variations during the program execution.

The Data Memory occupies a separate address space from Program Memory. In MUG51TB9AE, there are 256 bytes of internal scratch-pad RAM. For many applications those need more internal RAM, the MUG51TB9AE provides another on-chip 1 Kbytes of RAM, which is called XRAM, accessed by MOVX instruction.

The whole embedded Flash, functioning as Program Memory, is divided into four blocks: Application ROM (APROM) normally for User Code, Loader ROM (LDROM) normally for Boot Code and defined special address from APROM, LIB memroy and CONFIG bytes for hardware initialization. Actually, APROM and LDROM function in the same way but have different size. Each block is accumulated page by page and the page size is 128 bytes. The Flash control unit supports Erase, Program, and Read modes. The external writer tools though specific I/O pins, In-Application-Programming (IAP), or In-System-Programming (ISP) can both perform these modes.

6.2 System Manager

The MUG51TB9AE has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. The MUG51TB9AE is embedded with two internal oscillators: one 38.4 kHz low-speed and one 8 MHz median speed, which is factory trimmed to ±3% under 0C~70C conditions. A clock divider CKDIV is also available on MUG51TB9AE for adjustment of the flexibility between power consumption and operating performance.

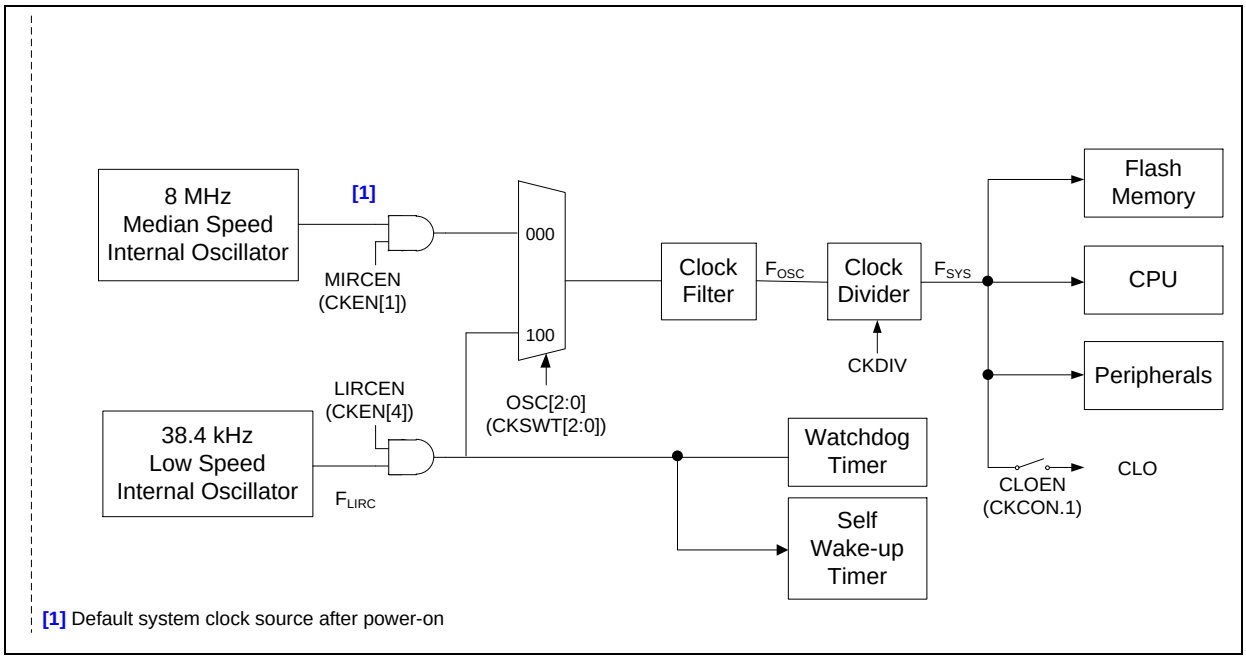


Figure 6.2-1 Clock System Block Diagram

6.3 Flash Memory Control

6.3.1 In-application-programming (IAP)

Unlike RAM's real-time operation, to update Flash data often takes long time. Furthermore, it is a quite complex timing procedure to erase, program, or read Flash data. The MUG51TB9AE carried out the Flash operation with convenient mechanism to help user re-programming the Flash content by In-Application-Programming (IAP). IAP is an in-circuit electrical erasure and programming method through software.

After IAP enabling by setting IAPEN (CHPCON.0 with TA protected) and setting the enable bit in IAPUEN that allows the target block to be updated, user can easily fill the 16-bit target address in IAPAH and IAPAL, data in IAPFD, and command in IAPCN. Then the IAP is ready to begin by setting a triggering bit IAPGO (IAPTRG.0). Note that IAPTRG is also TA protected. At this moment, the CPU holds the Program Counter and the built-in IAP automation takes over to control the internal charge-pump for high voltage and the detail signal timing. The erase and program time is internally controlled disregard of the operating voltage and frequency. Nominally, a page-erase time is 5 ms and a byte-program time is 23.5 μs. After IAP action completed, the Program Counter continues to run the following instructions. The IAPGO bit will be automatically cleared. An IAP failure flag, IAPFF (CHPCON.6), can be check whether the previous IAP operation was successful or not. Through this progress, user can easily erase, program, and verify the Flash Memory by just taking care of pure software.

6.3.2 In-Circuit-Programming (ICP)

The Flash Memory can be programmed by "In-Circuit-Programming" (ICP). If the product is just under development or the end product needs firmware updating in the hand of an end customer, the hardware programming mode will make repeated programming difficult and inconvenient. ICP method makes it easy and possible without removing the microcontroller from the system. ICP mode also allows customers to manufacture circuit boards with un-programmed devices. Programming can be done after the assembly process allowing the device to be programmed with the most recent firmware or a customized firmware.

There are three signal pins, nRESET , ICPDA, and ICPCK, involved in ICP function. nRESET is used to enter or exit ICP mode. ICPDA is the data input and output pin. ICPCK is the clock input pin, which synchronizes the data shifted in to or out from MCU under programming. User should leave these three pins plus V_{DD} and GND pins on the circuit board to make ICP possible.

Nuvoton provides ICP tool for MUG51TB9AE, which enables user to easily perform ICP through Nuvoton ICP programmer. The ICP programmer developed by Nuvoton has been optimized according to the electric characteristics of MCU. It also satisfies the stability and efficiency during production progress. For more details, please visit Nuvoton 8-bit Microcontroller website: Nuvoton 80C51 Microcontroller Technical Support.

6.3.3 On-Chip-Debugger (ICE)

The MUG51TB9AE is embedded in an on-chip-debugger (OCD) providing developers with a low cost method for debugging user code, which is available on each package. The OCD gives debug capability of complete program flow control with eight hardware address breakpoints, single step, free running, and non-intrusive commands for memory access. The OCD system does not occupy any locations in the memory map and does not share any on-chip peripherals.

6.4 GPIO Port Structure and Operation

6.4.1 GPIO Mode

The MUG51TB9AE has a maximum of 24 general purpose I/O pins which 18 bit-addressable general I/O pins grouped as 5 ports, P0 to P4, and general I/O pins grouped as P5. Each port has its port control register (Px register). The writing and reading of a port control register have different meanings. A write to port control register sets the port output latch logic value, where as a read gets the port pin logic state. These four modes are quasi-bidirectional (standard 8051 port structure), push-pull, input-only, and open-drain modes. Each port spends two special function registers PxM1 and PxM2 to select the I/O mode of port Px. The list below illustrates how to select the I/O mode of Px.n. Note that the default configuration of is input-only (high-impedance) after any reset.

All I/O pins can be selected as TTL level inputs or Schmitt triggered inputs by selecting corresponding bit in PxS register. Schmitt triggered input has better glitch suppression capability. All I/O pins also have bit-controllable, slew rate select ability via software. The Register Description are PxSR. By default, the slew rate is slow. If user would like to increase the I/O output speed, setting the corresponding bit in PxSR, the slew rate is selected in a faster level.

6.5 Timer

MUG51TB9AE provides following 16-bit Timer. Two 16-bit Timers/Counters 0 and 1 compatible with standard 8051. One 16-bit Timer 2 with three-channel input capture module and 9 input pin can be selected. One 16-bit auto-reload Timer 3, which can be the baud rate clock source of UARTs.

6.5.1 Features

- Two 16-bit Timers/Counters 0 and 1 compatible with standard 8051.
- One 16-bit Timer 2 with three-channel input capture module and 9 input pin can be selected.
- One 16-bit auto-reload Timer 3, which can be the baud rate clock source of UARTs.

6.6 Watchdog Timer (WDT)

The MUG51TB9AE provides one Watchdog Timer (WDT). It can be configured as a time-out reset timer to reset whole device. Once the device runs in an abnormal status or hangs up by outward interference, a WDT reset recover the system. It provides a system monitor, which improves the reliability of the system. Therefore, WDT is especially useful for system that is susceptible to noise, power glitches, or electrostatic discharge. The WDT also can be configured as a general purpose timer, of which the periodic interrupt serves as an event timer or a durational system supervisor in a monitoring system, which is able to operate during Idle or Power-down mode. WDTEN[3:0] (CONFIG4[7:4]) initialize the WDT to operate as a time-out reset timer or a general purpose timer.

The Watchdog time-out interval is determined by the formula $\frac{1}{F_{LIRC} \times \text{clock divider scalar}} \times 64$, where F_{LIRC} is the frequency of internal 38.4 kHz oscillator. The following table shows an example of the Watchdog time-out interval with different pre-scales.

6.7 Self Wake-up Timer (WKT)

6.7.1 Overview

The MUG51TB9AE has a dedicated Self Wake-up Timer (WKT), which serves for a periodic wake-up timer in low power mode or for general purpose timer. WKT remains counting in Idle or Power-down mode. When WKT is being used as a wake-up timer, a start of WKT can occur just prior to entering a power management mode. WKT has two clock source, internal LIRC 38.4 kHz. Note that the system clock frequency must be twice over WKT clock. If WKT starts counting, the selected clock source will remain active once the device enters Idle or Power-down mode. Note that the selected clock source of WKT will not automatically enabled along with WKT configuration. User should manually enable the selected clock source and waiting for stability to ensure a proper operation.

The WKT is implemented simply as a 16-bit auto-reload, up-counting timer with pre-scale 1/1 to 1/2048 selected by WKPS[2:0] (WKCON[2:0]). User fills the reload value into RWK register to determine its overflow rate. The RWK can reloadable when counter is count to overflow. The CWK can read current count value. The WKTR (WKCON.3) can be set to start counting. When the counter rolls over FFH, WKTF (WKCON.4) is set as 1 and a reload is generated and causes the contents of the RWK register to be reloaded into the internal 8-bit counter. If EWKT (EIE1.2) is set as 1, WKT interrupt service routine will be served.

6.8 Pulse Width Modulated (PWM)

6.8.1 Overview

The PWM (Pulse Width Modulation) signal is a useful control solution in wide application field. It can used on motor driving, fan control, backlight brightness tuning, LED light dimming, or simulating as a simple digital to analog converter output through a low pass filter circuit.

The MUG51TB9AE PWM0 is especially designed for motor control by providing three pairs, maximum 16-bit resolution of PWM0 output with programmable period and duty. The architecture makes user easy to drive the one-phase or three-phase brushless DC motor (BLDC), or three-phase AC induction motor. Each of six PWM can be configured as one of independent mode, complementary mode, or synchronous mode. If the complementary mode is used, a programmable dead-time insertion is available to protect MOS turn-on simultaneously. The PWM waveform can be edge-aligned or center-aligned with variable interrupt points.

6.8.2 Features

- Up To 6 output pins can be selected
- Supports maximum clock source frequency up to F_{SYS}
- Supports independent mode for PWM output
- Supports complementary mode for 3 complementary paired PWM output channels
- Dead-time insertion with 8-bit resolution
- Supports 16-bit resolution PWM counter
- Supports mask function and tri-state enable for each PWM pin
- Supports brake function

6.9 Serial Port (UART0 & UART1)

6.9.1 Overview

The MUG51TB9AE includes two enhanced full duplex serial ports enhanced with automatic address recognition and framing error detection. As control bits of these two serial ports are implemented the same. Generally speaking, in the following contents, there will not be any reference to serial port 1, but only to serial port 0.

Each serial port supports one synchronous communication mode, Mode 0, and three modes of full duplex UART (Universal Asynchronous Receiver and Transmitter), Mode 1, 2, and 3. This means it can transmit and receive simultaneously. The serial port is also receiving-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the register. The receiving and transmitting registers are both accessed at SBUF. Writing to SBUF loads the transmitting register, and reading SBUF accesses a physically separate receiving register. There are four operation modes in serial port. In all four modes, transmission initiates by any instruction that uses SBUF as a destination register.

6.9.2 Features

- Supports up to 2 UARTs: UART0, UART1
- Supports 1 Smart Card configuration as UART function as UART2 List in Smart Card Interface Chapter
- UART baud rate clock from MIRC.
- Full-duplex asynchronous communications
- Programmable 9th bit.
- TXD and RXD pins of UART0/1 exchangeable via software.

6.10 Smart Card Interface (SC)

6.10.1 Overview

The MUG51TB9AE provides Smart Card Interface controller (SC controller) with asynchronous protocal based on ISO/IEC 7816-3 standard. Software controls GPIO pins as the smartcard reset function and card detection function. This controller also provides UART emulation for high precision baud rate communication.

6.10.2 Features

- ISO 7816-3 T = 0, T = 1 compliant
- Programmable transmission clock frequency
- Programmable extra guard time selection
- Supports auto inverse convention function
- Supports UART mode
  - Full duplex, asynchronous communications
  - Supports programmable baud rate generator for each channel
  - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting SCnEGT register
  - Programmable even, odd or no parity bit generation and detection
  - Programmable stop bit, 1 or 2 stop bit generation

6.11 Serial Peripheral Interface (SPI)

6.11.1 Overview

The MUG51TB9AE provides two Serial Peripheral Interface (SPI) block to support high-speed serial communication. SPI is a full-duplex, high-speed, synchronous communication bus between microcontrollers or other peripheral devices. It provides either Master or Slave mode, high-speed rate up to $F_{SYS}/4$, transfer complete and write collision flag. For a multi-master system, SPI supports Master Mode Fault to protect a multi-master conflict.

6.11.2 Features

- Supports Master or Slave mode operation
- Supports MSB first or LSB first transfer sequence
- Slave mode up to 4 Mhz

6.12 Inter-Integrated Circuit (I^2C)

6.12.1 Overview

The MUG51TB9AE provides two Inter-Integrated Circuit (I^2C) bus to serves as an serial interface between the microcontrollers and the I^2C devices. The I^2C bus used two wires design (a serial data line SDA and a serial clock line SCL) to transfer information between devices.

The I^2C bus uses bi-directional data transfer between masters and slaves. There is no central master and the multi-master system is allowed by arbitration between simultaneously transmitting masters. The serial clock synchronization allows devices with different bit rates to communicate via one serial bus. The I^2C bus supports four transfer modes including master transmitter, master receiver, slave receiver, and slave transmitter. The I^2C interface only supports 7-bit addressing mode. A special mode General Call is also available. The I^2C can meet both standard (up to 100kbps) and fast (up to 400k bps) speeds.

6.12.2 Features

- 2 sets of I^2C devices
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- 7-bit addressing mode
- Standard mode (100 kbps) and Fast mode (400 kbps).
- Supports 8-bit time-out counter requesting the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflows
- Multiple address recognition (four slave addresses with mask option)
- Supports hold time programmable

6.13 Analog Comparator Controller (ACMP)

6.13.1 Overview

The MUG51TB9AE contains two comparators. The comparator output is logic 1 when positive input is greater than negative input; otherwise, the output is 0. The comparator can be configured to generate an interrupt when the comparator output value changes.

6.13.2 Features

- Analog input voltage range: 0 ~ AV_{DD}(voltage of AV_{DD} pin)
- Supports hysteresis function
- Supports wake-up function
- Selectable input sources of negative input
- Comparator ACMP0 supports
  - 4 positive sources:
    - P2.5 (ACMPn_P0)
    - P2.3 (ACMPn_P1)
    - P2.1 (ACMPn_P2)
    - P3.1 (ACMPn_P3)
  - 4 negative sources:
    - P2.4 (ACMP0_N0)
    - Comparator Reference Voltage (CRV)
    - VBG (BAND-GAP voltage)
    - P2.0 (ACMP0_N1)
- Comparator ACMP1 supports
  - 4 positive sources:
    - P2.5 (ACMPn_P0)
    - P2.3 (ACMPn_P1)
    - P2.1 (ACMPn_P2)
    - P3.1 (ACMPn_P3)
  - 4 negative sources:
    - P2.2 (ACMP1_N0)
    - Comparator Reference Voltage (CRV)
    - VBG (BAND-GAP voltage)
    - P3.2 (ACMP1_N1)

6.14 PDMA Controller (PDMA)

6.14.1 Overview

The MUG51TB9AE provides peripheral direct memory access (PDMA) controller. The PDMA controller is used to provide high-speed data transfer between memory and peripherals or between memory and memory. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications.

6.14.2 Features

- Supports transfer data width of 8 bits
- Supports software and SPI and SMC/UART request
- Supports source and destination address increment size can be byte
- Supports transfer done and half done interrupt
- Supports using PDMA to write data to perform CRC operation

6.15 Instruction Set

6.15.1 Instruction Set And Addressing Modes

The MUG51TB9AE executes all the instructions of the standard 80C51 family fully compatible with MCS-51. However, the timing of each instruction is different for it uses high performance 1T 8051 core. The architecture eliminates redundant bus states and implements parallel execution of fetching, decode, and execution phases. The MUG51TB9AE uses one clock per machine-cycle. It leads to performance improvement of rate 8.1 (in terms of MIPS) with respect to traditional 12T 80C51 device working at the same clock frequency. However, the real speed improvement seen in any system will depend on the instruction mix.

All instructions are coded within an 8-bit field called an OPCODE. This single byte should be fetched from Program Memory. The OPCODE is decoded by the CPU. It determines what action the CPU will take and whether more operation data is needed from memory. If no other data is needed, then only one byte was required. Thus the instruction is called a one byte instruction. In some cases, more data is needed, which is two or three byte instructions.

7 APPLICATION CIRCUIT

7.1 Power Supply Scheme

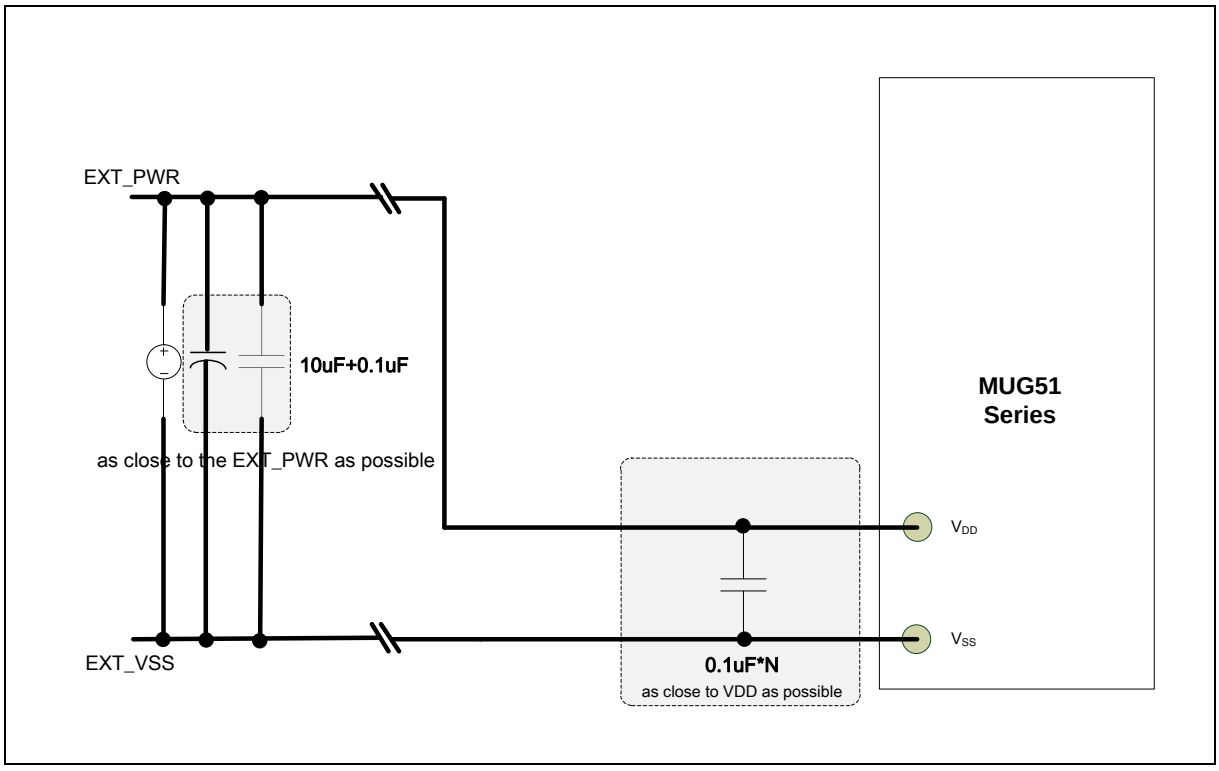
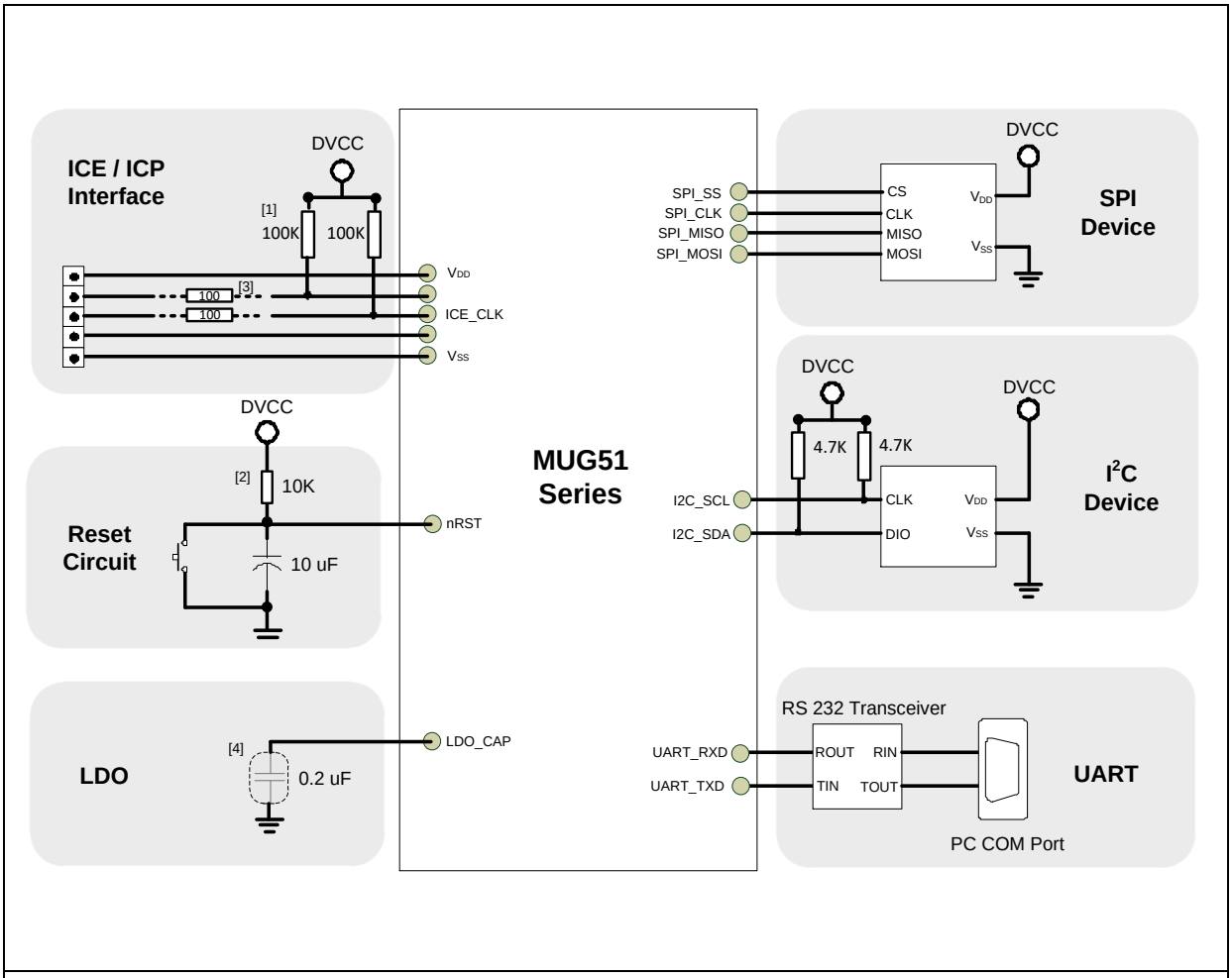


Figure 7.1-1 MUG51TB9AE Power Supply Circuit

7.2 Peripheral Application Scheme



Note:

1. It is recommended to use 100 kΩ pull-up resistor on both ICE_DAT and ICE_CLK pin.
2. It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.
3. It is suggest add 100ohm series resistor between ICE_DAT/ICE_CLK and writer pin to filter the disturb of noise on the circuit.

Figure 7.2-1 MUG51TB9AE Peripheral Interface Circuit

8 ELECTRICAL CHARACTERISTICS

Please refer to the relative Datasheet for detailed information about the MUG51TB9AE electrical characteristics.

8.1 General Operating Conditions

(V_{DD}-V_{SS} = 1.8 ~ 5.5V, T_A = 25°C, Fsys = 24 MHz unless otherwise specified.)

8.1.1 MUG51TB9AE

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
V_{DD}	Operation voltage	1.8	-	5.5	V	
AV_{DD}[1]	Analog operation voltage	V_{DD}				

Note:

1. It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation.
2. Based on characterization, tested in production.

Table 8.1-1 General Operating Conditions

8.2 DC Electrical Characteristics

8.2.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

8.2.1.1 MUG51TB9AE Power consumption

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for V_{DD} = 1.8V ~ 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.
- $V_{DD} = AV_{DD}$
- When the peripherals clock base is the system clock Fsys.
- Program run “while (1);” in Flash.

Normal Run Mode

Symbol	Conditions	Fsys	Typ [2]	Max[3]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_RUN}	Normal run mode, executed from Flash, all peripherals disable	7.3728 MHz (MIRC)[1]	0.98	1.08	1.16	1.17	mA
		4 MHz (MIRC)[1]	0.65	0.73	0.78	0.79	
		2 MHz (MIRC)[1]	0.47	0.54	0.58	0.6	
		1.2288 MHz (MIRC)[1]	0.41	0.47	0.51	0.52	
		38.4 kHz (LIRC)[1]	0.13	0.19	0.21	0.23	
	Normal run mode, executed from Flash, all peripherals enable	7.3728 MHz (MIRC)[1]	1.25	1.35	1.42	1.44	
		4 MHz (MIRC)[1]	0.79	0.86	0.91	0.92	
		2 MHz (MIRC)[1]	0.54	0.61	0.65	0.66	
		1.2288 MHz (MIRC)[1]	0.45	0.52	0.56	0.57	
		38.4 kHz (LIRC)[1]	0.14	0.2	0.22	0.24	

Note:
1. This value base on MIRC enable, LIRC enable
2. $AV_{DD} = V_{DD}$ = 3.3V, LVR17 enabled, POR enable and BOD enable.
3. $AV_{DD} = V_{DD}$ = 5.5V, LVR17 enabled, POR enable and BOD enable.
4. Based on characterization, not tested in production unless otherwise specified.

Table 8.2-1 Current Consumption in Normal Run Mode

Idle Mode

Symbol	Conditions	Fsys	Typ [2]	Max[3]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_IDLE}	Idle mode, all peripherals disable	7.3728 MHz (MIRC)[1]	0.56	0.62	0.66	0.67	mA
		4 MHz (MIRC)[1]	0.42	0.48	0.52	0.53	
		2 MHz (MIRC)[1]	0.35	0.41	0.46	0.46	
		1.2288 MHz (MIRC)[1]	0.33	0.39	0.42	0.43	
		38.4 kHz (LIRC)[1]	0.13	0.19	0.21	0.22	
	Idle mode, all peripherals enable	7.3728 MHz (MIRC)[1]	0.83	0.91	0.96	0.97	
		4 MHz (MIRC)[1]	0.56	0.63	0.67	0.68	
		2 MHz (MIRC)[1]	0.43	0.49	0.52	0.54	
		1.2288 MHz (MIRC)[1]	0.38	0.44	0.47	0.49	
		38.4 kHz (LIRC)[1]	0.13	0.2	0.22	0.24	

Note:

1. This value base on MIRC enable, LIRC enable
2. AVDD = VDD = 3.3V, LVR17 enabled, POR enable and BOD enable.
3. AVDD = VDD = 5.5V, LVR17 enabled, POR enable and BOD enable.
4. Based on characterization, not tested in production unless otherwise specified.

Table 8.2-2 Current Consumption in Idle Mode

Power-down mode

Symbol	Test Conditions	Typ	Max[5]			Unit
		T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_PD}	Power-down mode Level 0 @3.3V[1]	14	-	-	-	µA
	Power-down mode Level 1 @3.3V[1]	1.3	-	-	-	
	Power-down mode Level 2 @3.3V[1]	0.8	-	-	-	
	Power-down mode Level 2 @3.3V[2]	1.2	-	-	-	
	Power-down mode Level 2 @3.3V[3]	3.8	-	-	-	
	Power-down mode Level 2 @3.3V[4]	2.0	-	-	-	
	Power-down mode Level 0 @5.5V[1]	-	20.7	30.9	46.3	
	Power-down mode Level 1 @5.5V[1]	-	2.7	10.4	23.7	
	Power-down mode Level 2 @5.5V[1]	-	2.1	9.3	21.2	
	Power-down mode Level 0 @5.5V[2]	-	20.9	31.5	46.0	
	Power-down mode Level 1 @5.5V[2]	-	3.0	10.7	23.1	
	Power-down mode Level 2 @5.5V[2]	-	2.5	9.5	20.7	
	Power-down mode Level 0 @5.5V[3]		23.9	34.6	48.6	
	Power-down mode Level 1 @5.5V[3]		6.0	13.8	25.6	
	Power-down mode Level 2 @5.5V[3]	-	5.5	12.6	23.2	
	Power-down mode Level 0 @5.5V[4]		21.9	32.5	46.0	
	Power-down mode Level 1 @5.5V[4]		4.0	11.8	23.2	
	Power-down mode Level 2 @5.5V[4]	-	3.4	10.5	20.7	

Note:

1. All peripherals disable, LVR disable, POR disable and BOD disable.
2. All peripherals disable, LVR enable, POR disable and BOD disable.
3. All peripherals disable, LVR enable, POR disable and Low power BOD enable.
4. LIRC on, WKT and WDT on, all other peripherals disable, LVR disable, POR disable and BOD disable.
5. Based on characterization, not tested in production unless otherwise specified.
6. The Power-down mode condition and select please reference Table 8.2-4.
7. When analog peripheral blocks such as ADC and ACMP are ON, an additional power consumption should be considered.

Table 8.2-3 Current Consumption in Power-down Mode

Register/Instruction Mode	PD (PCON.1)	IDL (PCON.0)	PDLS(PDL[1:0])
Normal mode	0	0	-
Idle mode	0	1	-
Power-down mode (PD) Level 0: all IP off / flash standby / MIRC off / LDO on (Default)	1	X	00
Power-down mode (PD) Level 1: all IP off / flash standby / MIRC off / LDO off	1	X	01
Power-down mode (PD) Level 2: all IP off / flash off / MIRC off / LDO off	1	X	10

Table 8.2-4 Entry Setting of Power-down Mode

8.2.2 On-Chip Peripheral Current Consumption

- The typical values for T_A= 25 °C and V_{DD} = AV_{DD} = 3.3 V unless otherwise specified.
- All GPIO pins are set as output high of push pull mode without multi-function.
- The system clock = 24 MHz.
- The result value is calculated by measuring the difference of current consumption between all peripherals clocked off and only one peripheral clocked on

Peripheral	$I_{DD\ Base}$	I_{DD}[1]	Unit
ACMP0[3]	1.0		µA
ACMP1[3]	1.1		
PWM0	152.3		
SPI0	40.2		
UART0	98.8	1	
UART1		1	
I2C0	118.7	1	
I2C1		1	
SC0	67.8		
Pin Interrupt	0.2		
TIMER 0	145	4.1	
TIMER 1		3.9	
TIMER 2		4.4	
TIMER 3		10	
INT0	0.3		
INT1	0.3		
WDT	0.4		
WKT	0.7		
PDMA0	13.4	0.5	
PDMA1		0.5	
CAPTURE0	145	0.5	
CAPTURE1		0.3	
CAPTURE2		0.5	

Note:

1. Guaranteed by characterization results, not tested in production.
2. When the ADC is turned on, add an additional power consumption per ADC for the analog part.
3. When the ACMP is turned on, add an additional power consumption per ACMP for the analog part.

Table 8.2-5 Peripheral Current Consumption

8.2.3 Wakeup Time from Low-Power Modes

The wakeup times given in Table 8.2-6 Low-Power Mode Wakeup Timings is measured on a wakeup phase with a 7.3728 MHz MIRC oscillator.

Symbol	Parameter		Typ	Max	Unit
t_{WU_IDLE}	Wakeup from IDLE mode		5	6	cycles
t_{WU_NPD}[1][2]	Wakeup from Power-down Level 0 mode	Fsys = MIRC @5.5V	4	20	µs
		Fsys = MIRC @3.3V	5	20	µs
		Fsys = MIRC @1.8V	7	20	µs
		Fsys = LIRC	938	1500	µs
	Wakeup from Power-down Level 1 mode	Fsys = MIRC @3.3V	8	20	µs
	Wakeup from Power-down Level 2 mode	Fsys = MIRC @3.3V	10	20	µs

Note:

1. Based on test during characterization, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first.
3. Power down level select table please reference Table 8.2-4 Entry Setting of Power-down Mode

Table 8.2-6 Low-Power Mode Wakeup Timings

8.2.4 I/O DC Characteristics

8.2.4.1 GPIO Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage	0	-	$0.3*V_{DD}$	V	
V_{IL1}	Input low voltage (I/O with TTL input)	V_{SS}-0.3	-	$0.2V_{DD}$-0.1	V	
V_{IH}	Input high voltage	0.2VDD+0.9	-	VDD+0.3	V	
V_{IH1}	Input high voltage (I/O with Schmitt trigger input and Xin)	$0.7*V_{DD}$	-	V_{DD}	V	
V_{HY}[1]	Hysteresis voltage of schmitt input	-	$0.2*V_{DD}$	-	V	
I_{LK}[2]	Input leakage current	-1		1	µA	$V_{SS} < V_{IN} < V_{DD}$, Open-drain or input only mode
		-1		1		$V_{DD} < V_{IN} < 5.5$ V, Open-drain or input only mode
R_{PU}[1] [3]	Pull up resistor	40	-	60	kΩ	V_{DD} = 5.5 V, Quasi mode and Input mode with pull up enable
		40	-	60		V_{DD} = 3.3 V, Quasi mode and Input mode with pull up enable
		40	-	70		V_{DD} = 1.8 V, Quasi mode and Input mode pull up enable
R_{PD}[1] [3]	Pull down resistor	40	-	60	kΩ	V_{DD} = 5.5 V, Quasi mode and Input mode with pull up enable
		40	-	60		V_{DD} = 3.3 V, Quasi mode and Input mode with pull up enable
		40	-	70		V_{DD} = 1.8 V, Quasi mode and Input mode pull up enable

Note:

1. Guaranteed by characterization result, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.
3. To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up resistors must be disabled. Leakage could be higher than the maximum value, if positive current is injected on adjacent pins
4. Test condition of V_{DD} is base on the maximum value of V_{DD}

Table 8.2-7 GPIO Input Characteristics

8.2.4.2 nRESET Pin Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	-	-	0.3*V_{DD}	V	
V_{IHR}	Positive going threshold, nRESET	0.7*V_{DD}	-	-	V	
R_{RST}[1]	Internal nRESET pull up resistor	45	-	60	KΩ	V_{DD} = 5.5 V
		50	-	65		V_{DD} = 1.8 V
t_{FR}[1]	nRESET input response time	-	1.5	-	µs	Normal run and Idle mode
		10	-	25		Power-down mode

Note:

1. Guaranteed by characterization result, not tested in production.
2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

Table 8.2-8 nRESET Pin Input Characteristics

8.2.4.3 GPIO Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR}[1] [2]	Source current for quasi-bidirectional mode and high level	-7.7	-7.8	-8	µA	V_{DD} = 5.5 V V_{IN} =(V_{DD}-0.4) V
		-7.7	-7.8	-8	µA	V_{DD} = 4.5 V V_{IN} =(V_{DD}-0.4) V
		-7.6	-7.8	-7.9	µA	V_{DD} = 3.3 V V_{IN} =(V_{DD}-0.4) V
		-7.6	-7.8	-7.9	µA	V_{DD} = 2.5 V V_{IN} =(V_{DD}-0.4) V
		-7.6	-7.7	-7.8	µA	V_{DD} = 1.8 V V_{IN} =(V_{DD}-0.4) V
	Source current for push-pull mode and high level	-7	-9	-11	mA	V_{DD} = 5.5 V V_{IN} =(V_{DD}-0.4) V
		-6	-7.8	-10	mA	V_{DD} = 4.5 V V_{IN} =(V_{DD}-0.4) V
		-5	-5.7	-8	mA	V_{DD} = 3.3 V V_{IN} =(V_{DD}-0.4) V
		-4	-4.8	-6	mA	V_{DD} = 2.5 V V_{IN} =(V_{DD}-0.4) V
		-2	-2.6	-4	mA	V_{DD} = 1.8 V V_{IN} =(V_{DD}-0.4) V
I_{SK}[1] [2]	Sink current for push-pull mode and low level	16	20	24	mA	V_{DD} = 5.5 V V_{IN} = 0.4 V
		15	19	23	mA	V_{DD} = 4.5 V V_{IN} = 0.4 V
		13	15	17	mA	V_{DD} = 3.3 V V_{IN} = 0.4 V
		10	12	14	mA	V_{DD} = 2.5 V V_{IN} = 0.4 V
		5	7	9	mA	V_{DD} = 1.8 V V_{IN} = 0.4 V
V_{OH}[1]	Output high level voltage for quasi-bidirectional mode	V_{DD}-0.4	-	V_{DD}	V	I_{SR} = -7.3 uA
	Output high level voltage for push-pull mode	V_{DD}-1.2	-	V_{DD}	V	V_{DD} ≥ 4.5 V I_{SR} = -20 mA
					V	V_{DD} ≥ 3.3 V I_{SR} = -13 mA
					V	V_{DD} ≥ 2.7 V I_{SR} = -9 mA

		V_{DD}-0.4	-	V_{DD}	V	V_{DD} ≥ 4.5 V I_{SR} = -9 mA
					V	V_{DD} ≥ 3.3 V I_{SR} = -6 mA
					V	V_{DD} ≥ 2.7 V I_{SR} = -4.2 mA
V_{OL}[1]	Output low level voltage for push-pull mode	V_{SS}	-	1.2	V	V_{DD} ≥ 2.7 V I_{SR} = 20 mA (Max.)
		V_{SS}	-	0.4	V	V_{DD} ≥ 5.5 V I_{SR} = 18 mA
					V	V_{DD} ≥ 3.3 V I_{SR} = 16 mA
					V	V_{DD} ≥ 2.4 V I_{SR} = 9.7 mA
C_{IO}[1]	I/O pin capacitance	-	5	-	pF	

Note:

1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.

Table 8.2-9 GPIO Output Characteristics

8.3 AC Electrical Characteristics

The maximum values are obtained for V_{DD} = 1.8 V ~ 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified. V_{DD} = AV_{DD}.

8.3.1 7.3728 MHz Internal Median Speed RC Oscillator (MIRC)

The 7.3728 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	1.8	-	5.5	V	
F_{MIRC}	Oscillator frequnecy	-	7.3728	-	MHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-1[1]	-	1[1]	%	T_A = 25 °C, V_{DD} = 3.3V
		-2[2]	-	2[2]	%	T_A = 0°C ~ +70 °C, V_{DD} = 1.8 ~ 5.5V
		-10[2]		10[2]	%	T_A = -40°C ~ 105°C, V_{DD} = 1.8 ~ 5.5V
I_{MIRC}[2]	Operating current	-	30	60	µA	
T_S[3]	Stable time	-	5	10	µs	T_A = -40°C ~ +105 °C, V_{DD} = 1.8 ~ 5.5V

Note:

1. Based on characterization, tested in production.
2. Guaranteed by characterization result, not tested in production.
3. Guaranteed by design.

Table 8.3-1 8 MHz Internal Median Speed RC Oscillator (MIRC) Characteristics

8.3.2 38.4 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	1.8	-	5.5	V	
F_{LRC}	Oscillator frequnecy	-	38.4	-	kHz	
	Frequency drift over temperarure and volatge	-2[1]	-	2[1]	%	T_A = 25 °C, V_{DD} = 5V
		-10[2]	-	10[2]	%	T_A=-40~105°C VDD=1.8V~5.5V Without software calibration
I_{LRC} [2]	Operating current	-	0.85	1	μA	V_{DD} = 3.3V
T_S	Stable time	-	500	-	μs	T_A=-40~105°C VDD=1.8V~5.5V

Note:

1. Guaranteed by characterization, tested in production.
2. Guaranteed by characterization, not tested in production.
3. The 38.4 kHz low speed RC oscillator can be calibrated by user.
4. Guaranteed by design.

Table 8.3-2 38.4 kHz Internal Low Speed RC Oscillator(LIRC) Characteristics

8.3.3 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[1].	Unit	Test Conditions[2]
$t_{f(I/O)out}$	Normal mode [4] output high (90%) to low level (10%) falling time	4.6	5.1	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.9	3.3		C_L = 10 pF, V_{DD} >= 5.5 V
		6.6	8		C_L = 30 pF, V_{DD} >= 3.3 V
		4.3	5		C_L = 10 pF, V_{DD} >= 3.3 V
		8.5	12.5		C_L = 30 pF, V_{DD} >= 1.8 V
		8.0	10.7		C_L = 10 pF, V_{DD} >= 1.8 V
$t_{f(I/O)out}$	High slew rate mode [5] output high (90%) to low level (10%) falling time	4.0	4.3	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.1	2.5		C_L = 10 pF, V_{DD} >= 5.5 V
		4.9	5.8		C_L = 30 pF, V_{DD} >= 3.3 V
		3.0	3.7		C_L = 10 pF, V_{DD} >= 3.3 V
		9.5	13.8		C_L = 30 pF, V_{DD} >= 1.8 V
		5.4	7.4		C_L = 10 pF, V_{DD} >= 1.8 V
$t_{r(I/O)out}$	Normal mode [4] output low (10%) to high level (90%) rising time	5.6	6.1	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		3.4	3.7		C_L = 10 pF, V_{DD} >= 5.5 V
		8.1	9.4		C_L = 30 pF, V_{DD} >= 3.3 V
		5.1	5.8		C_L = 10 pF, V_{DD} >= 3.3 V
		15.1	20.3		C_L = 30 pF, V_{DD} >= 1.8 V
		9.6	12.4		C_L = 10 pF, V_{DD} >= 1.8 V
$t_{r(I/O)out}$	High slew rate mode [5] output low (10%) to high level (90%) rising time	4.8	5.2	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.1	2.5		C_L = 10 pF, V_{DD} >= 5.5 V
		6.4	7.4		C_L = 30 pF, V_{DD} >= 3.3 V
		3.0	3.7		C_L = 10 pF, V_{DD} >= 3.3 V
		12.7	16.9		C_L = 30 pF, V_{DD} >= 1.8 V
		5.4	7.4		C_L = 10 pF, V_{DD} >= 1.8 V
$f_{max(I/O)out}$[3]	I/O maximum frequency	24	24	MHz	C_L = 30 pF, V_{DD} >= 1.8 V
					C_L = 10 pF, V_{DD} >= 1.8 V

Note:

1. Guaranteed by characterization result, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. The maximum frequency is defined by $f_{max} = \frac{2}{3 \times (t_f + t_r)}$.
4. PxSR.n bit value = 0, Normal output slew rate
5. PxSR.n bit value = 1, high speed output slew rate

Table 8.3-3 I/O AC Characteristics

8.4 Analog Characteristics

8.4.1 Reset and Power Control Block Characteristics

The maximum values are obtained for V_{DD} = 1. 8V ~ 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V.The parameters in below table are derived from tests performed under ambient temperature unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{POR}[1]	POR Operating Current	-	60	100	μA	AV_{DD} = 5.5V
I_{LVR}[1]	LVR Operating Current	-	30	80		AV_{DD} = 5.5V
	LVR Low Power Run Mode Operating Current		0.5	1		AV_{DD} = 5.5V
I_{BOD}[1]	BOD Operating Current	-	0.5	2.9		AV_{DD} = 5.5V
V_{POR}	POR Reset Voltage	1.45	1.55	1.65	V	-
V_{LVR}	LVR Reset Voltage	1.55	1.63	1.70		-
V_{BOD}	BOD Brown-Out Detect Voltage	1.7	1.8	2		
		1.9	2	2.2		
		2.3	2.4	2.5		
		2.55	2.7	2.8		
		2.85	3	3.2		
		3.55	3.7	3.9		
		4.2	4.4	4.5		
T_{LVR_SU}[1]	LVR Startup Time	-	1	2	μs	-
T_{LVR_RE}[1]	LVR Respond Time	-	15	20		-
	LVR Low Power Run Mode Respond Time	-	20	30		-
T_{BOD_SU}[1]	BOD Startup Time	-	250	350		-
T_{BOD_RE}[1]	BOD Respond Time	-	19	30		-

Note:

1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.

Table 8.4-1 Reset and Power Control Unit

8.4.2 Analog Comparator Controller (ACMP)

The maximum values are obtained for V_{DD} = 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
AV_{DD}	Analog supply voltage	1.8	-	5.5	V	$V_{DD} = AV_{DD}$
T_A	Temperature	-40	-	105	℃	
I_{DD}	Operating current	-	2	5	μA	
V_{CM}[2]	Input common mode voltage range	0.35	1/2 AV_{DD}	AV_{DD} -0.3		
V_{DI}[2]	Differential input voltage sensitivity	10	20	-	mV	Hysteresis disable
V_{offset}[2]	Input offset voltage	-	10	20	mV	Hysteresis disable
V_{hys}[2]	Hysteresis window	-	10	20	mV	
A_v[1]	DC voltage Gain	45	65	75	dB	
T_d[2]	Propagation delay	-	-	5	μS	
T_{Stable}[2]	Stable time	-	-	5	μS	
A_{CRV}[2]	CRV output voltage	-5	-	5	%	AV_{DD} x (1/6+CRVCTL/24)
R_{CRV}[2]	Unit resistor value	-	4.5	-	kΩ	
T_{SETUP_CRV}[2]	Stable time	-	-	2	μS	CRV output voltage settle to ±5%
I_{DD_CRV}[2]	Operating current	-	2	-	μA	

Note:

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production. unless otherwise specified.

Table 8.4-2 ACMP Characteristics

8.5 Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[1]	Supply voltage	-	1.5	-	V	T_A = 25°C
T_{ERASE}	Page erase time	-	5	-	ms	
T_{PROG}	Program time	-	10	-	µs	
I_{DD1}	Read current	-	4	-	mA	
I_{DD2}	Program current	-	4	-	mA	
I_{DD3}	Erase current	-	12	-	mA	
N_{ENDUR}	Endurance	100,000	-		cycles[2]	T_J = -40°C~125°C
T_{RET}	Data retention	50	-	-	year	100 kcycle[3] T_A = 55°C
		25	-	-	year	100 kcycle[3] T_A = 85°C
		10	-	-	year	100 kcycle[3] T_A = 105°C

Note:

1. V_{FLA} is source from chip internal LDO output voltage.
2. Number of program/erase cycles.
3. Guaranteed by design.

Table 8.5-1 Flash Memory Characteristics

8.6 Absolute Maximum Ratings

Volrage Stesses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

8.6.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-VSS[1]	DC power supply	-0.3	6.5	V
ΔV_{DD}	Variations between different power pins	-	50	mV
$\|V_{DD} - AV_{DD}\|$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
ΔV_{SS}	Variations between different ground pins	-	50	mV
$\|V_{SS} - AV_{SS}\|$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input voltage on I/O	V_{SS}-0.3	6.5	V

Note:

1. All main power (V_{DD}, AV_{DD}) and ground (V_{SS}, AV_{SS}) pins must be connected to the external power supply.

Table 8.6-1 Voltage Characteristics

8.6.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD}[1]	Maximum current into V_{DD}	-	150	mA
ΣI_{SS}	Maximum current out of V_{SS}	-	150	
I_{IO}	Maximum current sunk by a I/O Pin	-	22	
	Maximum current sourced by a I/O Pin	-	10	
	Maximum current sunk by total I/O Pins[2]	-	100	
	Maximum current sourced by total I/O Pins[2]	-	100	
$I_{INJ(PIN)}$ [3]	Maximum injected current by a I/O Pin	-	±5	
$\Sigma I_{INJ(PIN)}$ [3]	Maximum injected current by total I/O Pins	-	±25	

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by $V_{IN}>A_{VDD}$ and a negative injection is caused by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 8.6-2 Current Characteristics

8.6.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA})$

- T_A = ambient temperature (°C)
- θ_{JA} = thermal resistance junction-ambient (°C/Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	105	°C
T_J	Operating junction temperature	-40	-	125	
T_{ST}	Storage temperature	-65	-	150	
θ_{JA}[1]	Thermal resistance junction-ambient 33-pin QFN(4x4 mm)	-	28	-	°C/Watt

Note:

1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 8.6-3 Thermal Characteristics

8.6.4 EMC Characteristics

8.6.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

8.6.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latchup

performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

8.6.4.3 Electrical fast transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system..

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International ElectrotechnicalCommission (IEC).

8.6.4.4 EMC Character Table

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[1]	Electrostatic discharge,human body mode	- 7000	-	+ 7000	V
V_{CDM}[2]	Electrostatic discharge,charge device model	- 1000	-	+ 1000	
LU[3]	Pin current for latch-up[3] @V_{DD} = 5.5V	- 150	-	+ 150	mA
V_{EFT}[*4] [*5]	Fast transient voltage burst	- 4.4	-	+ 4.4	kV

Note:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test.
5. The performace cretia class is 4A.

Table 8.6-4 EMC Characteristics

8.6.5 Package Moisture Sensitivity(MSL)

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

Pacakge	MSL
33-pin QFN(4x4 mm) [1]	MSL 3
Note: Determined according to IPC/JEDEC J-STD-020	

Table 8.6-5 Package Moisture Sensitivity (MSL)

8.6.6 Soldering Profile

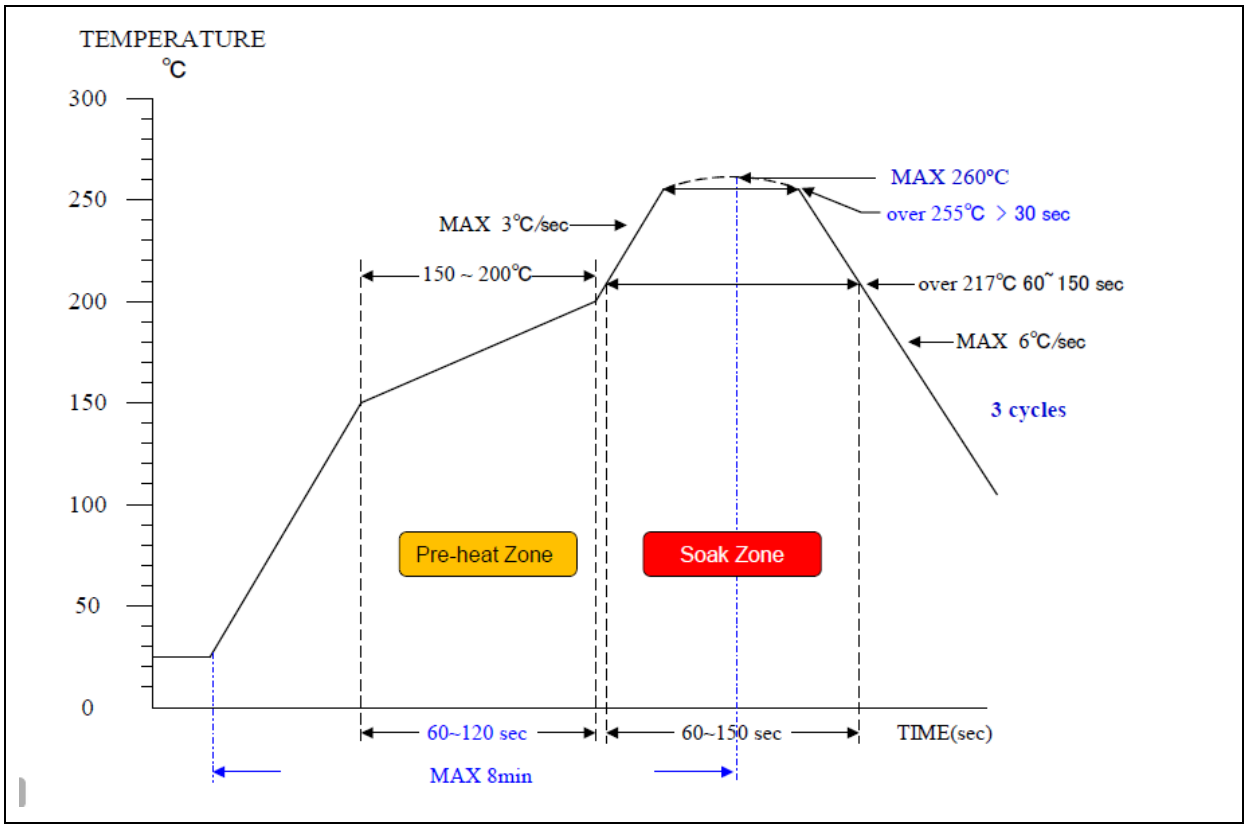


Figure 8.6-1 Soldering Profile from J-STD-020C

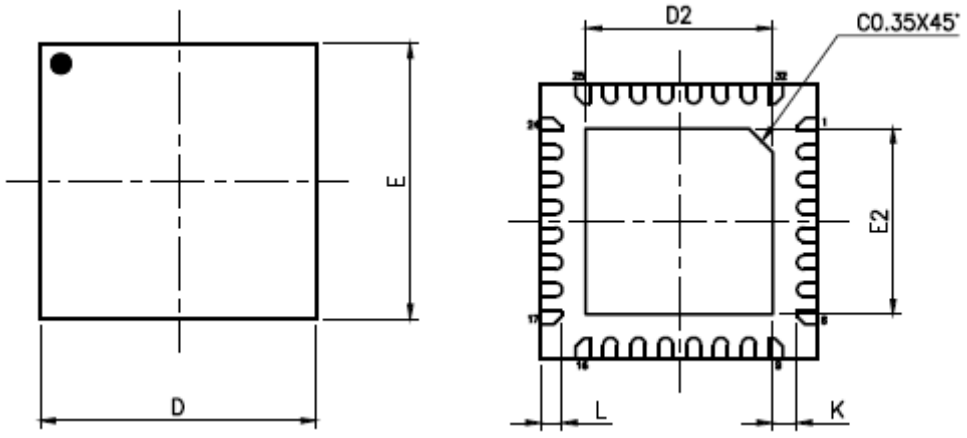
Porfile Feature	Pb Free Package
Average ramp-up rate (217°C to peak)	3°C/sec. max
Preheat temperature 150°C ~200°C	60 sec. to 120 sec.
Temperature maintained above 217°C	60 sec. to 150 sec.
Time with 5°C of actual peak temperature	> 30 sec.
Peak temperature range	260°C
Ramp-down rate	6°C/sec ax.
Time 25°C to peak temperature	8 min. max
Note: 1. Determined according to J-STD-020C	

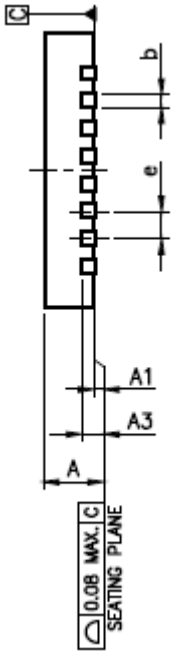
Table 8.6-6 Soldering Profile

9 PACKAGE DIMENSIONS

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

9.1 QFN 33-pin (4.0 x 4.0 x 0.8 mm)





SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D		4.00 BSC	
E		4.00 BSC	
e		0.40 BSC	
L	0.25	0.30	0.35
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
K	0.20	—	—

Figure 9.1-1 QFN-33 Package Dimension

10 ABBREVIATIONS

10.1 Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
BOD	Brown-out Detection
GPIO	General-Purpose Input/Output
Fsys	Frequency of system clock
MIRC	Median Speed RC Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LCD	Liquid Crystal Displays
LDO	Low Dropout Regulator
LIRC	10 kHz internal low speed RC oscillator (LIRC)
LVR	Low Voltage $eset
PDMA	Peripheral Direct Memory Access
POR	Power On Reset
PWM	Pulse Width Modulation
RTC	Real Time Clock
SPI	Serial Peripheral Interface
TK	Touch Key
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WKT	Wakeup Timer
WDT	Watchdog Timer

Table 10.1-1 List of Abbreviations

11 REVISION HISTORY

Date	Revision	Description
2022.07.25	1.00	• Initial version.

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.